## Description

The present invention relates to a video signal generator for generating a signal representing both a main picture and an auxiliary picture simultaneously.

Known picture-in-picture television receivers include two video signal channels, a main and an auxiliary channel, each including a tuner; an IF chain; and a video detector. The information from the auxiliary channel is compressed and stored in a memory in synchronism with the auxiliary video signal. This stored information is retrieved in synchronism with the main video signal and replaces a portion of the main video signal at a predetermined image location. In this way, a picture-in-picture video signal is formed representing an image having a first region which displays the main video image, as represented by the main video signal, and a second, usually smaller, region which displays the auxiliary video image, as represented by the auxiliary video signal. For example, EP-A-0200330 discloses a television apparatus having a picture-in-picture (pix-in-pix) display apparatus. The display apparatus includes circuitry for reducing the amount of memory needed to hold one field of the reduced size image. In the display apparatus, digital samples representing the large and small picture signals are developed at substantially equal rates by separate circuitry. Subsampling circuitry including a memory stores one out of every five of the samples representing a horizontal line of the small picture. These samples are displayed, synchronous with the large picture at a rate three-fifths times the display rate of the large picture samples to produce an apparent size reduction of one-third in the horizontal direction.

An NTSC standard video signal consists of successive frames of 525 lines made-up of two interlaced fields of 262½ lines each. A sampled-data processed NTSC signal sampled at a rate of four times the color subcarrier frequency contains 910 samples in each line. The auxiliary video signal is compressed by, for example, sampling it at the above rate, and storing in the memory only every third sample of every third line. Each field of compressed auxiliary image information, thus, comprises 87 lines of 303 samples each.

In each NTSC video field, 21 lines form a vertical blanking interval (VBI) and do not contain image information. Thus, in general, seven lines (1/3 of 21) of the compressed auxiliary video signal contain VBI signal information and need not be displayed in the inserted auxiliary image. Only the 80 remaining lines contain image information. In addition, in each line, approximately 150 samples form a horizontal blanking interval (HBI) and do not contain image information. Thus, in general, 50 samples (1/3 of 150) of compressed auxiliary video signal contain HBI signal information and need not be displayed in the inserted auxiliary image. Only the 253 remaining samples contain image information.

In each field of a sampled data main video signal, a portion, consisting of 253 adjoining samples of 80 adjoining lines, is replaced by the previously stored non-VBI and HBI compressed auxiliary samples. If this portion is located in the lower right hand corner, for example, samples 607 through 859 (totaling 253 samples) of lines 182 through 261 (totaling 80 lines) of the main video signal may be replaced with the previously stored compressed auxiliary video samples to form the picture-in-picture video signal. Alternatively, the previously stored 80 lines of 253 samples each, which represent the auxiliary image, may be retrieved from the memory, converted into a continuous signal and substituted into a corresponding portion of a main video signal, which is also in continuous form.

The memory may be envisioned as being subdivided into three blocks, each capable of storing one field of compressed auxiliary video information. Successive fields of compressed auxiliary video information are written into these blocks in round robin fashion. Fields of previously stored compressed auxiliary video information are retrieved from the blocks, also in round robin fashion, so that no block is written into and read from simultaneously.

Dual port memories have recently become available which have a high memory capacity (for example, they are capable of storing a full field of video information), and are priced such that integration into a consumer television receiver is feasible. For example, the HM 53051P, 262,144-word 4-bit frame memory, manufactured by Hitachi, is such a dual port video memory system. Such a high capacity memory chip allows flexibility in use which was previously unavailable with lower capacity memory integrated circuits.

The HM 53031P includes a data input terminal and a write address terminal. Standard random access memories (RAM's) require each sample to be stored to be accompanied by an address signal. Unlike the standard RAMs, an address signal need not be supplied concurrently with each sample to be stored for the HM 53031P. Instead, the write address terminal receives an initial write address. Subsequent successive samples are sequentially stored in storage locations beginning at the location corresponding to the last received initial write address. The HM 53031P further includes a data output terminal and a read address terminal. The read address terminal receives an initial read address. Samples are retrieved from sequential loca-

tions in the memory beginning at the location corresponding to the last received initial read address. In the remainder of this specification, such a memory will be referred to as a self-sequencing memory. It is desirable to incorporate such a memory in a picture-in-picture video signal generator.

In accordance with the present invention, there is provided a picture-in-picture video signal generator, including; a source of an auxiliary video signal; means for producing successive samples representing said auxiliary video signal; a source of a main video signal; and means coupled to the data output terminal of a memory and said main video signal source for generating a picture-in-picture video signal; characterized in that: said memory is a self-sequencing memory having, a data input terminal coupled to said means for producing samples and input terminal means for receiving sequences of initial read and write addresses, in that said memory stores samples in sequential storage locations beginning at a location corresponding to the last received write address and retrieves samples from sequential storage locations beginning at a location corresponding to the last received read address; and further characterised by write control circuitry coupled between said source of said auxiliary video signal and said address input terminal of said self-sequencing memory, for producing appropriately occurring sequences of initial write address signals, said write address signals occurring in synchronism with and at the rate of horizontal line intervals of said auxiliary video signal; and read control circuitry coupled between said main video signal source and said address input terminal of said self-sequencing memory, for producing appropriately occurring sequences of initial read address signals, said read address signals occurring in synchronism with and at the rate of horizontal line intervals of said main video signal.

In the drawings:

FIGURE 1 is a block diagram of an exemplary embodiment of a picture-in-picture image signal generator according to the present invention;

FIGURE 2 is a timing diagram useful in understanding the operation of the picture-in-picture video signal generator illustrated in FIGURE 1;

FIGURE 3 is a block diagram illustrating an embodiment of a write address generator which may be used in the picture-in-picture video signal generator illustrated in FIGURE 1;

FIGURE 4 is a memory allocation diagram illustrating a possible memory allocation scheme for the picture-in-picture image signal generator illustrated in FIGURE 1;

FIGURE 5 is a block diagram of a read address generator which may be used in the picture-in-picture video signal generator illustrated in FIGURE 1; and

FIGURE 6 is a block diagram of a vertical enable signal generator which may be used in the read address generator illustrated in FIGURE 4.

For simplicity, in all of the FIGURES, equalizing delays, which may be required in various paths between processing blocks, have been omitted. A person skilled in the art of circuit design would understand where these delays are required and how to implement them properly. In addition, the system illustrated in the FIGURES will produce a black-and-white picture-in-picture video signal. Three such systems may be combined to form a color picture-in-picture video signal. The three may operate on a luminance and two color difference signals, or on red, green and blue color signals. In the detailed description below, both the main and auxiliary video signals are assumed to be sampled data signals. It should be understood that the main video signal could be a continuous signal, and still operate properly.

In FIGURE 1, a source 10 of a main video signal may, for example include an antenna, tuner, IF chain, video detector and luminance/chrominance separator, as found in a standard color television receiver. An output terminal of the main video signal source 10 is coupled to an input terminal of a main sample producer 20. An output terminal of main sample producer 20 is coupled to an input terminal of an auxiliary picture insertion circuit 30. An output terminal of auxiliary picture insertion circuit 30 is coupled to a picture-in-picture video signal processor 40 which may include video amplifiers, a picture tube, and deflection circuitry as found in a standard color television receiver.

An auxiliary video signal source 50 may include, for example, a second tuner, IF chain, video detector and luminance/chrominance separator, similar to those which may be found in the main video signal source 10. An output terminal of the auxiliary video signal source 50 is coupled to an input terminal of an auxiliary sample producer 60. An output terminal of auxiliary sample producer 60 is coupled to a data input terminal of a self-sequencing memory 70. A data output terminal of self-sequencing memory 70 is coupled to a second input terminal of the auxiliary picture insertion circuit 30.

The output terminal of the auxiliary video signal source 50 is also coupled to an input terminal of an auxiliary synchronization component separator 80. A first output terminal of auxiliary synchronization separator 80 is coupled to a write clock input terminal (W CLK) of memory 70. A second output terminal of the auxiliary synchronization component separator 80 is coupled to an input terminal of a write address generator 90. An output terminal of the write address generator 90 is coupled to a write

address input terminal (W ADR) of memory 70. The combination of auxiliary synchronization component separator 80 and write address generator 90 form circuitry which controls the writing of auxiliary video signal samples into self-sequencing memory 70.

The output terminal of main video signal source 10 is also coupled to an input terminal of a main synchronization component separator 100. A first output terminal of main synchronization component separator 100 is coupled to a read clock input terminal (R CLK) of memory 70. A second output terminal of main synchronization component separator 100 is coupled to an input terminal of a read address generator 110. An output terminal of read address generator 110 is coupled to a read address input terminal (R ADR) of memory 70. The combination of main synchronization component separator 100 and read address generator 110 form circuitry which controls the reading of previously stored samples from self-sequencing memory 70.

In operation, auxiliary sample producer 60 produces successive samples representing an auxiliary image. Samples from the auxiliary sample producer 60 are stored in self-sequencing memory 70 in synchronism with the auxiliary video signal. This synchronism is maintained by the clock signal supplied from the first output terminal of the auxiliary synchronization component separator 80 to the write clock input terminal (W CLK) of memory 70. A sample at the data input terminal of memory 70 is written into a memory location when a clock signal is supplied to the write clock input terminal (W CLK).

Samples from only every third line of the auxiliary video signal are stored in self-sequencing memory 70 as part of the compressed auxiliary video signal. In order to store the samples of the compressed auxiliary video signal in the correct location in memory, a write address must be supplied to memory 70 for each line of compressed auxiliary video signal to be stored. This address corresponds to the location into which the first sample of that line is to be stored. Before the beginning of the selected lines of the auxiliary video signal, write address generator 90 supplies that address to the write address terminal (W ADR) of memory 70. Samples of the selected line of the auxiliary video signal field are stored in sequential memory locations beginning at that write initial location.

Samples from self-sequencing memory 70, representing the compressed auxiliary video signal image, are substituted for appropriate main video signal samples in the auxiliary picture insertion circuitry 30. The reading of these previously stored samples from memory 70 is in synchronism with the main video signal source. This synchronism is maintained by the clock signal supplied from the first. output terminal of the main synchronization component separator 100 to the read clock input terminal (R CLK) of memory 70. A sample is read from memory 70 and is presented to the data output terminal when a clock signal is supplied to the read clock input terminal (R CLK).

In the example described above, samples 607 through 859 (totaling 253 samples) of lines 182 through 261 (totaling 80 lines) of the main video signal are replaced with previously stored compressed auxiliary video samples retrieved from memory 70. A counter in the main synchronization component separator 100 counts lines of the main video signal and generates a signal when lines 182 through 261 are being scanned. Another counter counts samples within lines of the main video signal and generates a signal when samples 607 through 859 are being scanned. The concurrence of these two signals indicates that auxiliary video signal samples are to be retrieved from memory 70. Read clock signals are supplied to memory 70 during the period of concurrence.

In order to retrieve samples representing the correct line from memory 70, a read address must be supplied to memory 70 corresponding to the location of the first sample of that line. Before the 607th sample of each of lines 182 through 261 of the main video signal, read address generator 110 supplies an address to the read address terminal (R ADR) of memory 70. This address corresponds to the predetermined read initial location in the memory 70 for the current line. Samples of the previously stored auxiliary video signal are retrieved from sequential memory locations beginning at this read initial location.

As described above, self-sequencing memory 70 (of FIGURE 1) may be envisioned as being subdivided into three blocks designated 1, 2 and 3. Successive fields of auxiliary video samples are written into successive blocks of the memory 70 in round robin fashion. In FIGURE 2, waveform a) is divided into blocks representing auxiliary video signal field time intervals. The number within each division indicates the block number into which compressed data representing that auxiliary video field is being written. For example, the field scanned during the leftmost field time period is written into block 1; the next field is written into block 2; the next into block 3; and so forth. Waveform b) is divided into blocks representing main video signal field time intervals. The number within each division represents the block from which data is read and inserted into the main video signal to form the picture-in-picture video signal. For example, the left-most field is read from block 3; the next field from block 1; the next from block

2; and so forth. This sequencing of the read and write blocks result in no block being written into and read from simultaneously. So that proper sequencing may be maintained, information from the write address generator 90 (of FIGURE 1) may be supplied to the read address generator 110, as shown in phantom in FIGURE 1.

FIGURE 3 illustrates an embodiment of a write address generator 90 which may be used in the picture-inpicture video signal generator illustrated in FIGURE 1. Write address generator 90 supplies an initial write address to self-sequencing memory 70 for each line of compressed auxiliary video signal to be stored. In both FIGURES 3 and 5, thick lines represent multi-bit digital signal paths, and thin lines represent single-bit digital signal paths. The auxiliary synchronization component separator 80 (of FIGURE 1) supplies two signals: a horizontal synchronization component H AUX, and a vertical synchronization component V AUX.

In FIGURE 3, an input terminal 91 is coupled to auxiliary synchronization component separator 80 (of FIGURE 1), and receives the horizontal synchronization component H AUX. Input terminal 91 is coupled to a clock input terminal (indicated by a small triangle) of a divide-by-3 counter 92. An output terminal of divide-by-3 counter 92 is coupled to a clock input terminal of line address counter 94. An output terminal 95 of line address counter 94 is coupled to the write address terminal (W ADR) of self-sequencing memory 70 (of FIGURE 1), and carries the initial write address for each line of the compressed auxiliary video signal.

An input terminal 93 is also coupled to auxiliary synchronization component separator 80 (of FIGURE 1), and receives the vertical synchronization component V AUX. Input terminal 93 is coupled to an input terminal of a count-to-3 counter 96 and a load input terminal LD of line address counter 94. An output terminal 97 of the count-to-3 counter 96 is coupled to a block start address generator 98 and to read address generator 110 (of FIGURE 1). An output of block start address generator 98 is coupled to a jam input terminal of line address counter 94.

The write address generator 90 of FIGURE 3 may be configured to allocate samples representing compressed auxiliary video information to memory locations in the following manner. This exemplary memory allocation scheme, which may be used for the HM 53051P memory chip, is described below and illustrated in FIGURE 4.

The HM 53051P self-sequencing memory stores groups of 32 samples in each storage location. As described above, each line of compressed auxiliary video information consists of 303 samples. Thus, 10 storage locations are required to store each line of compressed auxiliary video information. Also as described above, three blocks of memory, each capable of storing one field consisting of 87 lines, are allocated to store compressed auxiliary video information.

In FIGURE 4, selected storage locations in selfsequencing memory 70 (of FIGURE 1) are illustrated as rectangles. The address which corresponds to that storage location is denoted by its value within the rectangle representing that location. Each row of rectangles represents ten sequential storage locations; enough to contain one line of compressed auxiliary video information. The topmost row, representing storage locations 0 through 9, is allocated to hold samples representing the first horizontal line of a field of compressed auxiliary video information which is to be stored in block 1 (i.e., line 1 of a field n). The second row, representing storage locations 10 through 19, is allocated to hold samples representing line 1 of a field of compressed auxiliary video information which is to be stored in block 2 (i.e., line 1 of a field n+1); and the third row is allocated to hold samples representing line 1 of block 3 (i.e., line 1 of a field n+2).

The fourth row, which represents storage locations 32 through 41, is allocated to hold samples representing the second line of the field of compressed auxiliary video information to be stored in block 1. The fifth row is allocated to hold samples representing line 2 of block 2, and the sixth row is allocated to hold samples representing line 2 of block 3. This pattern continues for all 87 lines. The two memory locations corresponding to addresses 30 and 31 are not allocated to storage of compressed auxiliary video samples. Neither are memory locations corresponding to addresses 62 and 63. Two memory locations remain unallocated for every three lines of compressed auxiliary video signal.

When a field of compressed auxiliary video information is to be written into block 1 of self-sequencing memory 70 (of FIGURE 1), write address counter 90 first produces an address signal having the value 0. This is the address corresponding to the location allocated to store the first group of 32 samples in line 1 of block 1 (see FIGURE 4). Self-sequencing memory 70 stores the next 303 samples in the sequential locations corresponding to address 0 through 9, without requiring further address information. Before the beginning of the second line of that compressed field, write address generator produces an address signal having the value 32, the address corresponding to the location allocated to store the first group of samples in line 2 of block 1. The next 303 samples are stored in locations 32 through 41. The value of the address signal produced before each subsequent line of compressed auxiliary video information is 32 more

than that of the previous line.

When lines of compressed auxiliary video information are being written into block 2, write address generator 90 first produces an address signal having the value 10. Samples representing line 1 of this field are stored in sequential locations corresponding to addresses 10 through 19. With every subsequent line, the value of the address signal is incremented by 32. Thus, samples representing the second line of block 2 is stored in 10 sequential locations beginning at the location corresponding to address 42, and so forth.

Similarly, the value of the first address produced by write address generator 90 when a field is to be stored in block 3 is 20. Samples representing line 1 of this field are stored in sequential locations corresponding to addresses 20 through 29. As before, with every subsequent line to be stored, the value of the address signal is incremented by 32. Samples representing line 2 of fields to be stored in block 3 are stored in locations 52 through 61, and so forth.

Referring again to FIGURE 3, in operation, countto-three counter 96 produces a signal which represents the block number into which the current field is to be stored. For example, count-to-three counter 96 may produce a two-bit binary signal repetitively sequencing through the values 1, 2 and 3. Block start address generator 98 produces a starting address corresponding to the initial memory location allocated to the first line in that block as described above. When the output of count-to-three counter 96 is 1, the starting address is 0; when the output of count-to-three counter 96 is 2, the starting address is 10; when the output of count-to-three counter 96 is 3, the starting address is 20.

Block start address generator 98 may be a read only memory (ROM) having an address input terminal coupled to the output terminal of count-to-three counter 96 and a data output terminal coupled to the jam input terminal of line address counter 94, with the associated predetermined start address values preprogrammed into the memory locations corresponding to the addresses 1, 2 and 3. Alternatively, block start address generator 98 may be combinatorial logic circuitry which generates the predetermined start address values from the 2-bit output of count-to-three counter 96.

At the beginning of each auxiliary video signal field, the start address from block start address generator 98 is loaded into line address counter 94 in response to the auxiliary vertical synchronization signal V AUX. The output of line address counter becomes the same as this predetermined value.

Frequency divider 92 produces a clock pulse at the beginning of every third line of the compressed auxiliary video signal. This clock pulse causes line address counter 94 to increment the value of the signal at its output terminal by 32. The write address counter 90 of FIGURE 3 may, thus, produce the properly valued address signals to implement the memory allocation scheme described above.

Line address counter 94 may, for example, comprise a binary counter, and a 5-bit latch. The 5-bit latch has an input terminal coupled to the jam input terminal of line address counter 94, and a clock terminal coupled to the load terminal LD of line address counter 94. The output terminal of the 5-bit latch is coupled to the 5 lower-significance bits of the output terminal of line address counter 94. The counter has a clear input terminal (CLR) coupled to the load terminal (LD) of line address counter 94, and a clock input terminal coupled to the clock input terminal of line address counter 94. An output terminal of the binary counter is coupled to the remaining higher significance bits of the output terminal of line address counter 94.

In operation, the 5-bit latch is coupled to receive the output of the block start address generator 98. As described above, for block 1, the start address is 0, or '00000' in 5-bit binary; for block 2, the start address is 10, or '01010' in 5-bit binary; for block 3, it is 20 or '10100'. When an auxiliary vertical synchronization signal occurs, the appropriate 5-bit binary value is latched into the 5-bit latch, and becomes the 5 lesser signficance bits of the initial write address. At that same time, the binary counter CNTR is cleared to a count of 0. The resulting initial write address is 0, 10, or 20, as appropriate. As each clock signal occurs at the clock input terminal (CNTR) of the counter its output value increments by one. Because the 5 lesser significance bits are supplied from the 5-bit latch, when the output from the binary counter CNTR increments by one, the value of the initial write address increments by 32. This arrangement can thus produce the required sequence of addresses for the memory allocation scheme illustrated in FIGURE 4 in response to the load and clock signals.

FIGURE 5 illustrates a read address generator 110 which may be used in the picture-in-picture signal generator illustrated in FIGURE 1. In FIGURE 5, input terminals 111, 113, and 119 are all coupled to the main synchronization component signal separator 100 (of FIGURE 1). Input terminal 111 receives a horizontal synchronization component signal H MAIN, and is coupled to a first input terminal of a vertical enable signal generator 112 and a clock input terminal of line address counter 114. Input terminal 113 receives a vertical synchronization component signal V MAIN, is coupled to a load input terminal LD of line address counter 114. Input terminal 119 receives a vertical blanking sig-

nal .V BLNK MAIN, and is coupled to a second input terminal of vertical enable signal generator 112. An output terminal of vertical enable signal generator 112 is coupled to an enable E input terminal of a line address counter 114. An output terminal 117 of line address counter 114 is coupled to the read address input terminal (R ADR) of memory 70 (of FIGURE 1).

An input terminal 115 is coupled to write address generator 90 (of FIGURE 1). Input terminal 115 is coupled to an input terminal of delay 116. An output terminal of delay 116 is coupled to an input terminal of a block start address generator 118. An output terminal of block start address generator 118 is coupled to a jam input terminal of line address counter 114.

In operation, delay 116 receives a signal which corresponds to the sequence of block numbers represented in waveform a) of FIGURE 2, and produces a signal which corresponds to the sequence of block numbers represented in waveform b) of FIGURE 2. The output signal from delay 116 represents the block number of memory from which previously stored compressed auxiliary video information is to be retrieved. Block start address generator 118 generates the predetermined starting address (i.e., 0, 10 or 20) corresponding to the memory block number in a similar manner to that described above for block start address generator 98 of write address generator 90 (of FIGURE 3). The main vertical synchronization signal V MAIN, indicating the start of a new field of main video information, conditions line address counter 114 to load the starting address from block start address generator 118 at the beginning of every main vertical scanning interval. This starting address forms the first initial read address.

Vertical enable signal generator 112 generates an enable signal for line address counter 114. The enable signal is produced while the main video signal is scanning lines 182 through 261, into which previously stored auxiliary video signal information is to be inserted. While line address counter 114 is enabled, the main horizontal synchronization component signal H MAIN clock, indicating the start of a new line of main video information, causes the line address counter 114 to increment. Line address counter 114 increments by 32 in a similar manner to the line address counter 94 of the write address generator 90 illustrated in FIGURE 3. The output of line address counter 114 is the initial read address for the next line of previously stored compressed auxiliary video information to be inserted into the main video signal. Once this address is supplied to self-sequencing memory 70 (of FIGURE 1), subsequent previously stored auxiliary video samples will be retrieved from sequential storage locations of memory 70 without requiring further address information.

FIGURE 6 illustrates an embodiment of a vertical enable signal generator 112, which may be used in the read address generator 110 of FIGURE 5. Vertical enable signal generator 112 generates a signal indicating that the 80 lines of the main video signal, into which the auxiliary video image is to be inserted, are currently being scanned. This signal is used to enable line address counter 114 of read address generator 110 illustrated in FIGURE 5. Until enabled, line address counter 114 produces the address of the storage location containing the first sample of the first line in the memory block from which this data is to be retrieved. When enabled, line address counter is incremented by 32 at each subsequent line of the main video signal. It thus produces the address corresponding to the storage location containing the first sample of the corresponding line of the previously stored compressed auxiliary video information.

In FIGURE 6, input terminals 1121 and 1123 are coupled to the main synchronization component separator 100. Input terminal 1121 receives horizontal synchronization signal H MAIN. Input terminal 1123 receives vertical blanking signal V BLNK MAIN. Input terminal 1121 is coupled to a clock input terminal of divide-by-80 counter 1122. An output terminal of divide-by-80 counter 1122 is coupled to a clock input terminal of a divide-by-3 ring counter 1124. Ring counter 1124 includes three output terminals $Q_A$, $Q_B$ and $Q_C$. These output terminals are coupled to respective input terminals of a selector switch 1126. An output terminal of selector switch 1126 is coupled to an output terminal 1125. Output terminal 1125 is coupled to the enable input terminal (E) of line address counter 114 (of FIGURE 5). Input terminal 1123 is coupled to respective reset terminals (R) of divide-by-80 counter 1122 and ring counter 1124.

In operation, the main vertical blanking signal V BLNK MAIN, is present during the first 21 lines of each field of the main video signal and indicates that the vertical blanking interval (VBI as described above) of the main video signal is being scanned. This signal conditions the divide by 80 counter 1122 to produce logic signals at outputs ($Q_A$, $Q_B$, $Q_C$) of (1,0,0) respectively. The main horizontal synchronization component H MAIN causes divide by 80 counter to increment at the beginning of every main video signal horizontal line.

During the first 80 lines after the VBI (i.e., lines 22 through 101), the outputs ($Q_A$,$Q_B$,$Q_C$) of ring counter 1124 produce logic signals (1,0,0) respectively. After 80 lines of the main video signal have been counted by divide-by-80 counter 1122, a clock pulse is provided to ring counter 1124. The logic signals at output terminals ($Q_A$, $Q_B$, $Q_C$) are then (0,1,0), respectively. These logic signals re-

main during the next 80 lines (i.e., lines 102 through 181). After another 80 lines is counted by divide by 80 counter 1122, another clock pulse is supplied to ring counter 1124. Ring counter 1124 output terminals ($Q_A$, $Q_B$, $Q_C$) then produce logic signals (0,0,1). These logic signals remain during the next 80 lines (i.e., lines 182 through 261). $Q_A$ is thus a logic '1' signal during a top third of the picture-in-picture image, and a logic '0' signal otherwise: output terminal $Q_B$ is a logic '1' signal during a middle third and output terminal $Q_C$ is a logic '1' signal during a lower third of the picture-in-picture image and are logic '0' signals otherwise. Selector switch 1126, supplies one of the output signals from ring counter 1124 to output terminal 1125. The vertical location of the auxiliary video image in the picture-in-picture video image is selected by enabling line address counter 114 of the read address counter 110 (of FIGURE 4) during either the top, middle or bottom third of the picture-in-picture image.

In the following Claims, the term self-sequencing memory is a memory which stores samples in sequential storage locations beginning at a location corresponding to the last received write address and retrieves samples from sequential storage locations beginning at a location corresponding to the last received read address. Moreover, while an embodiment of the invention has been described which operates for NTSC television signals, the invention may also be adapted for other, e.g. PAL, television standards.

## Claims

1. A picture-in-picture video signal generator, including;

a source (50) of an auxiliary video signal;

means (60) for producing successive samples representing said auxiliary video signal;

a source (10) of a main video signal; and

means (20,30) coupled to the data output terminal of a memory and said main video signal source for generating a picture-in-picture video signal; characterized in that

said memory is a self-sequencing memory (70) having, a data input terminal coupled to said means for producing samples and input terminal means for receiving sequences of initial read and write addresses, in that said memory stores samples in sequential storage locations beginning at a location corresponding to the last received write address and retrieves samples from sequential storage locations beginning at a location corresponding to the last received read address; and further characterized by:

write control circuitry (80,90) coupled between said source of said auxiliary video signal and said address input terminal of said self-sequencing memory, for producing appropriately occurring sequences of initial write address signals, said write address signals occurring in synchronism with and at the rate of horizontal line intervals of said auxiliary video signal; and

read control circuitry (100,110) coupled between said main video signal source and said address input terminal of said selfsequencing memory, for producing appropriately occurring sequences of initial read address signals, said read address signals occurring in synchronism with and at the rate of horizontal line intervals of said main video signal.

2. The picture-in-picture video signal generator, of Claim 1, wherein said read control circuitry comprises a synchronization component separator (100) coupled to said main video signal source (10), for producing a main horizontal synchronization signal; and produces successive initial read address signals in synchronism with said main horizontal synchronization signal.

3. The picture-in-picture video signal generator, of Claim 2, wherein:

said synchronization component separator (100) also produces main vertical synchronization and blanking signals; and said read control circuitry further includes a read address generator (110) comprising:

a line address counter (114), responsive to said main horizontal synchronization signal, and having an enable input terminal, for producing a signal representing said initial read address in response to a signal at said enable input terminal;

a vertical enable signal generator (112), responsive to said main horizontal synchronization and vertical blanking signals, and having an output terminal coupled to said enable terminal of said line address counter, for generating said enable signal when currently scanned lines of said main video signal are to have auxiliary image information inserted into them; and

means responsive to said main vertical synchronization signal (113), for setting said line address counter to a predetermined value at the beginning of a vertical scan of said main video signal.

4. The picture-in-picture video signal generator of Claim 3, wherein said vertical enable signal generator (112) comprises a ring counter

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main during the next 80 lines (i.e., lines 102 through 181). After another 80 lines is counted by divide by 80 counter 1122, another clock pulse is supplied to ring counter 1124. Ring counter 1124 output terminals ($Q_A$, $Q_B$, $Q_C$) then produce logic signals (0,0,1). These logic signals remain during the next 80 lines (i.e., lines 182 through 261). $Q_A$ is thus a logic '1' signal during a top third of the picture-in-picture image, and a logic '0' signal otherwise: output terminal $Q_B$ is a logic '1' signal during a middle third and output terminal $Q_C$ is a logic '1' signal during a lower third of the picture-in-picture image and are logic '0' signals otherwise. Selector switch 1126, supplies one of the output signals from ring counter 1124 to output terminal 1125. The vertical location of the auxiliary video image in the picture-in-picture video image is selected by enabling line address counter 114 of the read address counter 110 (of FIGURE 4) during either the top, middle or bottom third of the picture-in-picture image.

In the following Claims, the term self-sequencing memory is a memory which stores samples in sequential storage locations beginning at a location corresponding to the last received write address and retrieves samples from sequential storage locations beginning at a location corresponding to the last received read address. Moreover, while an embodiment of the invention has been described which operates for NTSC television signals, the invention may also be adapted for other, e.g. PAL, television standards.

## Claims

1. A picture-in-picture video signal generator, including;

   a source (50) of an auxiliary video signal;

   means (60) for producing successive samples representing said auxiliary video signal;

   a source (10) of a main video signal; and

   means (20,30) coupled to the data output terminal of a memory and said main video signal source for generating a picture-in-picture video signal; characterized in that

   said memory is a self-sequencing memory (70) having, a data input terminal coupled to said means for producing samples and input terminal means for receiving sequences of initial read and write addresses, in that said memory stores samples in sequential storage locations beginning at a location corresponding to the last received write address and retrieves samples from sequential storage locations beginning at a location corresponding to the last received read address; and further characterized by:

   write control circuitry (80,90) coupled between said source of said auxiliary video signal and said address input terminal of said self-sequencing memory, for producing appropriately occurring sequences of initial write address signals, said write address signals occurring in synchronism with and at the rate of horizontal line intervals of said auxiliary video signal; and

   read control circuitry (100,110) coupled between said main video signal source and said address input terminal of said selfsequencing memory, for producing appropriately occurring sequences of initial read address signals, said read address signals occurring in synchronism with and at the rate of horizontal line intervals of said main video signal.

2. The picture-in-picture video signal generator, of Claim 1, wherein said read control circuitry comprises a synchronization component separator (100) coupled to said main video signal source (10), for producing a main horizontal synchronization signal; and produces successive initial read address signals in synchronism with said main horizontal synchronization signal.

3. The picture-in-picture video signal generator, of Claim 2, wherein:

   said synchronization component separator (100) also produces main vertical synchronization and blanking signals; and said read control circuitry further includes a read address generator (110) comprising:

   a line address counter (114), responsive to said main horizontal synchronization signal, and having an enable input terminal, for producing a signal representing said initial read address in response to a signal at said enable input terminal;

   a vertical enable signal generator (112), responsive to said main horizontal synchronization and vertical blanking signals, and having an output terminal coupled to said enable terminal of said line address counter, for generating said enable signal when currently scanned lines of said main video signal are to have auxiliary image information inserted into them; and

   means responsive to said main vertical synchronization signal (113), for setting said line address counter to a predetermined value at the beginning of a vertical scan of said main video signal.

4. The picture-in-picture video signal generator of Claim 3, wherein said vertical enable signal generator (112) comprises a ring counter

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(1124) coupled to the output of a frequency divider (1122) which is responsive to said main horizontal synchronization signal.

5. The picture-in-picture video signal generator of Claim 3, wherein:

memory locations of said self-sequencing memory (70) are allocated as a plurality of blocks, each of which can store one field of auxiliary video signal information; and

said read line address counter setting means comprises means (96,116) for producing a signal representing the block of said self-sequencing memory from which samples representing a previously stored field of said auxiliary video signal are to be retrieved; a block start address generator (118), coupled to said block representative signal producing means, for producing a signal representing the initial read address of the first line of said block of said self-sequencing memory; and means for setting said line address counter (114) to said initial read address of said first line at the beginning of the time period of insertion of said auxiliary video signal information into said picture-in-picture video signal.

6. The picture-in-picture video signal generator of Claim 5, wherein said block representative signal producing means includes a delay circuit (116).

7. The picture-in-picture video signal generator of any preceding claim wherein said write control circuitry comprises: a synchronization component separator (80), coupled to said auxiliary video signal source (50), for producing an auxiliary horizontal synchronization signal, and said write control circuitry produces (90) said successive initial write address signals in synchronism with said auxiliary horizontal synchronization signal.

8. The picture-in-picture video signal generator of Claim 7, wherein:

said synchronization component separator (80) further produces an auxiliary vertical synchronization signal; and said write control circuitry further includes a write address generator (90) comprising:

a frequency divider (92) responsive to said auxiliary horizontal synchronization signal, and having an output terminal;

a line address counter (94) having a clock input terminal coupled to said output terminal of said frequency divider and an output terminal for producing at least a component of said initial write address; and

means, responsive to said auxiliary vertical synchronization signal (93), for setting said line address counter to a predetermined count at the beginning of a vertical scan of said auxiliary video signal.

9. The picture-in-picture video signal generator of Claim 3 or 8, wherein said line address counter (94;114) comprises:

a latch for producing lower significance bits of said initial read or write address; and

a binary counter for producing higher significance bits of said initial read or write address.

10. The picture-in-picture video signal generator of Claim 8 or 9, wherein:

memory locations of said self-sequencing memory (70) are allocated as a plurality of blocks, each of which can store one field of auxiliary video signal information; and

said write line address counter setting means comprises a field counter (96) responsive to said auxiliary vertical synchronization signal for producing a signal representing the block of said self-sequencing memory into which samples representing a current field of said auxiliary video signal is to be written; a block start address generator (98), coupled to said field counter, for producing a signal representing the initial write address of the first line of said block of said self-sequencing memory; and means for setting said line address counter to said initial write address of said first line at the beginning of said current field of said auxiliary video signal.

**Patentansprüche**

1. Bild-in-Bild-Videosignalerzeuger;

mit einer Hilfs-Videosignalquelle (50);

mit Mitteln (60) zur Erzeugung aufeinanderfolgender Abtastungen, die das Hilfs-Videosignal darstellen;

mit einer Haupt-Videosignalquelle (10); und

mit Mitteln (20, 30), die mit der Datenausgangsklemme eines Speichers und der Haupt-Videosignalquelle gekoppelt sind, um ein Bild-in-Bild-Videosignal zu erzeugen, dadurch gekennzeichnet, daß

der Speicher ein selbst die Reihenfolge bestimmender Speicher (70) ist, der eine mit den Mitteln zur Erzeugung von Abtastungen gekoppelte Dateneingangsklemme und Eingangsklemmenmittel zum Empfang von Folgen von Anfangs-Lese- und Schreibadressen hat, daß der Speicher Abtastungen in aufeinander-

folgenden Speicherplätzen speichert, die an einem Platz beginnen, der der letzten empfangenen Schreibadresse entspricht, und Abtastungen von aufeinanderfolgenden Speicherplätzen wiedergewinnt, die an einem Platz beginnen, der der letzten empfangenen Leseadresse entspricht, und

daß zwischen der Hilfs-Videosignalquelle und der Adressen-Eingangsklemme des selbst die Reihenfolge bestimmenden Speichers eine Schreibsteuerschaltung (80, 90) gekoppelt ist, um geeignet auftretende Folgen von Anfangs-Schreibadressen-Signalen zu erzeugen, wobei die Schreibadressen-Signale synchron mit und mit der Frequenz von horizontalen Zeilenintervallen des Hilfs-Videosignals auftreten, und

daß zwischen der Haupt-Videosignalquelle und der Adressen-Eingangsklemme des selbst die Reihenfolge bestimmenden Speichers eine Lese-Steuerschaltung (100, 110) gekoppelt ist, um geeignet auftretende Folgen von Anfangs-Leseadressen-Signalen zu erzeugen, wobei die Leseadressen-Signale synchron mit und mit der Frequenz von horizontalen Zeilenintervallen des Haupt-Videosignals auftreten.

2. Bild-in-Bild-Videosignalerzeuger nach Anspruch 1, bei dem die Lese-Steuerschaltung eine Snchronkomponenten-Abtrennstufe (100) enthält, die mit der Haupt-Videosignalquelle (10) gekoppelt ist, um ein Haupt-Horizontal-Synchron-Signal zu erzeugen; und aufeinanderfolgende Anfangs-Leseadressen-Signale synchron mit dem Haupt-Horizontal-Synchron-Signal erzeugt.

3. Bild-in-Bild-Videosignalerzeuger nach Anspruch 2, bei dem die Synchronkomponenten-Abtrennstufe (100) ferner Haupt-Vertikal-Synchron- und Austastsignale erzeugt, und bei dem die Lese-Steuerschaltung ferner einen Leseadressen-Generator (110) enthält, umfassend:

einen Zeilen-Adressen-Zähler (114), der auf das Haupt-Horizontal-Synchron-Signal anspricht und eine Auslöse-Eingangsklemme besitzt, um ein die Eingangs-Leseadresse darstellendes Signal in Abhängigkeit von einem Signal an der Auslöse-Eingangsklemme zu erzeugen;

einen Vertikal-Auslösesignal-Generator (112), der auf das Haupt-Horizontal-Synchron-Signal und die Vertikal-Austastsignale anspricht, und der eine Ausgangsklemme besitzt, die mit der Auslöse-Klemme des Zeilen-Adressen-Zählers gekoppelt ist, um das Auslösesignal zu erzeugen, wenn laufend abgetastete Zeilen des Haupt-Videosignals eine in sie einzufügende Hilfs-Bildinformation haben sollen; und

auf das Haupt-Vertikal-Synchron-Signal ansprechende Mittel (113), um den Zeilen-Adressen-Speicher auf einen vorgegebenen Wert am Anfang einer vertikalen Abtastung des Haupt-Videosignals zu setzen.

4. Bild-in-Bild-Videosignalerzeuger nach Anspruch 3, bei dem der Vertikal-Auslösesignal-Generator (112) einen Ringzähler (1124) umfaßt, der mit dem Ausgang eines Frequenzteilers (1122) gekoppelt ist, der auf das Haupt-Horizontal-Synchron-Signal anspricht.

5. Bild-in-Bild-Videosignalerzeuger nach Anspruch 3, bei dem die Speicherplätze des selbst die Reihenfolge bestimmenden Speichers (70) als eine Vielzahl von Blöcken angeordnet sind, von denen jeder ein Halbbild einer Hilfs-Videosignalinformation speichern kann; und

bei dem die Setzmittel für den Lese-Zeilen-Adressenzähler Mittel (96, 116) enthalten, um ein Signal zu erzeugen, das den Block des selbst die Reihenfolge bestimmenden Speichers darstellt, von dem Abtastungen, die ein zuvor gespeichertes Halbbild des Hilfs-Videosignals darstellen, wiedergewonnen werden sollen, wobei ein Block-Startadressen-Generator (118) mit den Mitteln zur Erzeugung des den Block darstellenden Signals gekoppelt ist, um ein Signal zu erzeugen, das die Anfangs-Leseadresse der ersten Zeile des Blocks des selbst die Reihenfolge bestimmenden Speichers darstellt; und wobei Mittel vorgesehen sind, um den Zeilen-Adressen-Zähler (114) auf die Anfangs-Leseadresse der ersten Zeile am Beginn der Zeitperiode zum Einfügen der Hilfs-Videoinformation in das Bild-in-Bild-Videosignal zu setzen.

6. Bild-in-Bild-Videosignalerzeuger nach Anspruch 5, bei dem die Mittel zur Erzeugung des den Block darstellenden Signals eine Verzögerungsschaltung (116) enthalten.

7. Bild-in-Bild-Videosignalerzeuger nach einem der vorhergehenden Ansprüche, bei dem die Schreibsteuerschaltung umfaßt: eine Synchronkomponenten-Abtrennstufe (80), die mit der Hilfs-Videosignalquelle (50) gekoppelt ist, um ein Hilfs-Horizontal-Synchron-Signal zu erzeugen, und wobei die Schreibsteuerschaltung (90) die aufeinanderfolgenden Anfangs-Schreibadressen-Signale synchron mit dem Hilfs-Horizontal-Synchron-Signal erzeugt.

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8. Bild-in-Bild-Videosignalerzeuger nach Anspruch 7, bei dem die Synchronkomponenten-Abtrennstufe (80) ferner ein Hilfs-Vertikal-Synchron-Signal erzeugt, und bei dem die Schreibsteuerschaltung ferner einen Schreibadressen-Generator (90) enthält, umfassend:

einen Frequenzteiler (92), der auf das Hilfs-Horizontal-Synchron-Signalanspricht und eine Ausgangsklemme hat;

einen Zeilen-Adressen-Zähler (94), der eine mit der Ausgangsklemme des Frequenzteilers gekoppelte Takt-Eingangsklemme und eine Ausgangsklemme zur Erzeugung wenigstens einer Komponente der Anfangs-Schreibadresse hat; und

auf das Hilfs-Vertikal-Synchron-Signal (93) ansprechende Mittel zum Setzen des Zeilen-Adressen-Zählers auf eine vorgegebene Zählung am Beginn einer vertikalen Abtastung des Hilfs-Videosignals.

9. Bild-in-Bild-Videosignalerzeuger nach Anspruch 3 oder 8, bei dem der Zeilen-Adressen-Zähler (94; 114)

einen Latch zur Erzeugung von Bits der Anfangs-Lese- oder Schreibadresse mit niedrigerer Signifikanz und

einen Binärzähler zur Erzeugung von Bits der Anfangs-Lese- oder Schreibadresse mit höherer Signifikanz umfaßt.

10. Bild-in-Bild-Videosignalerzeuger nach Anspruch 8 oder 9, bei dem Speicherplätze des selbst die Reihenfolge bestimmenden Speichers (70) als eine Vielzahl von Blöcken angeordnet sind, von denen jeder ein Halbbild der Hilfs-Videosignalinformation speichern kann; und

bei dem die Setzmittel für den Schreib-Zeilen-Adressen-Zähler einen Halbbild-Zähler (96) enthalten, der auf das Hilfs-Vertikel-Synchron-Signal anspricht, um ein Signal zu erzeugen, das den Block des selbst die Reihenfolge bstimmenden Speichers darstellt, in den ein laufendes Halbbild des Hilfs-Videosignals darstellende Abtastungen eingeschrieben werden sollen; wobei ein Block-Startadressen-Generator (98) mit dem Halbbild-Zähler gekoppelt ist, um ein Signal zu erzeugen, das die Anfangs-Schreibadresse der ersten Zeile des Blocks des selbst die Reihenfolge bestimmenden Speichers darstellt; und wobei Mittel zum Setzen des Zeilen-Adressen-Zählers auf die Anfangs-Schreibadresse der ersten Zeile am Beginn des laufenden Halbbildes des Hilfs-Videosignals vorgesehen sind.

**Revendications**

1. Générateur de signal vidéo du type image-en-image comportant :
   - une source (50) d'un signal vidéo auxiliaire ;
   - des moyens (60) pour produire des échantillons successifs représentant ledit signal vidéo auxiliaire ;
   - une source (10) d'un signal vidéo principal et ;
   - des moyens (20, 30) couplés à la borne de sortie de données d'une mémoire et à ladite source de signal vidéo principal pour générer un signal vidéo image-en-image, caractérisé en ce que :
   - ladite mémoire est une mémoire à auto-classement (70) comportant une borne d'entrée de données couplée auxdits moyens pour produire des échantillons, et des moyens de borne d'entrée pour recevoir des signaux initiaux d'adresses de lecture et d'écriture, en ce que ladite mémoire stocke des échantillons en des emplacements de stockage séquentiels débutant à un emplacement correspondant à l'adresse d'écriture reçue en dernier et elle extrait des échantillons d'emplacements de stockage séquentiels commençant à un emplacement qui correspond à la dernière adresse de lecture reçue et caractérisé en outre par :
   - un circuit de commande d'écriture (80, 90) couplé entre ladite source de signal vidéo auxiliaire et ladite borne d'entrée d'adresse de ladite mémoire à auto-classement, afin de produire des séquences, survenant de façon appropriée, de signaux initiaux d'adresse d'écriture, lesdits signaux d'adresse d'écriture survenant en synchronisme avec, et à la vitesse, des intervalles de lignes horizontales dudit signal vidéo auxiliaire et ;
   - un circuit de commande de lecture (100 - 110) couplé entre ladite source de signal vidéo principal et la borne d'entrée d'adresse de la mémoire à auto-classement, pour produire des séquences survenant de façon appropriée, de signaux initiaux d'adresse de lecture, lesdits signaux d'adresse de lecture survenant en synchronisme avec, et à la vitesse des intervalles de lignes horizontales, du signal vidéo principal.

2. Générateur de signal vidéo du type image-en-image selon la revendication 1 dans lequel ledit circuit de commande de lecture com-

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prend un séparateur de composante de synchronisation (100), couplé à ladite source de signal vidéo principal (10) pour produire un signal de synchronisation horizontale principal et il produit des signaux initiaux d'adresse de lecture successifs en synchronisme avec ledit signal principal de synchronisation horizontale.

3. Générateur de signal vidéo image-en-image selon la revendication 2 dans lequel :
   - ledit séparateur de composante de synchronisation (100) produit également des signaux principaux de suppression et de synchronisation verticales et ledit circuit de commande de lecture comprend un générateur d'adresses de lecture (110) comprenant :
   - un compteur d'adresses de lignes (114) agissant en réponse audit signal principal de synchronisation horizontale, et comportant une borne d'entrée d'activation pour produire un signal représentant ladite adresse de lecture initiale en réponse à un signal à ladite borne d'entrée d'activation ;
   - un générateur de signal d'activation verticale (112), agissant en réponse auxdits signaux principaux de suppression verticale et de synchronisation horizontale, et ayant une borne de sortie couplée à ladite borne d'activation du compteur d'adresses de lignes, pour générer ledit signal d'activation lorsqu'il est nécessaire d'insérer dans des lignes en cours de balayage dudit signal vidéo principal, une information d'image auxiliaire et ;
   - des moyens agissant en réponse audit signal de synchronisation verticale principal (113) pour régler ledit compteur d'adresses de lignes à une valeur prédéterminée au début d'un balayage vertical dudit signal vidéo principal.

4. Générateur de signal vidéo image-en-image selon la revendication 3 dans lequel ledit générateur de signal d'activation vertical (112) comprend un compteur annulaire (1124) couplé à la sortie d'un diviseur de fréquence (1122) qui agit en réponse audit signal de synchronisation horizontale, principal.

5. Générateur de signal vidéo image-en-image selon la revendication 3 dans lequel :
   - des emplacements de mémoire de ladite mémoire à autoclassement (70) sont affectés en tant qu'une pluralité de blocs, chacun d'eux pouvant stocker un champ de l'information de signal vidéo auxiliaire et ;
   - lesdits moyens de réglage du compteur d'adresses de lignes de lecture comprennent des moyens (96 - 116) pour produire un signal représentant le bloc de ladite mémoire à auto-classement à partir duquel doivent être extraits des échantillons représentant un champ préalablement stocké dudit signal vidéo auxiliaire ; un générateur d'adresses de départ de bloc (118), couplé auxdits moyens produisant un signal représentatif de bloc pour produire un signal représentant l'adresse de lecture initiale de la première ligne dudit bloc de la mémoire à auto-classement et, des moyens pour régler ledit compteur d'adresses de lignes (114) à ladite adresse de lecture initiale de ladite première ligne au début de la période de temps de l'insertion de l'information de signal vidéo auxiliaire dans ledit signal vidéo image-en-image.

6. Générateur de signal vidéo image-en-image selon la revendication 5 dans lequel les moyens de production de signal représentatif du bloc comportent un circuit retard (116).

7. Générateur de signal vidéo image-en-image selon l une quelconque des revendications précédentes dans lequel ledit circuit de commande d'écriture comprend : un séparateur de composantes de synchronisation (80), couplé à ladite source de signal vidéo auxiliaire (50), pour produire un signal de synchronisation horizontale auxiliaire et, ledit circuit de commande d'écriture produit (90) lesdits signaux initiaux d'adresses d'écriture successifs en synchronisme avec ledit signal auxiliaire de synchronisation horizontale.

8. Générateur de signal vidéo image-en-image selon la revendication 7 dans lequel :
   - ledit séparateur de composantes de synchronisation (80) produit en outre un signal auxiliaire de synchronisation verticale et, ledit circuit de commande d'écriture comprend en outre un générateur d'adresses d'écriture (90) comprenant :
   - un diviseur de fréquences (92) agissant en réponse audit signal auxiliaire de synchronisation horizontale et comportant une borne de sortie ;
   - un compteur d'adresses de lignes (94) comportant une borne d'entrée d'horloge couplée à ladite borne de sortie du diviseur de fréquences et une borne de sortie pour produire au moins une compo-

sante de ladite adresse d'écriture initiale et,

- des moyens, agissant en réponse audit signal auxiliaire de synchronisation verticale (93) pour régler ledit compteur d'adresses de lignes à un compte prédéterminé au début d'un balayage vertical dudit signal vidéo auxiliaire.

9. Générateur de signal vidéo image-en-image selon la revendication 3 ou 8 dans lequel le compteur d'adresses de lignes (94 ; 114) comprend :
   - une bascule pour produire des bits d'importance inférieure de ladite adresse initiale de lecture ou d'écriture et ;
   - un compteur binaire pour produire des bits d'importance supérieure de ladite adresse initiale de lecture et d'écriture.

10. Générateur de signal vidéo image-en-image selon la revendication 8 ou 9 dans lequel :
   - des emplacements de mémoire de ladite mémoire à autoclassement (70) sont affectés en tant qu'une pluralité de blocs, chacun d'eux pouvant stocker un champ d'informations de signal vidéo auxiliaire et ;
   - lesdits moyens de réglage du compteur d'adresses de lignes d'écriture comprennent un compteur de champ (96) agissant en réponse audit signal de synchronisation verticale auxiliaire pour produire un signal représentant le bloc de ladite mémoire à auto-classement dans lequel doivent être écrits des échantillons représentant un champ courant dudit signal vidéo auxiliaire ; un générateur d'adresses de départ de bloc (98) couplé audit compteur de champ pour produire un signal représentant l'adresse d'écriture initial de la première ligne dudit bloc de la mémoire à auto-classement et, des moyens pour régler ledit compteur d'adresses de lignes sur ladite adresse d'écriture initiale de ladite première ligne, au début du champ courant dudit signal vidéo auxiliaire.