FIG. 1

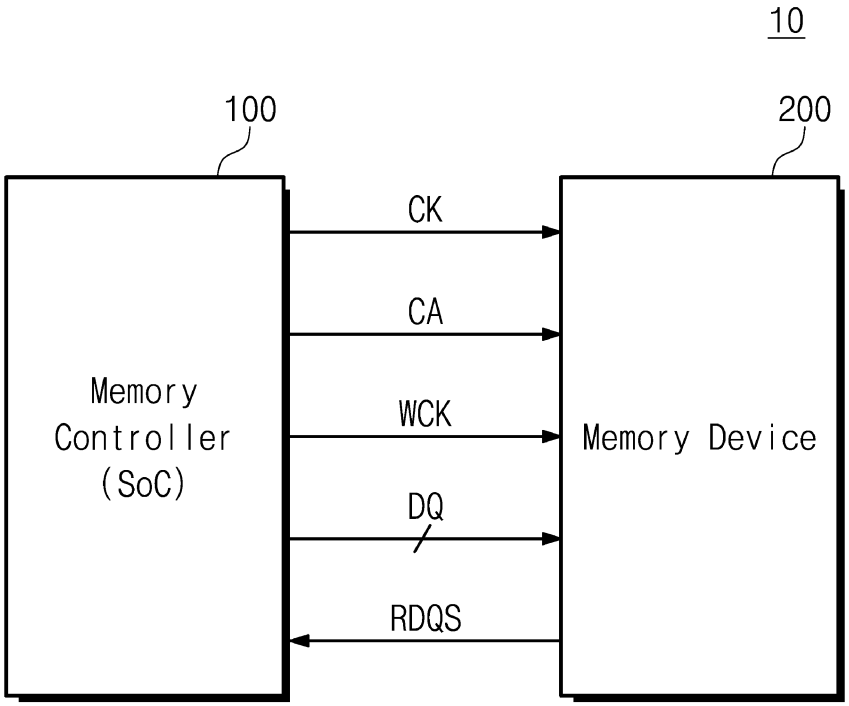

10
100
200
Memory Controller (SoC)
Memory Device
CK
CA
WCK
DQ
RDQS

FIG. 2

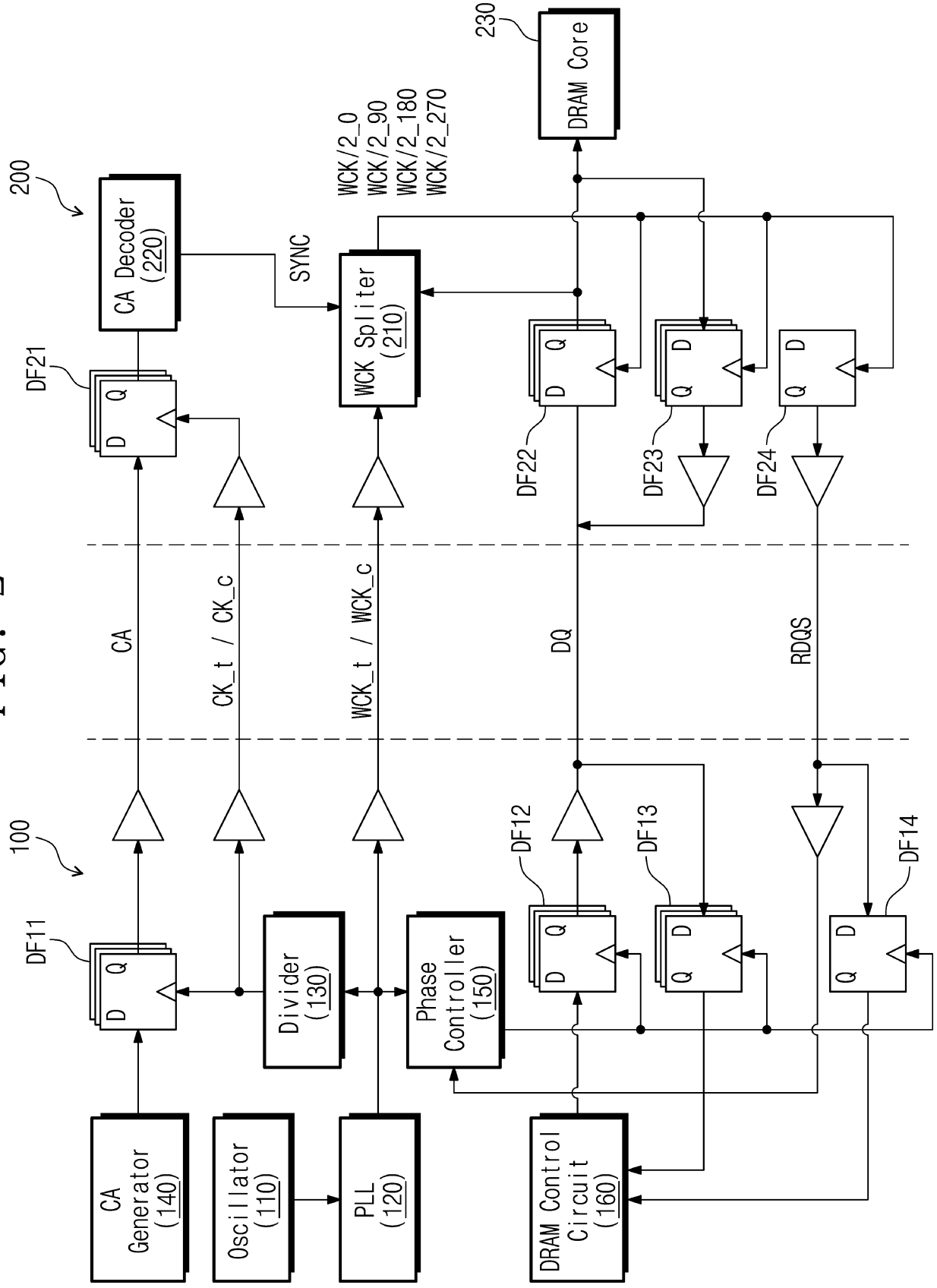

100
200
230
CA Generator (140)
Oscillator (110)
PLL (120)
Divider (130)
Phase Controller (150)
DRAM Control Circuit (160)
CA Decoder (220)
WCK Spliter (210)
DRAM Core
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DF11
DF12
DF13
DF14
DF21
DF22
DF23
DF24
D Q
CA
CK_t / CK_c
WCK_t / WCK_c
DQ
RDQS

FIG. 3

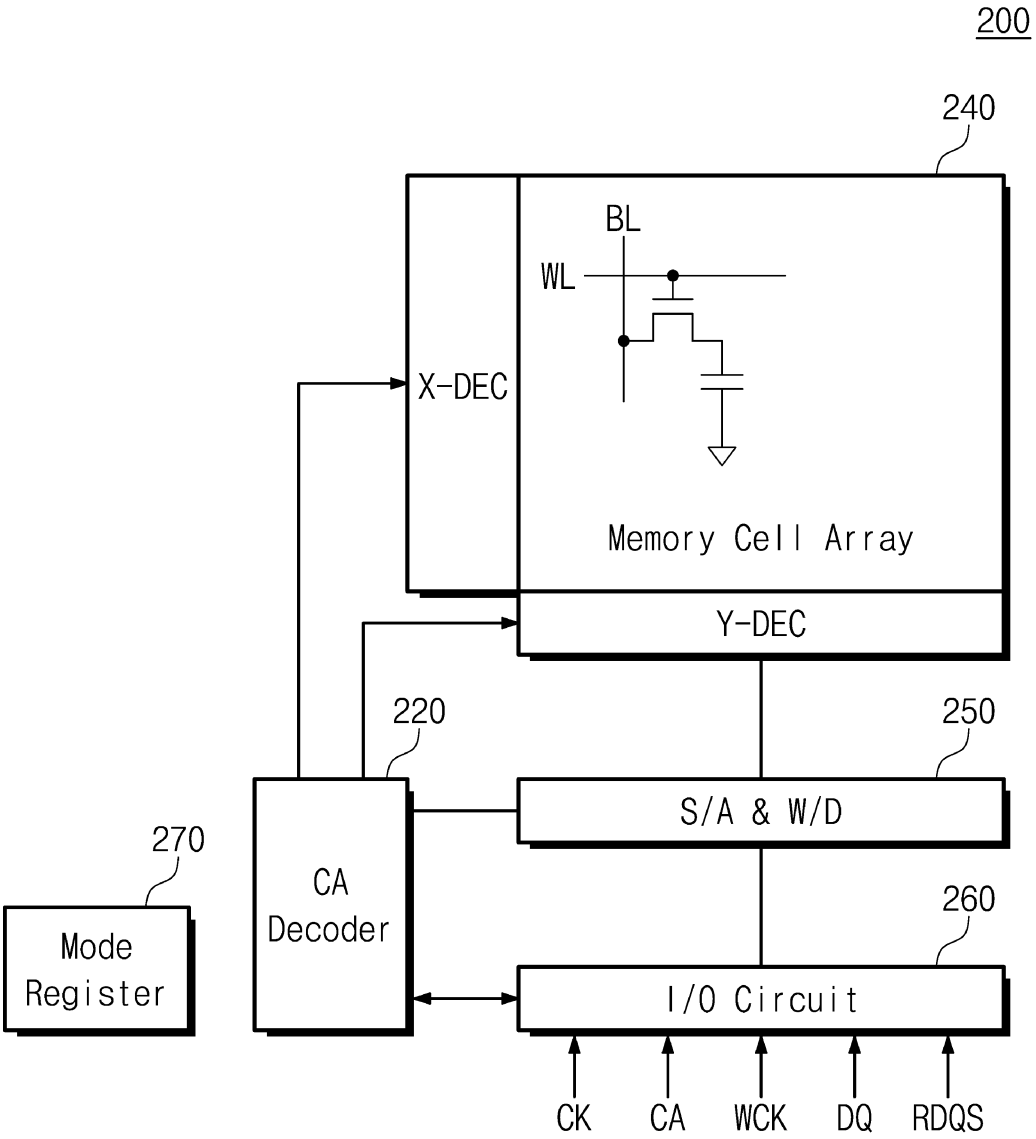

200
240
BL
WL
X-DEC
Memory Cell Array
Y-DEC
220
250
S/A & W/D
270
CA
Decoder
260
Mode
Register
I/O Circuit
CK
CA
WCK
DQ
RDQS

FIG. 4A

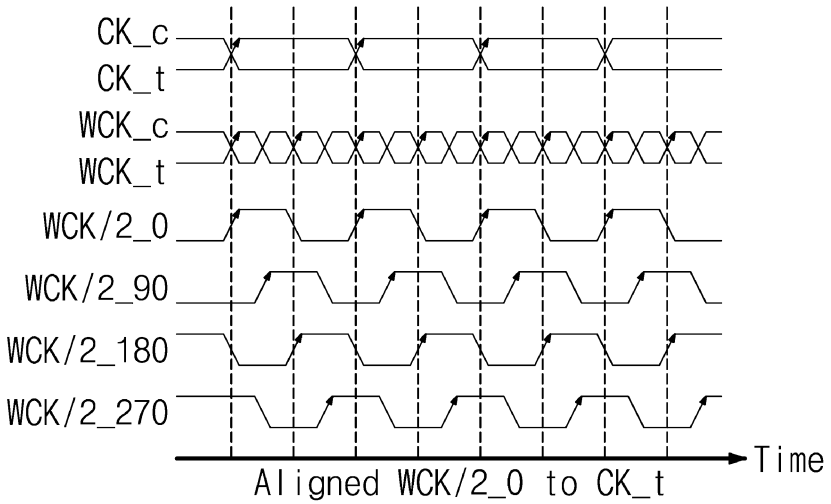

CK_c
CK_t
WCK_c
WCK_t
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
Time
Aligned WCK/2_0 to CK_t

FIG. 4B

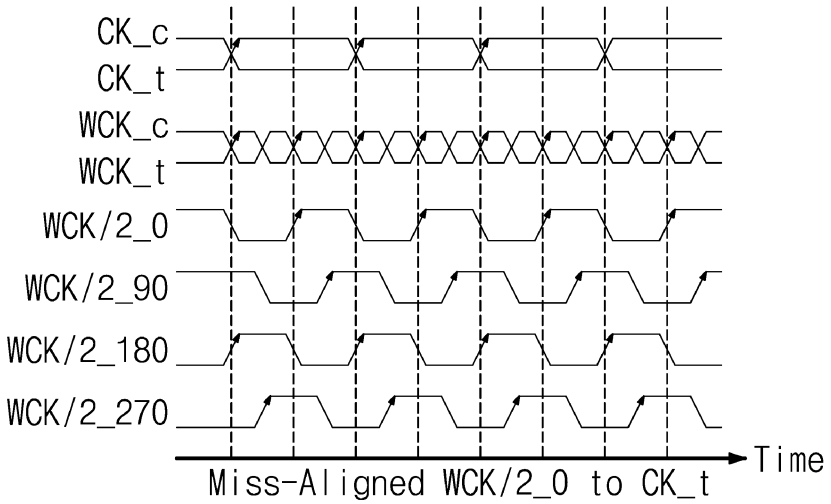

CK_c
CK_t
WCK_c
WCK_t
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
Time
Miss-Aligned WCK/2_0 to CK_t

FIG. 5

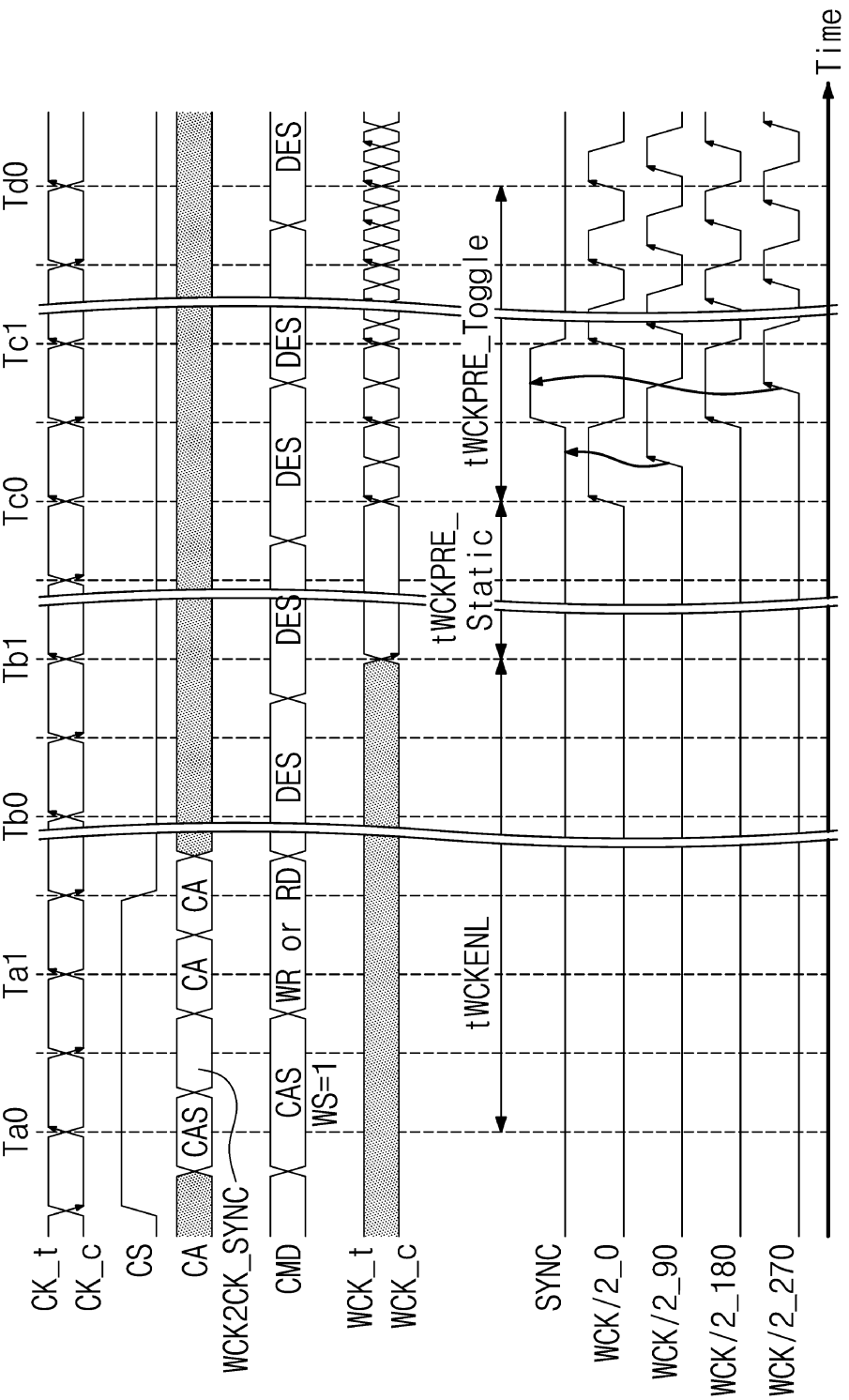

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
Td0
Time
CK_t
CK_c
CS
CA
WCK2CK_SYNC
CMD
WCK_t
WCK_c
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
CAS
CA
WR or RD
DES
WS=1
tWCKENL
tWCKPRE_Static
tWCKPRE_Toggle

FIG. 6

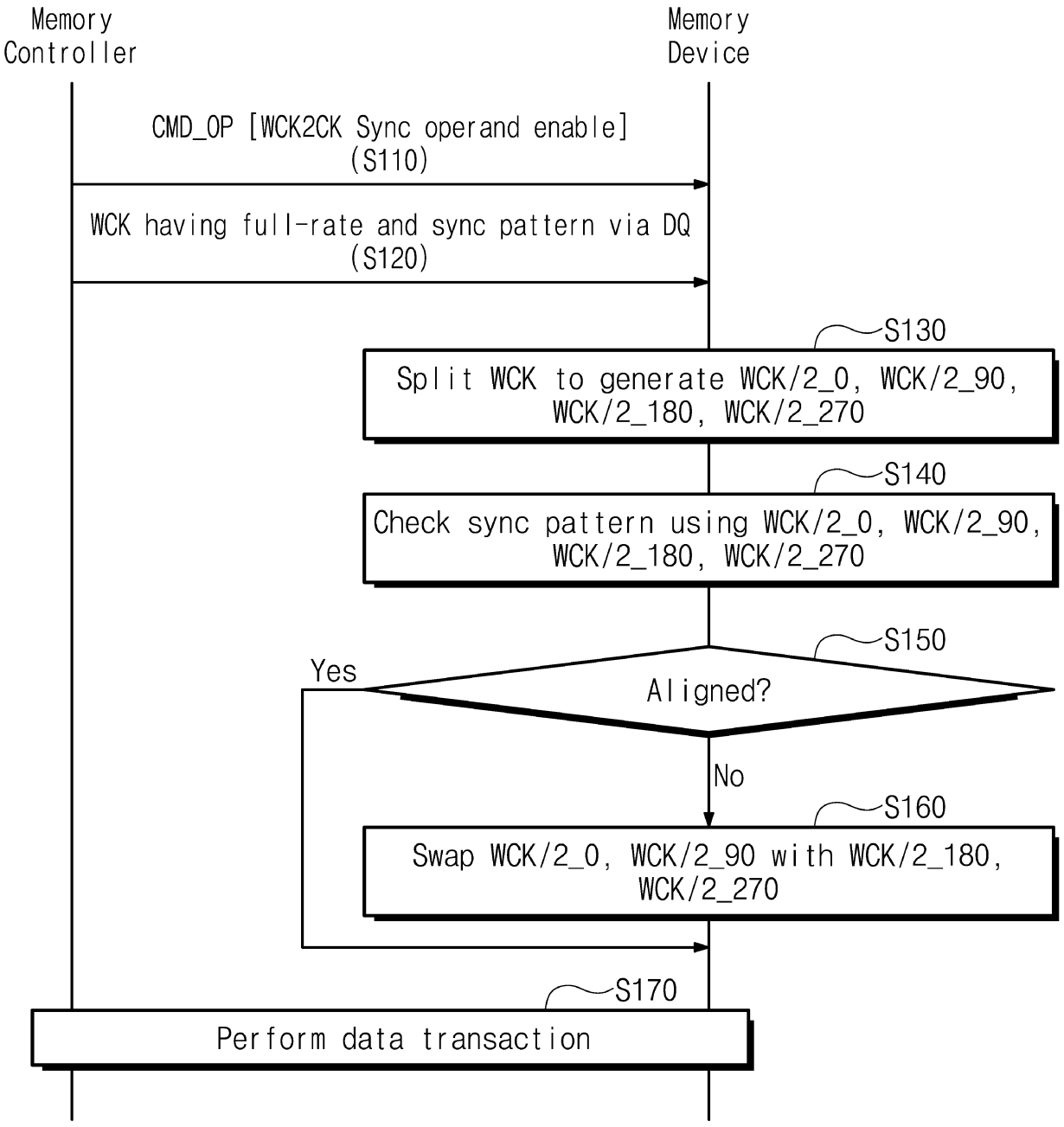

Memory Controller
Memory Device
CMD_OP [WCK2CK Sync operand enable] (S110)
WCK having full-rate and sync pattern via DQ (S120)
S130
Split WCK to generate WCK/2_0, WCK/2_90, WCK/2_180, WCK/2_270
S140
Check sync pattern using WCK/2_0, WCK/2_90, WCK/2_180, WCK/2_270
S150
Aligned?
Yes
No
S160
Swap WCK/2_0, WCK/2_90 with WCK/2_180, WCK/2_270
S170
Perform data transaction

FIG. 7

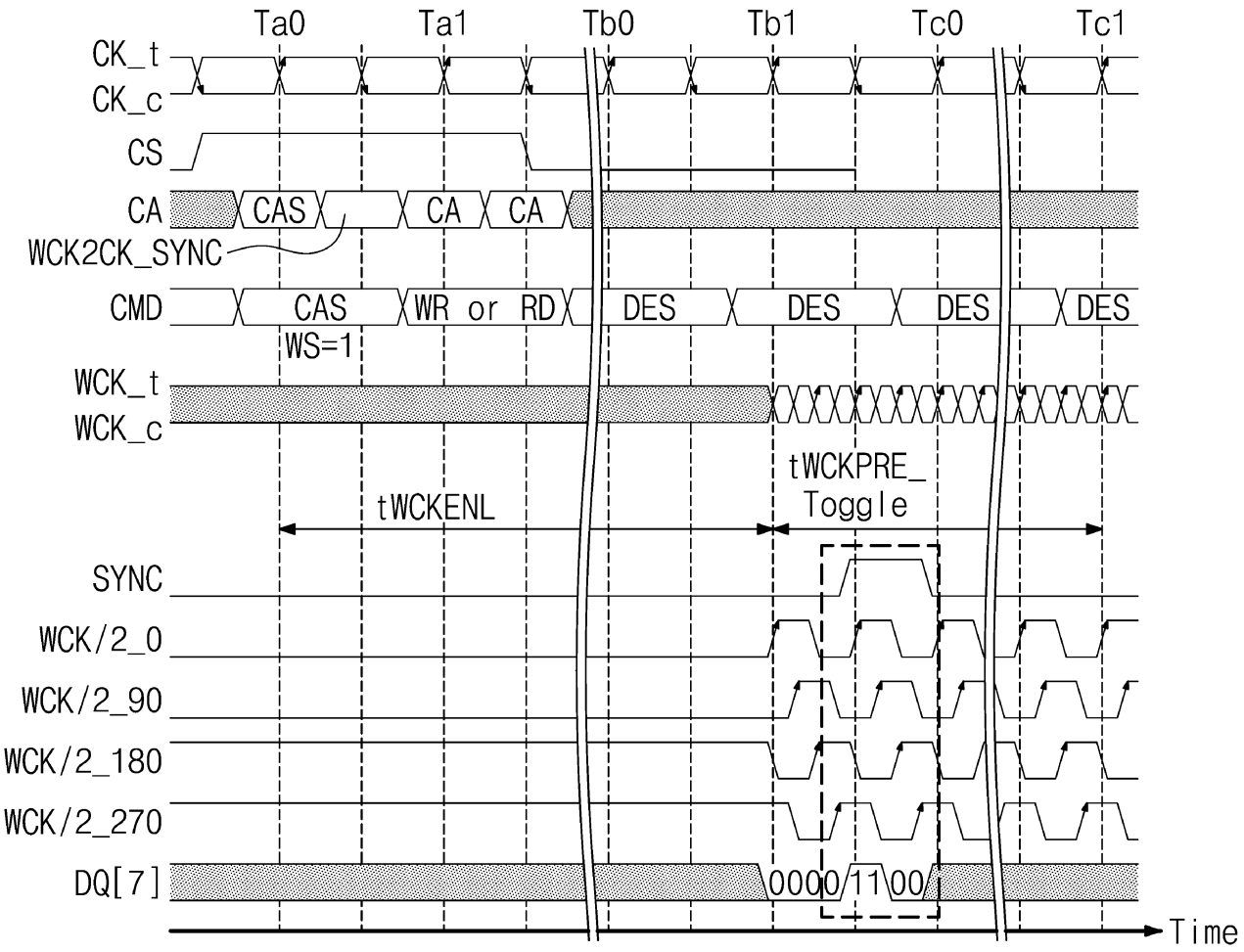

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
CK_t
CK_c
CS
CA
CAS
CA
CA
WCK2CK_SYNC
CMD
CAS
WR or RD
DES
DES
DES
DES
WS=1
WCK_t
WCK_c
tWCKENL
tWCKPRE_
Toggle
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
0000/1100/
Time

FIG. 8

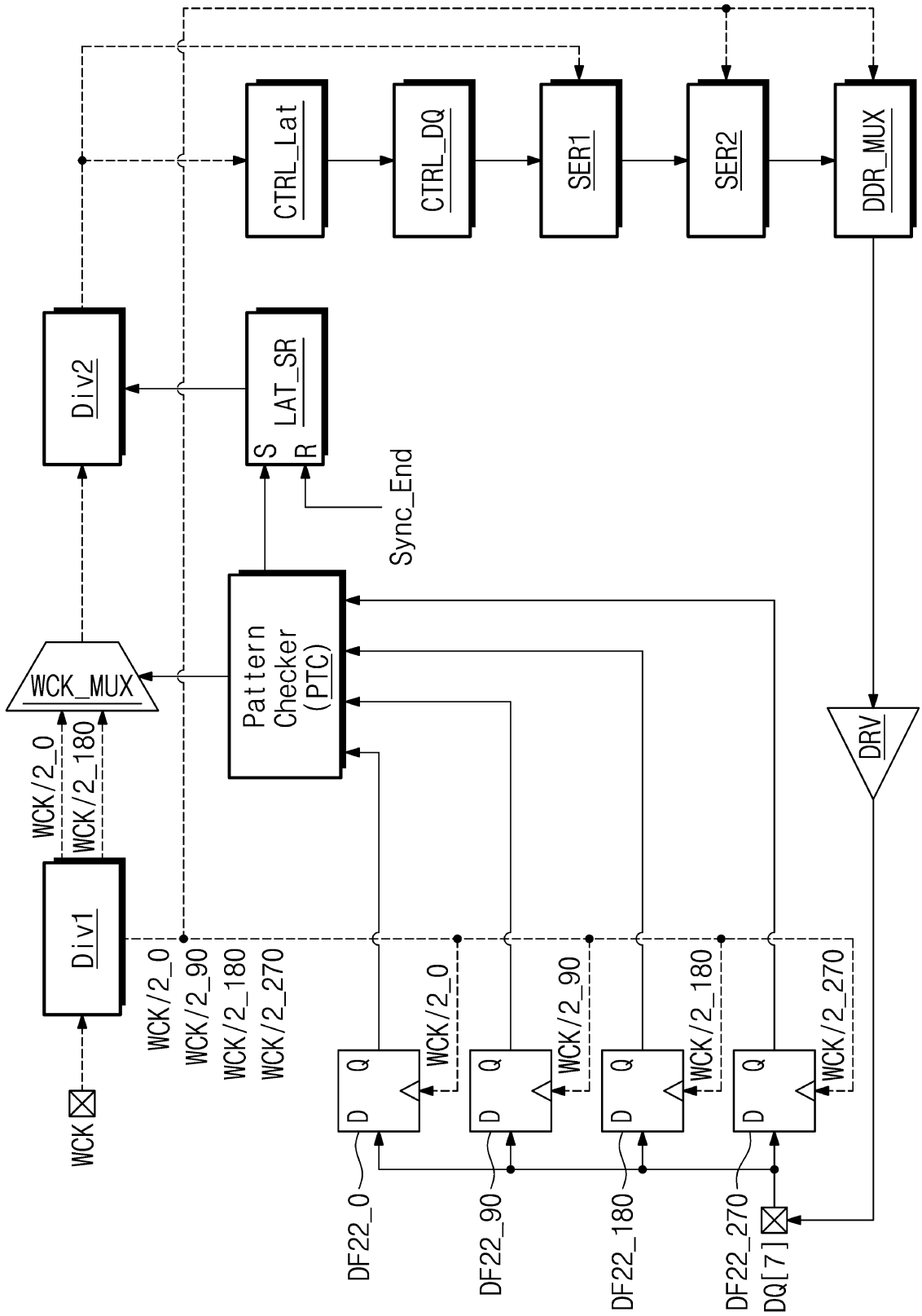

WCK
Div1
WCK/2_0
WCK/2_180
WCK_MUX
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
Div2
LAT_SR
S
R
Sync_End
Pattern Checker (PTC)
CTRL_Lat
CTRL_DQ
SER1
SER2
DDR_MUX
DRV
D Q
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DF22_0
DF22_90
DF22_180
DF22_270
DQ[7]

FIG. 9

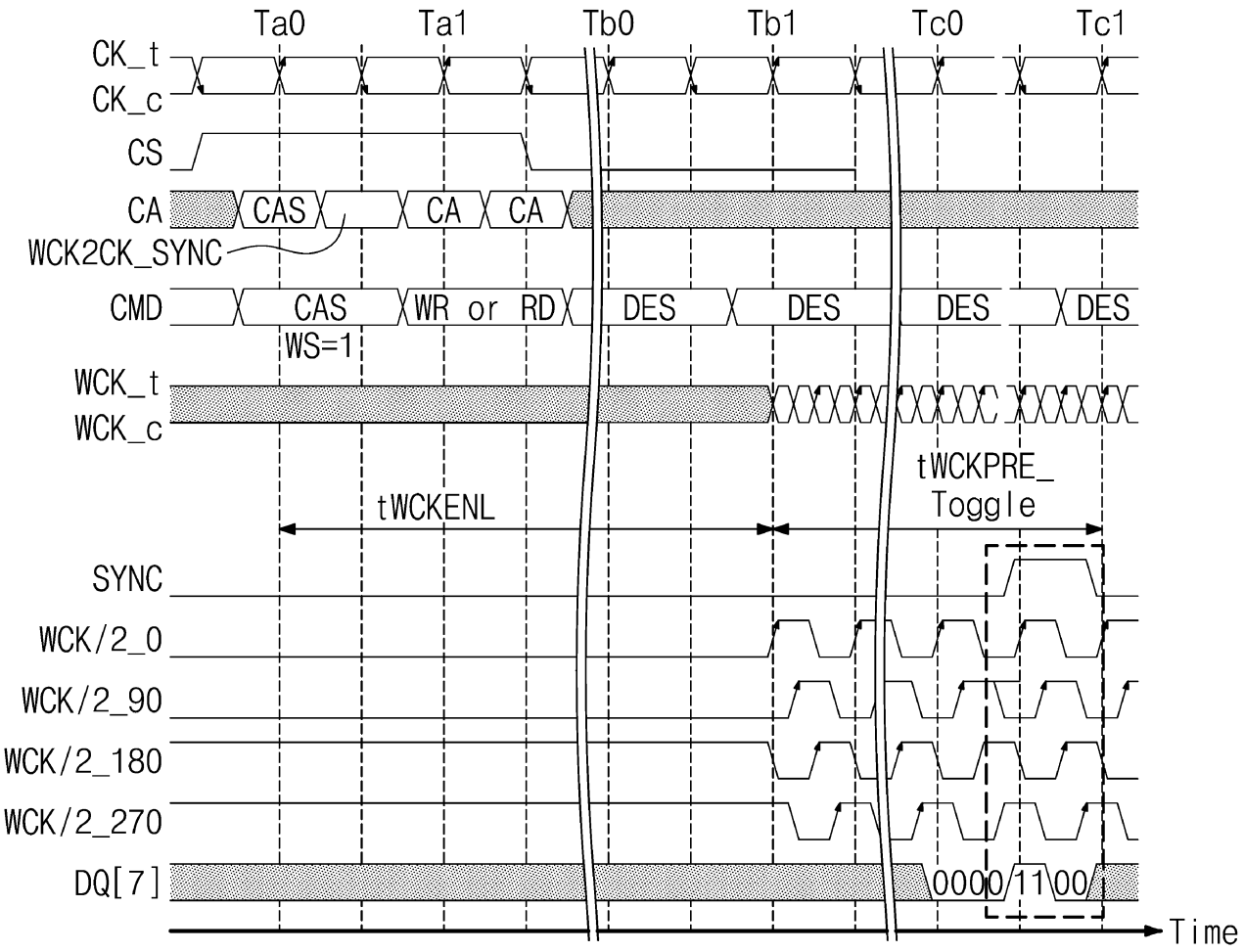

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
CK_t
CK_c
CS
CA
CAS
CA
CA
WCK2CK_SYNC
CMD
CAS
WR or RD
DES
DES
DES
DES
WS=1
WCK_t
WCK_c
tWCKENL
tWCKPRE_
Toggle
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
0000/1100
Time

FIG. 10

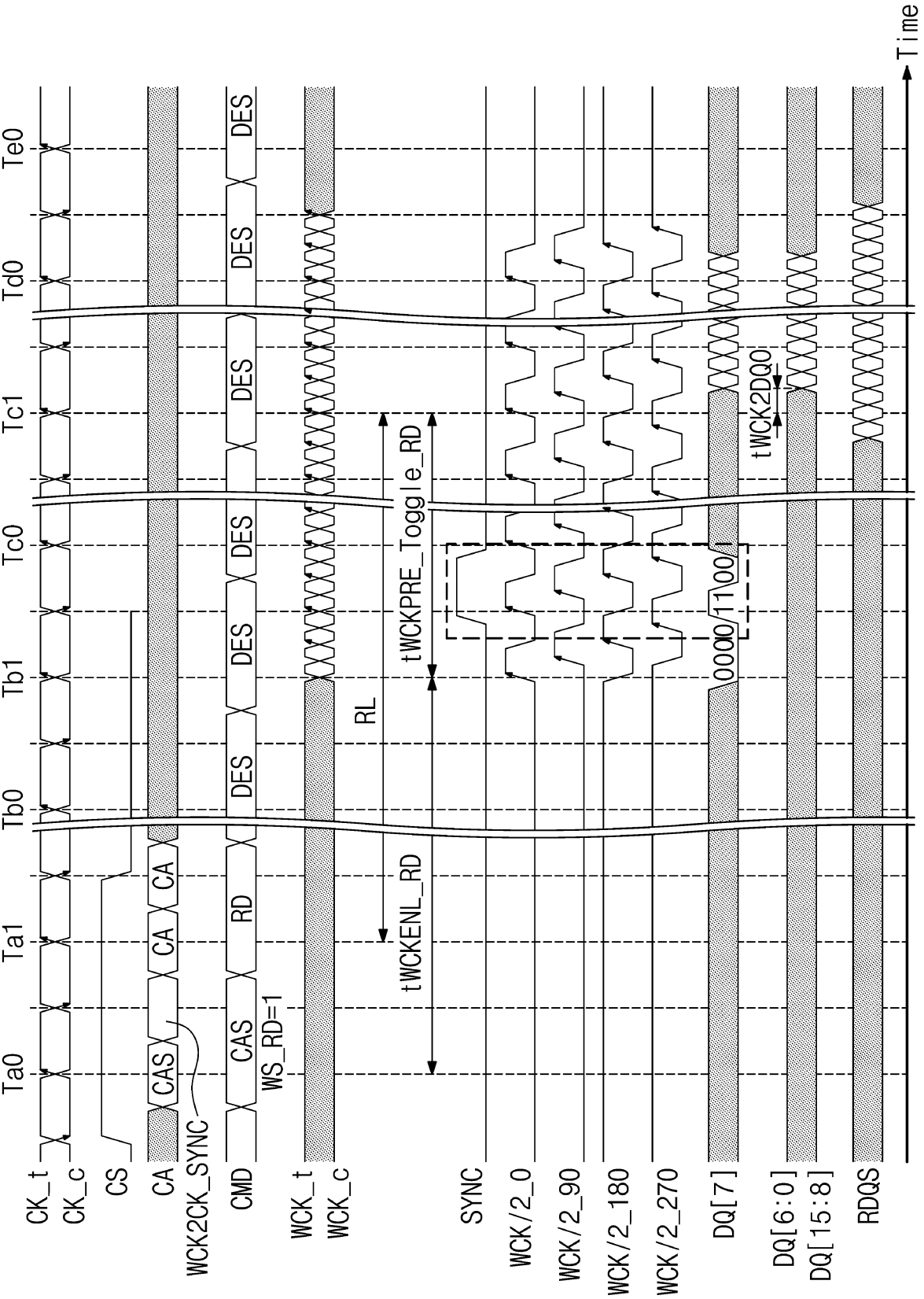

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
Td0
Te0
CK_t
CK_c
CS
CA
WCK2CK_SYNC
CMD
WCK_t
WCK_c
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
DQ[6:0]
DQ[15:8]
RDQS
CAS
CA
RD
DES
WS_RD=1
RL
tWCKENL_RD
tWCKPRE_Toggle_RD
tWCK2DQO
0000/1100
Time

FIG. 11

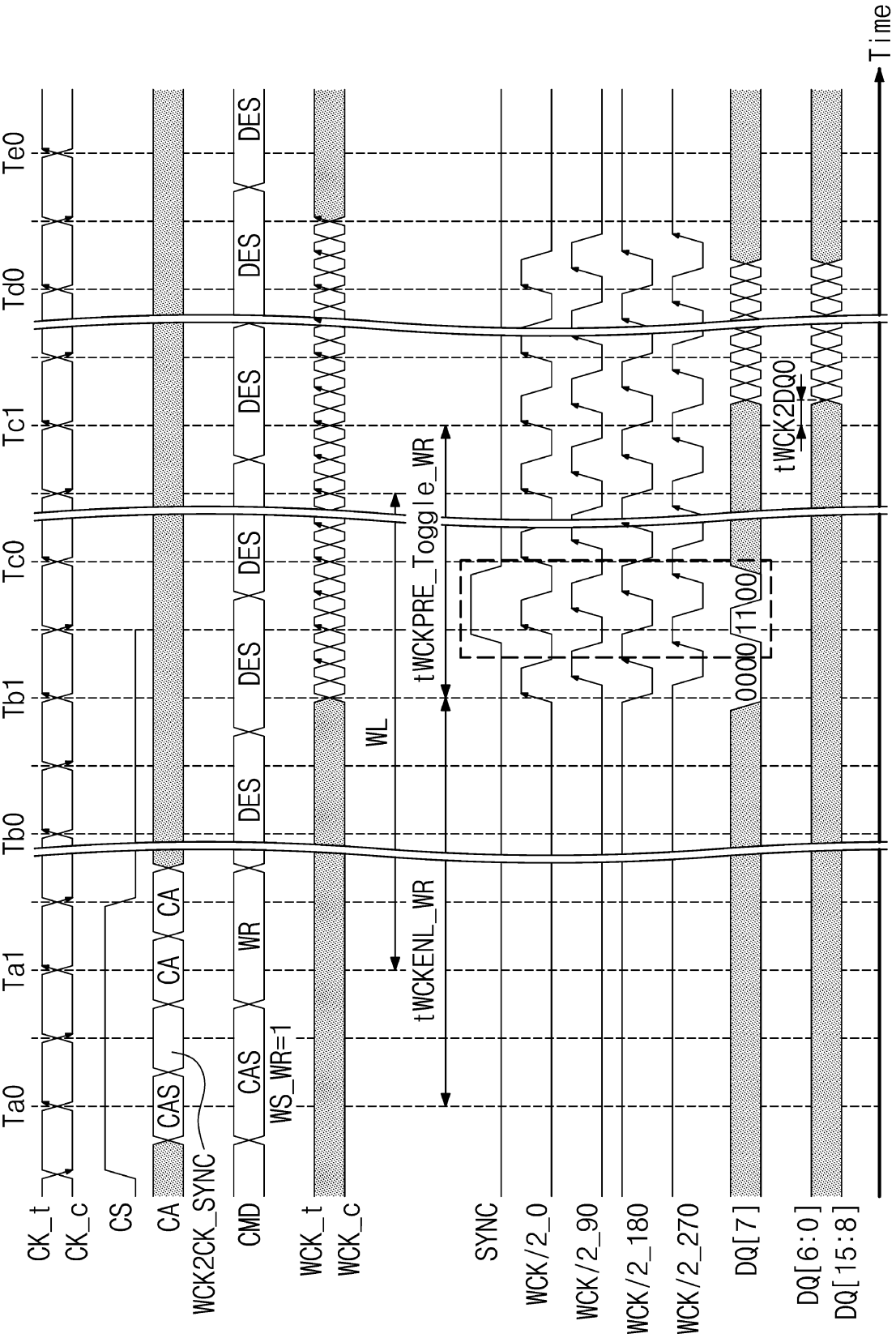

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
Td0
Te0
CK_t
CK_c
CS
CA
WCK2CK_SYNC
CMD
WCK_t
WCK_c
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
DQ[6:0]
DQ[15:8]
CAS
CA
WR
DES
WS_WR=1
WL
tWCKENL_WR
tWCKPRE_Toggle_WR
tWCK2DQO
0000/1100
Time

FIG. 12

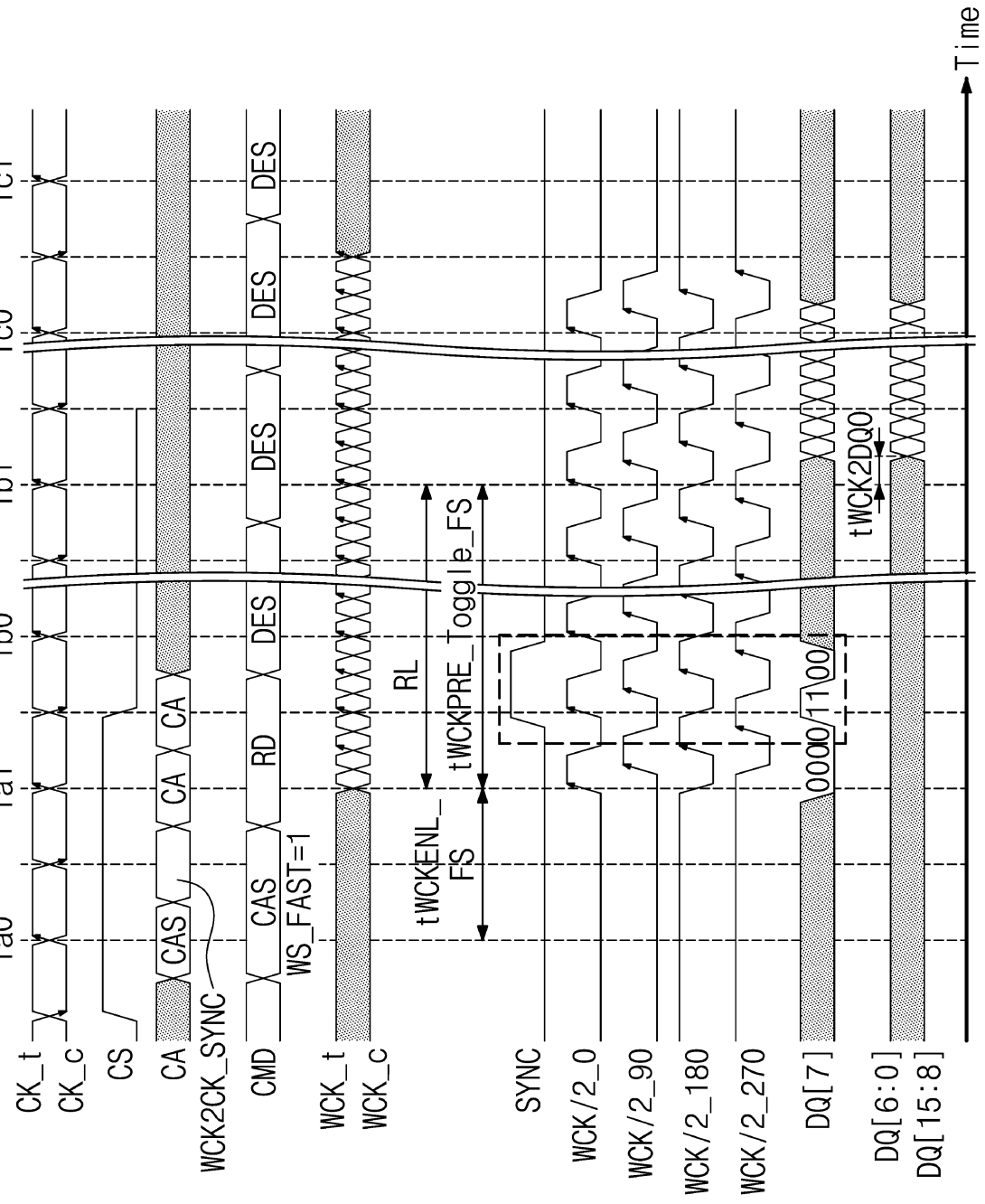

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
CK_t
CK_c
CS
CA
WCK2CK_SYNC
CMD
WCK_t
WCK_c
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
DQ[6:0]
DQ[15:8]
CAS
CA
RD
DES
WS_FAST=1
RL
tWCKENL_FS
tWCKPRE_Toggle_FS
0000/1100
tWCK2DQO
Time

FIG. 13

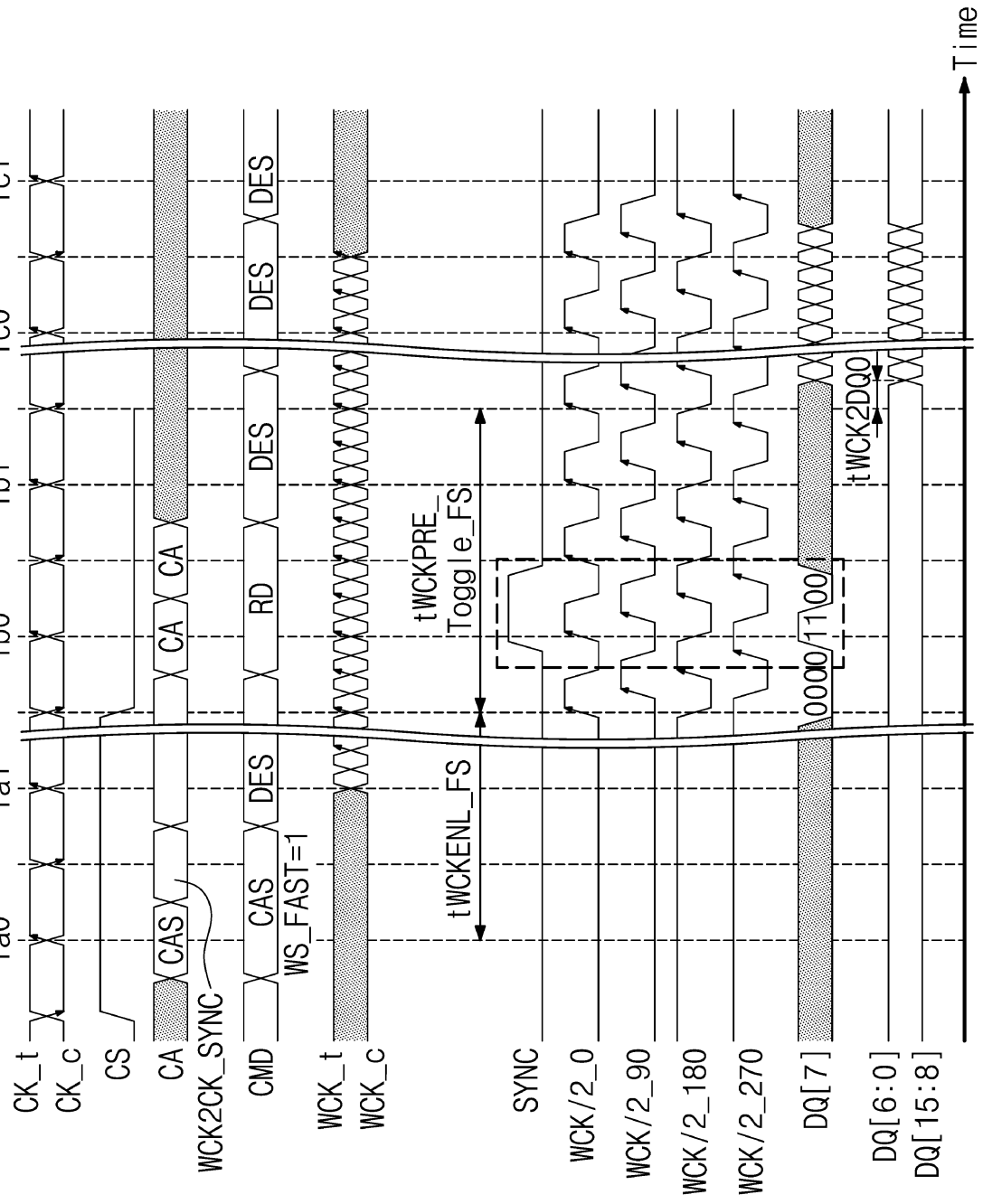

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
CK_t
CK_c
CS
CA
WCK2CK_SYNC
CMD
WCK_t
WCK_c
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
DQ[6:0]
DQ[15:8]
CAS
CA
RD
DES
WS_FAST=1
tWCKENL_FS
tWCKPRE_Toggle_FS
tWCK2DQO
0000/1100
Time

FIG. 14

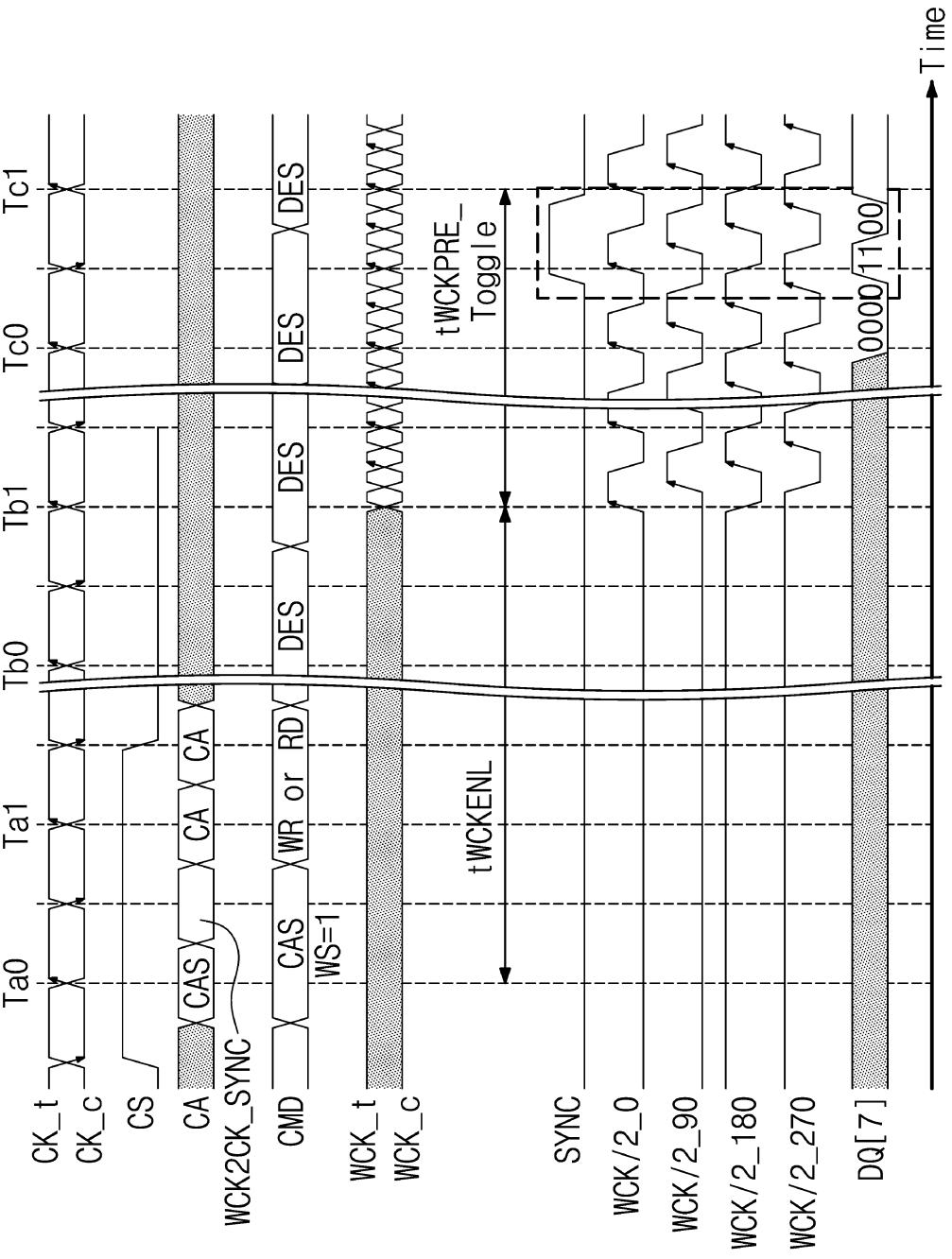

Ta0
Ta1
Tb0
Tb1
Tc0
Tc1
CK_t
CK_c
CS
CA
WCK2CK_SYNC
CMD
WCK_t
WCK_c
SYNC
WCK/2_0
WCK/2_90
WCK/2_180
WCK/2_270
DQ[7]
CAS
CA
WR or RD
DES
WS=1
tWCKENL
tWCKPRE_Toggle
0000/1100
Time

FIG. 15

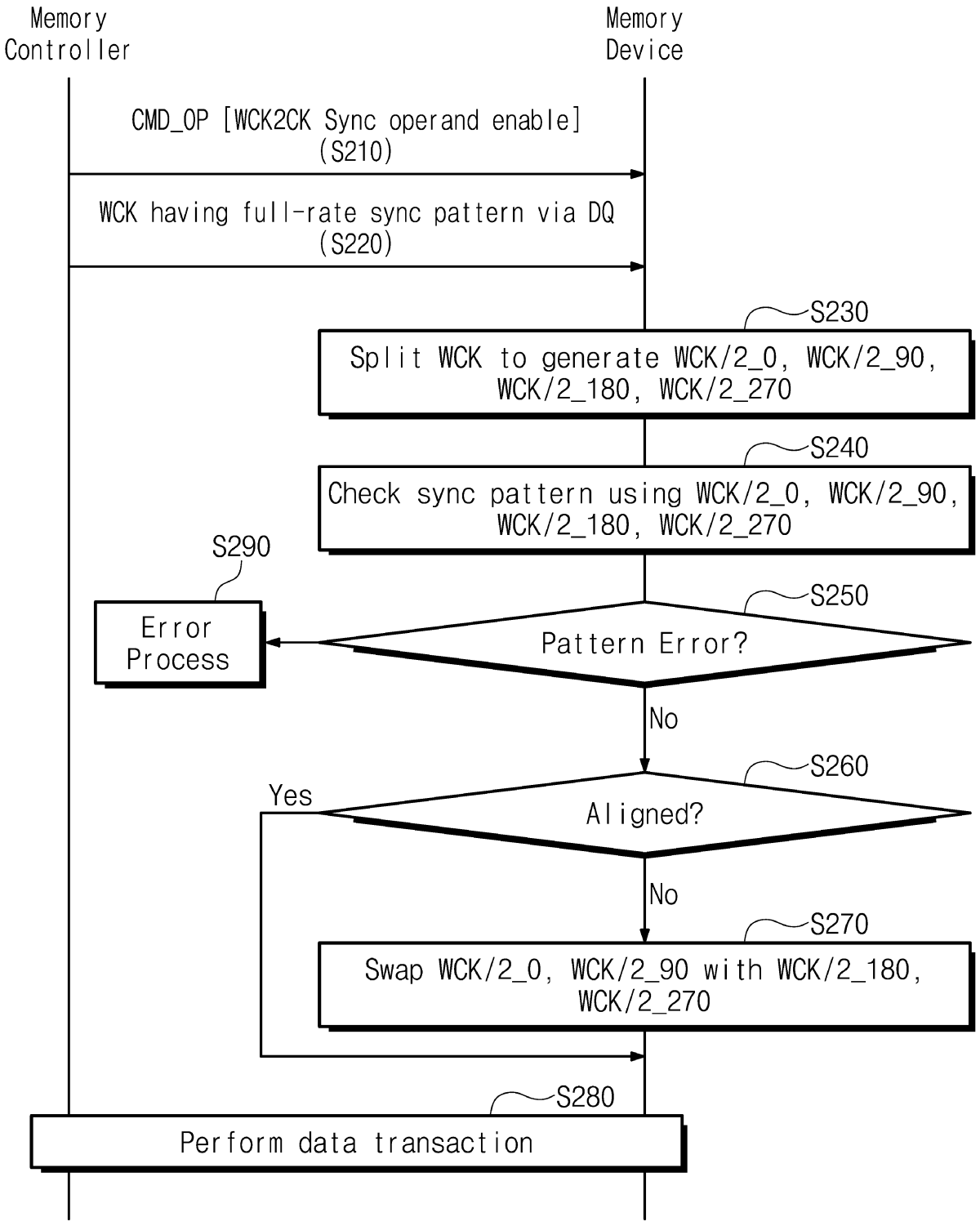

Memory Controller
Memory Device
CMD_OP [WCK2CK Sync operand enable] (S210)
WCK having full-rate sync pattern via DQ (S220)
S230
Split WCK to generate WCK/2_0, WCK/2_90, WCK/2_180, WCK/2_270
S240
Check sync pattern using WCK/2_0, WCK/2_90, WCK/2_180, WCK/2_270
S290
Error Process
S250
Pattern Error?
No
S260
Yes
Aligned?
No
S270
Swap WCK/2_0, WCK/2_90 with WCK/2_180, WCK/2_270
S280
Perform data transaction

FIG. 16

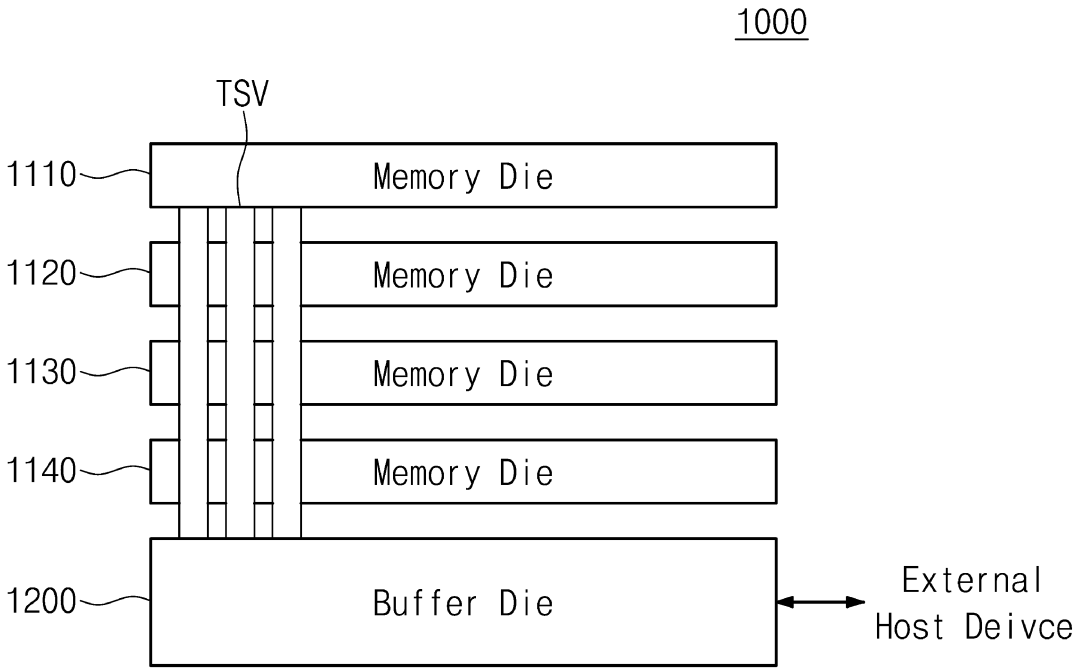

1000
TSV
1110
Memory Die
1120
Memory Die
1130
Memory Die
1140
Memory Die
1200
Buffer Die
External
Host Deivce

FIG. 17

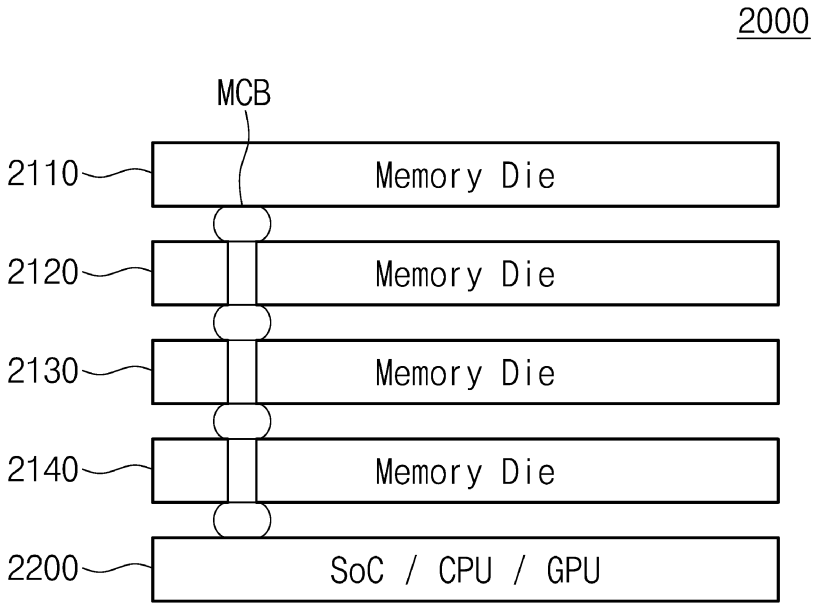

2000
MCB
2110
Memory Die
2120
Memory Die
2130
Memory Die
2140
Memory Die
2200
SoC / CPU / GPU

FIG. 18

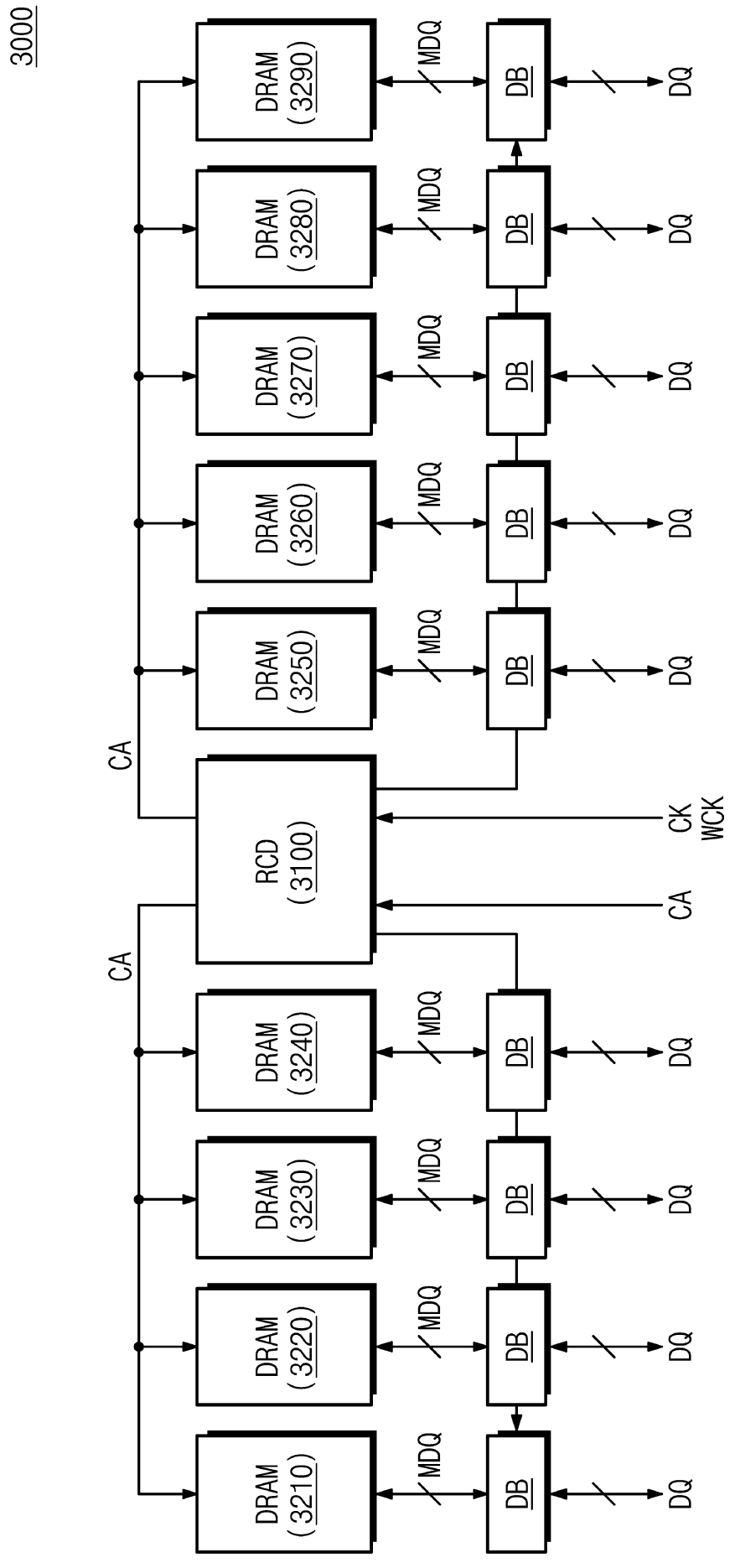
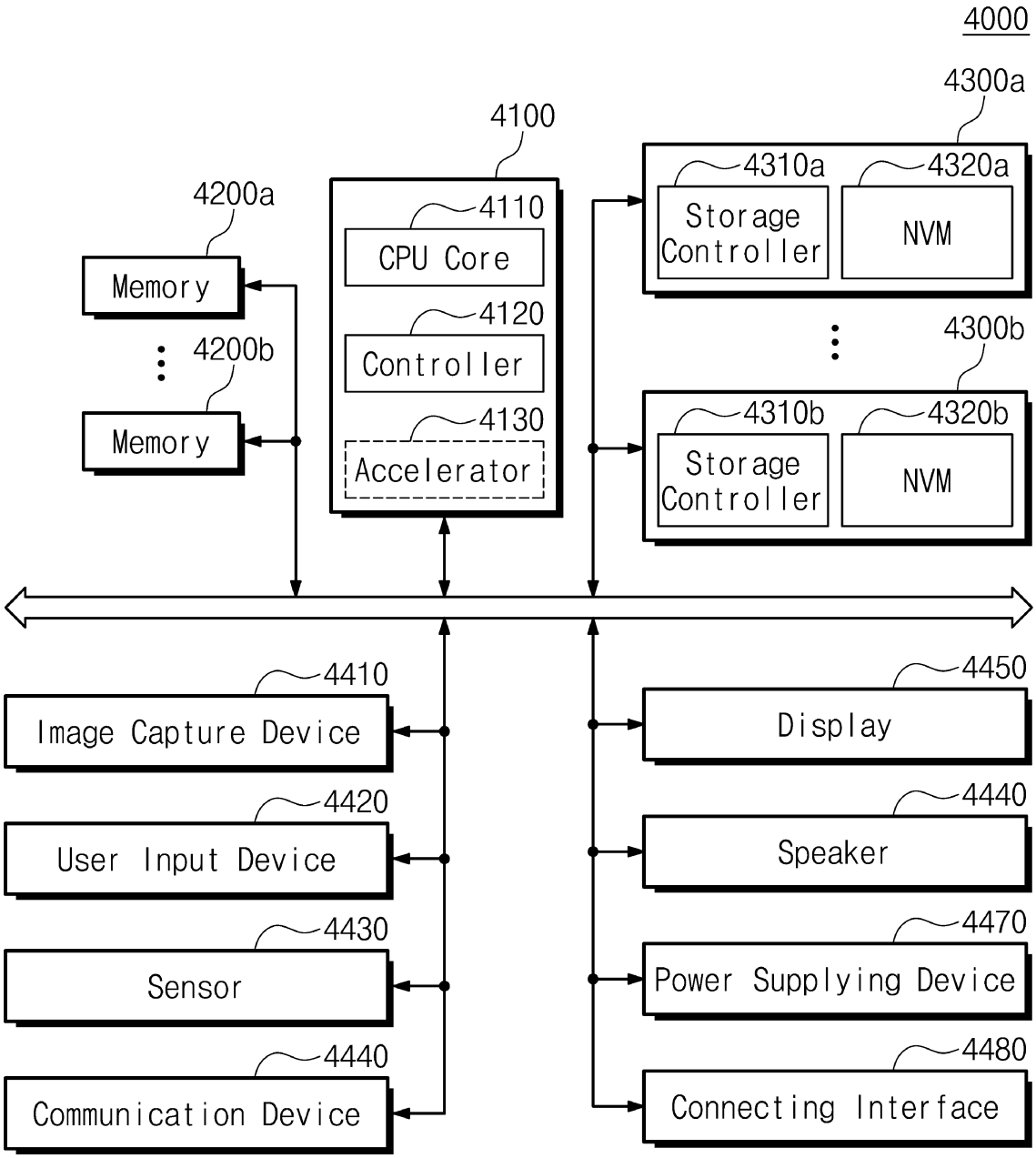

3000
RCD (3100)
CA
CA
CK
WCK
CA
DRAM (3210)
DRAM (3220)
DRAM (3230)
DRAM (3240)
DRAM (3250)
DRAM (3260)
DRAM (3270)
DRAM (3280)
DRAM (3290)
MDQ
DB
DQ

FIG. 19


4000
4300a
4100
4310a
4320a
4200a
Storage Controller
NVM
4110
CPU Core
Memory
4120
Controller
4200b
4300b
Memory
4130
4310b
4320b
Accelerator
Storage Controller
NVM
4410
4450
Image Capture Device
Display
4420
4440
User Input Device
Speaker
4430
4470
Sensor
Power Supplying Device
4440
4480
Communication Device
Connecting Interface