

DESCRIPTION

TITLE OF INVENTION: METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE, AND MEMORY DEVICE

TECHNICAL FIELD

[0001] The present disclosure relates to the field of semiconductor technology, and in particular to a method for manufacturing a semiconductor device, a semiconductor device, and a memory device.

BACKGROUND

[0002] With the development of semiconductor processes, the dimensions of devices become increasingly smaller, and the manufacturing difficulty increases correspondingly.

[0003] For semiconductor devices based on a floating gate structure, the filling of a control gate requires complete filling of gaps between floating gates. However, during the manufacturing process of semiconductor devices, the filling between floating gates is often incomplete (a void may occur), which may cause device reliability issues.

SUMMARY OF THE DISCLOSURE

[0004] A technical problem addressed by some embodiments of the present disclosure is to provide a method for manufacturing a semiconductor device, a semiconductor device, and a memory device, which may reduce a void generated in a control gate during the filling process and improve the yield of the manufactured semiconductor device.

[0005] To address the above technical problem, a technical solution adopted by the present disclosure may provide a method for manufacturing a semiconductor device. The method may include: forming shallow trench isolation structures in a substrate, where each shallow trench isolation structure has a protruding portion protruding from a surface of the substrate and first trenches are defined between the adjacent protruding portions of the shallow trench isolation structures; forming floating gates in the first trenches and performing a first etching

on a part of the protruding portions of the shallow trench isolation structures, where second trenches are formed between the adjacent floating gates; performing a narrowing process on the floating gates; performing a second etching on a remaining part of the protruding portions of the shallow trench isolation structures to widen the second trenches; and forming a control gate, where the control gate is partially filled in the second trenches.

[0006] In some embodiments, before forming the control gate, the method may further include: etching a dielectric layer on the floating gates.

[0007] In some embodiments, before forming the control gate, the method may further include: growing a dielectric layer on the floating gates.

[0008] In some embodiments, the dielectric layer may further include a first oxide layer, a first nitride layer, and a second oxide layer. The growing a dielectric layer on the floating gates may include: growing the first oxide layer on the floating gates; growing the first nitride layer on the first oxide layer; and growing the second oxide layer on the first nitride layer.

[0009] In some embodiments, a part of the dielectric layer may be disposed on sidewalls of the floating gates, forming sidewalls of the second trenches.

[0010] In some embodiments, the forming floating gates in first trenches may include: forming a polysilicon layer in the first trenches; and etching the polysilicon layer to form the floating gates, wherein an upper surface of the floating gates is higher than or flush with an upper surface of the shallow trench isolation structures.

[0011] In some embodiments, sidewalls of the second trench may be formed by opposing sidewalls between the adjacent floating gates. Each of the floating gates may include a first sidewall and a second sidewall. The first sidewall may be connected to a bottom of the second trench. The second sidewall may be connected to the first sidewall. An included angle between the first sidewall and the bottom of the second trench may be less than or equal to 90 degrees. An included angle between the second sidewall and the bottom of the second trench may be greater than 90 degrees.

[0012] In some embodiments, a cross-sectional area of the control gate located at a bottom of the second trenches may be smaller than a cross-sectional area of the control gate located at an opening of the second trenches.

[0013] To address the above technical problem, another technical solution adopted by the

present disclosure may provide a semiconductor device. The semiconductor device may be obtained through the manufacturing method provided by the above technical solution.

[0014] To address the above technical problem, another technical solution adopted by the present disclosure may provide a memory device. The memory device may include a semiconductor memory device. The semiconductor device may be the semiconductor device mentioned above or may be a semiconductor device obtained through the manufacturing method mentioned above.

[0015] Some technical effects of the present disclosure may be as follows. Different from the related art, some embodiments of the present disclosure may provide a method for manufacturing a semiconductor device, a semiconductor device, and a memory device. During a manufacturing process of a semiconductor device, in a case where the floating gates are manufactured but a filling of a control gate has not yet been started, only a part of protruding portions of shallow trench isolation structures may be etched to partially expose the floating gates. Then, a narrowing process may be performed on the floating gates so that an entire opening of the second trenches may be enlarged. Subsequently, after further etching the protruding portions of the shallow trench isolation structures, a void depth of each second trench may be reduced and an aspect ratio may be lowered. In this way, the filling of the control gate may become easier, which further reduces voids generated during the filling process of the control gate, thereby improving the yield of the manufactured semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] In order to more clearly illustrate the technical solutions in some embodiments of the present disclosure, a brief introduction will be given below to the drawings required in the description of the embodiments. It is evident that the drawings described below are merely some embodiments of the present disclosure, and those skilled in the art may obtain other drawings based on the following drawings without creative work.

[0017] FIG. 1 is a flowchart of an embodiment of a method for manufacturing a semiconductor device according to the present disclosure.

[0018] FIG. 2-10 are schematic structural views illustrating a process corresponding to the

method for manufacturing the semiconductor memory structure in FIG. 1.

[0019] FIG. 11 is a partial enlarged view of a second trench C shown in FIG. 9.

[0020] FIG. 12 is a flowchart of another embodiment of the method for manufacturing a semiconductor device according to the present disclosure.

[0021] FIG. 13-14 are schematic structural views illustrating another process corresponding to the method for manufacturing a semiconductor device according to present disclosure.

[0022] FIG. 15 is a schematic circuit view of the semiconductor device.

DETAILED DESCRIPTION

[0023] The technical solutions in some embodiments of the present disclosure may be described clearly and completely below with reference to the accompanying drawings in the embodiments of the present disclosure. Obviously, the described embodiments are only a part of the embodiments of the present disclosure, not all of them. Based on the embodiments of the present disclosure, all other embodiments obtained by those skills in the art without creative effort shall fall within the scope of protection of the present disclosure.

[0024] It is worth noting that directional terms such as “upper,” “lower,” and “side” may be used herein to describe the interlayer structure of the semiconductor, based on the condition that a deposition plane of the semiconductor structure is located in a horizontal plane. The corresponding “height” and “depth” are described based on a vertical direction. The corresponding “width” is described based on a horizontal direction. In a case where an overall position of the semiconductor structure changes (e.g., rotation), the corresponding directional descriptions may vary, but structural characteristics identical to those in the present disclosure should also fall within the scope of protection of the present disclosure.

[0025] With the development of semiconductor processes, the dimensions of devices become increasingly smaller, and the manufacturing difficulty increases correspondingly.

[0026] For semiconductor devices based on a floating gate structure, the filling of a control gate requires complete filling of gaps between floating gates. However, during the manufacturing process of semiconductor devices, the filling between floating gates is often incomplete (a void may occur), which may cause device reliability issues.

[0027] In view of the above, according to some embodiments of the present disclosure,

during a manufacturing process of a semiconductor device, in a case where the floating gates are manufactured but a filling of a control gate has not yet been started, only a part of protruding portions of shallow trench isolation structures may be etched to partially expose the floating gates. Then, a narrowing process may be performed on the floating gates so that an entire opening of the second trenches may be enlarged. Subsequently, after further etching the protruding portions of the shallow trench isolation structures, a void depth of each second trench may be reduced and an aspect ratio may be lowered. In this way, the filling of the control gate may become easier, which further reduces voids generated during the filling process of the control gate, thereby improving the yield of the manufactured semiconductor device.

[0028] As shown in FIG. 1, FIG. 1 is a flowchart of an embodiment of a method for manufacturing a semiconductor device according to the present disclosure. The method may include the following operations.

[0029] At operation 11: forming shallow trench isolation structures in a substrate.

[0030] In some embodiments, the substrate may be made of a semiconductor material, such as a silicon substrate, a germanium substrate, a silicon-germanium substrate, or a group III–V compound substrate. It may be understood that the substrate is generally of a plate-like material. An area of the substrate may be determined according to an area of a memory array to be manufactured. Typically, multiple sub-memory arrays may be formed from one substrate through a dicing process. Each sub-memory array may be further processed to form a memory chip.

[0031] An oxide layer 200 and a silicon nitride layer 300 may be sequentially formed on the substrate 100, as shown in FIG. 2.

[0032] In some embodiments, the oxide layer 200 may be an oxide of silicon, such as silicon dioxide.

[0033] The formation of the oxide layer 200 or the silicon nitride layer 300 on the substrate 100 may be performed by using physical vapor deposition (PVD) or chemical vapor deposition (CVD). The PVD refers to a process in which, under a vacuum condition, a surface of material source (solid or liquid) may be vaporized into gaseous atoms or molecules, or partially ionized into ions, and deposited onto a surface of the substrate through

a low-pressure gas (or plasma) process to form a thin film with a specific function. The PVD coating technology may mainly include three types: vacuum evaporation coating, vacuum sputtering coating, and vacuum ion plating. The CVD refers to a method in which chemical gases or vapors may react on the surface of the substrate to synthesize a coating or a nanomaterial, which is one of the most widely used techniques in the semiconductor industry for depositing various materials, including a wide range of insulating materials, most metallic materials, and metallic alloy materials.

[0034] Taking the CVD as an example, two or more gaseous raw materials may be introduced into a reaction chamber, where they may chemically react with each other to form a new material that may be deposited on the surface of the substrate. The deposition of silicon nitride (Si_3N_4) may be one example, which may be formed by the reaction of silane and nitrogen.

[0035] In some embodiments, a deposition thickness of the oxide layer may be 50Å to 200Å and a deposition thickness of the nitride layer may be 500Å to 2000Å.

[0036] Using a hard mask layer as a mask, a plurality of shallow trenches A may be formed or defined in the substrate 100. The silicon nitride layer 300 may form a silicon nitride structure 30a, as shown in FIG. 3.

[0037] The formation of trenches in a material may generally be performed through an etching process. Etching is an important operation in a semiconductor manufacturing process, a microelectronics integrated circuit (IC) manufacturing process, and a micro/nano manufacturing process. The etching may first involve photolithographically exposing and developing a photoresist, followed by selectively removing unwanted portions through chemical or physical processes. The etching may be a process in which unwanted materials are selectively removed from a surface of a silicon wafer by chemical or physical means, with a basic objective of accurately replicating a mask pattern on the coated silicon wafer.

[0038] The shallow trench isolation structures 400 may then be formed in the plurality of shallow trenches A. The silicon nitride structure 30a may be further removed to form first trenches B, as shown in FIG. 4. That is, each shallow trench isolation structure 400 may have a protruding portion protruding from the surface of the substrate 100. The first trenches B may be defined between the adjacent protruding portions of the shallow trench isolation

structures 400.

[0039] At operation 12: forming floating gates in first trenches and performing a first etching on a part of protruding portions of the shallow trench isolation structures. The second trenches may be formed between adjacent floating gates.

[0040] The floating gates 500 may be formed in the first trenches B, as shown in FIG. 5.

[0041] In some embodiments, a polysilicon layer may be formed in the first trenches B. The polysilicon layer may be etched to form the floating gates 500. An upper surface of the floating gates 500 may be higher than or flush with an upper surface of the shallow trench isolation structures 400.

[0042] In some other embodiments, the floating gates 500 may be formed in the first trenches B, as shown in FIG. 6.

[0043] In some embodiments, the polysilicon layer may be formed in the first trenches B. The polysilicon layer may be etched to form the floating gates 500. The upper surface of the floating gates 500 may be higher than the upper surface of the shallow trench isolation structures 400.

[0044] In some embodiments, there may be multiple methods for forming the polysilicon layer in the first trenches B, such as using a mask and a deposition process, or by combining deposition, chemical mechanical polishing (CMP), and blanket etching processes.

[0045] A polysilicon may be a crystalline form of silicon. In a case where molten silicon solidifies under a supercooled condition, silicon atoms may form numerous crystal nuclei in a diamond lattice arrangement. In a case where the crystal nuclei grow into grains with different crystal orientations, the grains after combining with each other may crystalize into the polysilicon.

[0046] In some other embodiments, a mask may be adopted to deposit the polysilicon in the first trenches B. In this case, an upper surface of the polysilicon may not be lower than the upper surface of the shallow trench isolation structures 400, with the depth not being limited. The polysilicon layer may then be etched to form the floating gates 500. The upper surface of the polysilicon may be higher than or flush with the upper surface of the shallow trench isolation structures 400. The above operation may be implemented through photolithography.

[0047] As shown in FIG. 7, in a case where the floating gates 500 are formed in the first

trenches B, the first etching may be performed on a part of the protruding portions of the shallow trench isolation structures 400. Second trenches C may be formed or defined between the adjacent floating gates 500. That is, the floating gates 500 may be partially exposed.

[0048] At operation 13: performing a narrowing process on the floating gates.

[0049] As shown in FIG. 8, in a case where the second trenches C are formed between the adjacent floating gates 500, i.e., after the floating gates 500 are exposed, the narrowing process may be performed on the floating gates 500. Since the floating gates 500 may have a three-dimensional structure, side edges of the floating gates 500 may be etched so that each floating gate may have a substantially trapezoidal shape. That is, after the narrowing process of the floating gates 500, a distance between the adjacent floating gates may increase. That is, an opening of each second trench C may be enlarged.

[0050] At operation 14: performing a second etching on a remaining part of the protruding portions of the shallow trench isolation structures to widen the second trenches.

[0051] As shown in FIG. 9, after performing the narrowing process on the floating gates 500, the second etching may be further performed on the remaining part of the protruding portions of the shallow trench isolation structures 400 to widen the second trenches C. In addition, the second trenches C may further be deepened.

[0052] During the etching process, the second trenches C may not only be deepened but may further cause a certain degree of damage to side portions of the floating gates 500, thereby serving to widen the second trenches C and making gaps between the floating gates 500 broader.

[0053] In some embodiments, the second etching of the remaining part of the protruding portions of the shallow trench isolation structures may be performed such that the upper surface of the shallow trench isolation structures 400 after etching may be flush with or lower than an upper surface of the oxide layer 200.

[0054] In some embodiments, as shown in FIG. 11, sidewalls of second trenches C may be formed by opposing sidewalls between the adjacent floating gates 500. Each floating gate may include a first sidewall 50b and a second sidewall 50a. The first sidewall 50b may be connected to a bottom of the second trench C. The second sidewall 50a may be connected to the first sidewall 50b. An included angle α between the first sidewall 50b and the bottom of

the second trench C may be less than or equal to 90 degrees. An included angle β between the second sidewall 50a and the bottom of the second trench C may be greater than 90 degrees. That is, the opening of the second trench C may gradually enlarge starting from the second sidewall 50a.

[0055] At operation 15: forming a control gate. The control gate may be partially filled in the second trenches.

[0056] As shown in FIG. 10, the control gate 600 may be formed. A part of the control gate 600 may be filled in the second trenches C. In this case, a cross-sectional area of the control gate 600 located at the bottom of the second trenches C may be smaller than a cross-sectional area of the control gate 600 located at the opening of the second trenches C.

[0057] During the manufacturing process of the semiconductor device, in a case where the floating gates 500 have been formed but the filling of the control gate 600 has not been started yet, i.e., after the floating gates 500 have been formed and before the filling of the control gate 600 is started, the protruding portions of the shallow trench isolation structures 400 may be only partially etched to expose a part of the floating gates 500. The narrowing process may be performed on the floating gates 500 so that an entire opening of the second trenches C may be enlarged. Subsequently, after further etching the protruding portions of the shallow trench isolation structures 400, a void depth of each second trench C may be reduced and an aspect ratio may be lowered. In this way, the filling of the control gate 600 may become easier, which further reduces voids generated during the filling process of the control gate 600, thereby improving the yield of the manufactured semiconductor device.

[0058] As shown in FIG. 12, FIG. 12 is a flowchart of another embodiment of the method for manufacturing a semiconductor device according to the present disclosure. The method may include the following operations.

[0059] At operation 21: forming shallow trench isolation structures in a substrate.

[0060] At operation 22: forming floating gates in first trenches and performing a first etching on a part of protruding portions of the shallow trench isolation structures. The second trenches may be formed between the adjacent floating gates.

[0061] At operation 23: performing a narrowing process on the floating gates.

[0062] At operation 24: performing a second etching on a remaining part of the protruding

portions of the shallow trench isolation structures to widen the second trenches.

[0063] The schematic manufacturing views corresponding to operations 21-24 may refer to FIGS. 2-9, which will not be repeated herein.

[0064] At operation 25: forming a dielectric layer on the floating gates.

[0065] As shown in FIG. 12, a dielectric layer 700 may be formed on the floating gates 500.

[0066] In some embodiments, the dielectric layer 700 may be an oxide layer, a nitride layer, or a stacked layer thereof. For example, the stacked layer may be formed by stacking the oxide layer and a mixed layer, which is formed by an oxide and a nitride, together

[0067] In some embodiments, the dielectric layer 700 may be etched on the floating gates 500. For example, a first oxide layer may be formed on the floating gates 500. A first nitride layer may be formed on the first oxide layer. A second oxide layer may be formed on the first nitride layer.

[0068] In some embodiments, the dielectric layer 700 may be grown on the floating gates 500. For example, a first oxide layer may be grown on the floating gates 500. A first nitride layer may be grown on the first oxide layer. A second oxide layer may be grown on the first nitride layer. That is, the dielectric layer 700 may include the first oxide layer, the first nitride layer, and the second oxide layer. The first oxide layer, the first nitride layer, and the second oxide layer may be sequentially stacked on the floating gates 500. The first oxide layer may be disposed in contact with or attached to the floating gates 500.

[0069] In a case where the dielectric layer 700 is formed on the floating gates 500, a part of the dielectric layer 700 may be disposed on the sidewalls of the floating gates, thereby forming the sidewalls of the second trenches C.

[0070] In some embodiments, the sidewalls of the second trenches C may be defined or formed by the dielectric layer 700 on opposing sidewalls between the adjacent floating gates 500. A shape of the dielectric layer 700 may be substantially consistent with shapes of the sidewalls of the floating gates 500. A part of the dielectric layer 700 may be disposed in contact with the sidewalls of the floating gates 500.

[0071] At operation 26: forming a control gate. The control gate may be partially filled in the second trenches.

[0072] As shown in FIG. 14, the control gate 600 may be formed. A part of the control gate

600 may be filled in the second trenches C. In this case, a cross-sectional area of the control gate 600 located at the bottom of each second trench C may be smaller than a cross-sectional area of the control gate 600 located at the opening of each second trench C.

[0073] In the present embodiments, during the manufacturing process of the semiconductor device, in a case where the floating gates 500 have been formed but the filling of the control gate 600 has not been started yet, the protruding portions of the shallow trench isolation structures 400 may be only partially etched to expose a part of the floating gates 500. The narrowing process may be performed on the floating gates 500 so that an entire opening of the second trenches C may be enlarged. Subsequently, after further etching the protruding portions of the shallow trench isolation structures 400, a void depth of each second trench C may be reduced and an aspect ratio may be lowered. In this way, the filling of the control gate 600 may become easier, which further reduces voids generated during the filling process of the control gate 600, thereby improving the yield of the manufactured semiconductor device.

[0074] Furthermore, taking FIG. 14 as an example, the structure of the semiconductor device is described as follows.

[0075] The semiconductor device may include the substrate 100, the oxide layer 200, the shallow trench isolation structures 400, the floating gates 500, the dielectric layer 700, and the control gate 600.

[0076] In some embodiments, the oxide layer 200 may be disposed on the substrate 100. The floating gates 500 may be disposed on the oxide layer 200.

[0077] The dielectric layer 700 may be formed on surfaces (an upper surface and sidewalls) of the floating gates 500. The control gate 600 may be formed in the trenches between the floating gates 500 and on the dielectric layer 700.

[0078] In some embodiments, the substrate 100 may be made of a semiconductor material, such as silicon, germanium, or silicon-germanium. The oxide layer 200 may be an oxide of silicon, such as silicon oxide. In a memory structure based on NOR FLASH, the oxide layer 200 may be referred to as an erase through oxide (ETOX) layer. The floating gates 500 and the control gate 600 may be polysilicon. The dielectric layer 700 may be an oxide layer, a nitride layer, or a stacked layer thereof. For example, the stacked layer may be formed by stacking the oxide layer and a mixed layer, which is formed by an oxide and a nitride,

together.

[0079] In some embodiments, the semiconductor device may further include a source and drain region (not shown in the figures). The source and drain region may be a conductive region formed in the substrate 100 by particle implantation/doping and led out through connected metal wires. It may be understood that the above-mentioned materials are merely examples, and similar materials may be used in other embodiments, which will not be described in detail herein.

[0080] The control gate 600 in the above semiconductor device may correspond to a gate of an ordinary transistor, with a difference in that the floating gates 500 are additionally provided. The floating gates 500 may have no electrical connection with the outside and may be surrounded and wrapped by the oxide layer 200 and the dielectric layer 700, which may be considered electrically floating and thus referred to as the floating gate. The floating gates may be configured to capture and store electrons. Since there is no external circuit, the electrons may not be lost even after power-off. The amount of electrons stored in the floating gate structure may change a threshold voltage, i.e., V_{th} , of the field effect transistor. Different V_{th} values may represent different states, thereby realizing information storage.

[0081] Next, referring to FIG. 15, FIG. 15 is a schematic circuit view of the semiconductor memory structure. The above-described semiconductor memory device may correspond to a field-effect transistor 1000 in FIG. 15. A gate of the transistor may correspond to the control gate 600 in FIG. 14 and may be connected to a white line (WL). A drain of the transistor may correspond to the drain in the source and drain region (not shown in the figures) of the semiconductor memory device and may be connected to a bit line (BL). The source of the transistor may correspond to the source in the source and drain region of the semiconductor device. The source may form a memory capacitor with a common source line (SL, not shown in the figures) in the semiconductor device.

[0082] The above semiconductor device may be considered as a memory cell. Each memory cell may include one access switch (i.e., a transistor) and one memory capacitor. The memory capacitor may represent logical “1” or “0” according to the amount of charge stored therein, or in other words, according to a voltage difference between two terminals of the memory capacitor being high or low. The conduction and cutoff of the access switch may determine

whether the information stored in the memory capacitor is allowed or prohibited to be read or rewritten.

[0083] In some embodiments, the word line WL may determine whether the access switch is conducted or cutoff. The bit line BL may be the only channel through which the outside accesses the memory capacitor. In a case where the access switch is conducted or turned on, external operations such as reading or writing of the memory capacitor may be performed through the bit line BL.

[0084] In some embodiments, a common terminal (Common) of the memory capacitor may be connected to a common source line (having a voltage of Vref).

[0085] In a case where the information stored in the memory capacitor represents “1,” a voltage at the other terminal of the memory capacitor may be 2Vref. In this case, the stored charge may be:

$$Q=+V_{ref}*C.$$

[0086] In a case where the information stored in the memory capacitor represents “0,” a voltage at the other terminal of the memory capacitor may be 0. In this case, the stored charge may be:

$$Q=-V_{ref}*C.$$

[0087] In some other embodiments, in a case where the semiconductor memory device shown in FIG. 14 is formed, a protective layer and/or an insulating layer may be covered on the semiconductor memory device. Wirings may be arranged in the protective layer and/or the insulating layer.

[0088] Furthermore, some embodiments of the present disclosure may further provide a memory device, which may include a semiconductor device. The semiconductor device may be the semiconductor device described above or a semiconductor device obtained through the manufacturing method described above.

[0089] In addition, the memory device may be a memory device including a flash memory (FLASH), for example, a NOR FLASH.

[0090] In some embodiments, the memory device may further include a main control chip and a memory chip. The memory chip may include a memory array and a corresponding configuration circuit and a corresponding wiring. The memory array may be the

semiconductor device provided in the above embodiments or a semiconductor device obtained through the manufacturing method provided in any one of the above embodiments.

[0091] The embodiments of the present disclosure may be implemented in the form of software functional units and may be sold or used as independent products. The software functional units may be stored in a computer-readable storage medium. Based on this understanding, the technical solutions of the present disclosure, or the parts thereof that essentially contribute to the prior art, may be embodied as a software product. The computer software product may be stored in a storage medium and may include several instructions for enabling a computer device (which may be a personal computer, a server, or a network device, etc.) or a processor to execute all or part of the operations of the methods described in the embodiments of the present disclosure. The aforementioned storage medium may include various media capable of storing program codes, such as a USB flash drive, a mobile hard disk, a read-only memory (ROM), a random-access memory (RAM), a magnetic disk, or an optical disk.

[0092] The foregoing description is merely exemplary embodiments of the present disclosure and is not intended to limit the scope of the present disclosure. Any equivalent structural or process transformations made based on the content of the specification and drawings of the present disclosure, or any direct or indirect applications to other related technical fields, shall be included within the protection scope of the present disclosure.

CLAIMS

1. A method for manufacturing a semiconductor device, comprising:

forming shallow trench isolation structures in a substrate, wherein each shallow trench isolation structure has a protruding portion protruding from a surface of the substrate and first trenches are defined between the adjacent protruding portions of the shallow trench isolation structures;

forming floating gates in the first trenches and performing a first etching on a part of the protruding portions of the shallow trench isolation structures, wherein second trenches are formed between the adjacent floating gates;

performing a narrowing process on the floating gates;

performing a second etching on a remaining part of the protruding portions of the shallow trench isolation structures to widen the second trenches; and

forming a control gate, wherein the control gate is partially filled in the second trenches.

2. The method as claimed in claim 1, wherein before forming the control gate, the method further comprises:

etching a dielectric layer on the floating gates.

3. The method as claimed in claim 1, wherein before forming the control gate, the method further comprises:

growing a dielectric layer on the floating gates.

4. The method as claimed in claim 3, wherein the dielectric layer comprises a first oxide layer, a first nitride layer, and a second oxide layer; and

wherein the growing a dielectric layer on the floating gates, comprises:

growing the first oxide layer on the floating gates;

growing the first nitride layer on the first oxide layer; and

growing the second oxide layer on the first nitride layer.

5. The method as claimed in claim 3, wherein a part of the dielectric layer is disposed on sidewalls of the floating gates, forming sidewalls of the second trenches.

6. The method as claimed in claim 1, wherein the forming floating gates in first trenches, comprises:

forming a polysilicon layer in the first trenches; and

etching the polysilicon layer to form the floating gates, wherein an upper surface of the floating gates is higher than or flush with an upper surface of the shallow trench isolation structures.

7. The method as claimed in claim 1, wherein sidewalls of the second trench are formed by opposing sidewalls between the adjacent floating gates, each of the floating gates comprises a first sidewall and a second sidewall, the first sidewall is connected to a bottom of the second trench, and the second sidewall is connected to the first sidewall;

an included angle between the first sidewall and the bottom of the second trench is less than or equal to 90 degrees and an included angle between the second sidewall and the bottom of the second trench is greater than 90 degrees.

8. The method as claimed in claim 1, wherein a cross-sectional area of the control gate located at a bottom of the second trenches is smaller than a cross-sectional area of the control gate located at an opening of the second trenches.

9. A semiconductor device, obtained through the method as claimed in any one of claims 1-8.

10. A memory device, comprising a semiconductor memory device that is the semiconductor device as claimed in claim 9 or is obtained through the method as claimed in any one of claims 1-8.