

CLAIMS

I/We claim:

1. A semiconductor package comprising:
a package substrate;
a first semiconductor die mounted to the package substrate, the first semiconductor die including a first redistribution structure, the first redistribution structure including—
a first signal trace electrically coupled to a first die contact, a first interconnect pad, and a first package contact, and
a second signal trace electrically coupled to a second interconnect pad and a second package contact, wherein the second signal trace is electrically isolated from the first signal trace; and
a second semiconductor die mounted to the first semiconductor die, the second semiconductor die including a second redistribution structure having a third signal trace electrically coupled to a second die contact, a third interconnect pad and a fourth interconnect pad,
wherein (1) the first interconnect pad of the first redistribution structure is aligned with the third interconnect pad of the second redistribution structure such that the first and third interconnect pads can be bridged by an interconnect structure, and (2) the second interconnect pad of the first redistribution structure is aligned with the fourth interconnect pad of the second redistribution structure such that the second and fourth interconnect pads can be bridged by an interconnect structure.
2. The semiconductor package of claim 1, further comprising an interconnect structure electrically coupling the first and second semiconductor dies.
3. The semiconductor package of claim 2 wherein the interconnect structure comprises a solder bump.

4. The semiconductor package of claim 2 wherein the interconnect structure connects the first interconnect pad to the third interconnect pad such that the first and second die contacts are both electrically coupled to the first package contact.

5. The semiconductor package of claim 2 wherein the interconnect structure connects the second interconnect pad to the fourth interconnect such that the first die contact is electrically coupled to the first package contact and the second die contact is electrically coupled to the second package contact.

6. The semiconductor package of claim 1 wherein:
the first redistribution structure is located on an upper surface of the first semiconductor die;
the second redistribution structure is located on a lower surface of the second semiconductor die; and
the first and second semiconductor dies are mounted on the package substrate with the upper surface of the first semiconductor die facing the lower surface of the second semiconductor die.

7. The semiconductor package of claim 1 wherein:
the first die contact, the first interconnect pad, and the second interconnect pad are at an interior portion of the first semiconductor die;
the first and second package contacts are at a peripheral portion of the first semiconductor die; and
the second die contact, the third interconnect pad, and the fourth interconnect pad are at an interior portion of the second semiconductor die.

8. The semiconductor package of claim 1 wherein the first and second package contacts are electrically coupled to respective first and second bond pads on the package substrate via wire bonds.

9. The semiconductor package of claim 8 wherein the package substrate is coupled to a first electrical connector and a second electrical connector, the first electrical connector is

electrically coupled to the first bond pad, and the second electrical connector is electrically coupled to the second bond pad.

10. The semiconductor package of claim 9 wherein the first and second electrical connectors are individual solder balls of a ball grid array.

11. The semiconductor package of claim 9 wherein the first and second bond pads are electrically coupled to the first and second electrical connectors via first and second wiring structures, respectively, and wherein the first and second wiring structures are routed on different layers of the package substrate.

12. A method of manufacturing a semiconductor package, the method comprising:
forming a first redistribution structure on a first semiconductor die, the first redistribution structure including—
a first signal trace electrically coupled to a first die contact, a first interconnect pad, and a first package contact, and
a second signal trace electrically coupled to a second interconnect pad and a second package contact;
forming a second redistribution structure on a second semiconductor die, the second redistribution structure including a third signal trace having a third signal trace electrically coupled to a second die contact, a third interconnect pad and a fourth interconnect pad; and
selecting, based on a design of the semiconductor package, either a first position or a second position for an interconnect structure between the first and second semiconductor dies, wherein—
when in the first position, the interconnect structure is between the first interconnect pad and the third interconnect pad so as to electrically couple the second die contact to the first package contact, and
when in the second position, the interconnect structure is between the second interconnect pad and the fourth interconnect pad so as to electrically couple the second die contact to the second package contact; and
electrically coupling the first and second semiconductor dies with the interconnect structure in the selected first or second position.

13. The method of claim 12 wherein the first signal trace is electrically isolated from the second signal trace.

14. The method of claim 12 wherein the design is a x4 and/or a x8 package design and the method further comprises positioning the interconnect structure in the first position such that the first and second die contacts are electrically coupled to the first package contact.

15. The method of claim 14, further comprising transmitting a signal from one or more of the first die contact or the second die contact to the first package contact.

16. The method of claim 12 wherein the design is a x16 package design and the method further comprises positioning the interconnect structure in the second position such that the first die contact is electrically coupled to the first package contact and the second die contact is electrically coupled to the second package contact.

17. The method of claim 16, further comprising:
transmitting a first signal from the first die contact to the first package contact; and
transmitting a second signal from the second die contact to the second package contact,
wherein the second signal is different from the first signal.

18. The method of claim 12, further comprising:
mounting the first semiconductor die on a package substrate; and
mounting the second semiconductor die on the first semiconductor die.

19. The method of claim 18 wherein the first and second semiconductor dies are mounted in a face-to-face configuration.

20. The method of claim 18, further comprising wirebonding the first semiconductor die to the package substrate.

21. The method of claim 20, further comprising transmitting a signal from the second semiconductor die to the package substrate via the first and second redistribution structures and the interconnect structure.