

ABSTRACT

A semiconductor device includes a gate pattern disposed over a lower structure, and including a gate electrode region and a gate pad region extending from the gate electrode region; and a vertical channel semiconductor layer having a side surface facing the gate electrode region of the gate pattern. The gate pad region includes a first pad region having a thickness greater than a thickness of the gate electrode region. The first pad region includes an upper surface, a lower surface opposing the upper surface, and an outer side surface. The outer side surface has a lower outer side surface and an upper outer side surface, divided from each other by a boundary portion. The lower outer side surface extends from the lower surface, and a connection portion of the lower outer side surface and the lower surface has a rounded shape.

FIG. 2B