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USER INPUT DEVICE WITH MEMORY

Field of the Invention

The present invention relates to a combined memory and user input device for a program-controlled apparatus.

Background to the Invention

The Nintendo (RTM) Gameboy (RTM) is a well-known portable video game device. The Nintendo (RTM) Gameboy (RTM) comprises a housing containing a processor, a display screen and pushbutton user input devices. The programs for video games are supplied in the form of ROM cartridges which are plugged into the body so that the processor can run the program stored in the ROM cartridge. A problem arising with the Nintendo (RTM) Gameboy (RTM) is that the arrangement of pushbuttons must serve for different types of game and a user input device suitable for a platform game will generally not be optimum for a motor racing game or a flight simulator game.

Summary of the Invention

The present invention addresses this problem of portable video game devices. However, it is more generally applicable to program-controlled apparatuses, e.g. personal digital organisers and smartphones, for providing user input means appropriate for a particular program.

According to the present invention, there is provided a program-controlled apparatus comprising a main portion including a processor and a display device controllable by the processor for displaying images, and a subsidiary portion including memory means, storing a program for the processor, and user input means, wherein the subsidiary portion can be temporarily arranged relative to the main portion for the communication of codes of said program to the main portion and communication of data (including commands), generated by operation of the user input means, to the main portion, said data providing inputs for said program when being run by the processor.



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According to the present invention, there is also provided a program-controlled apparatus comprising:

a main portion including

a processor, and

a display device controllable by the processor for displaying images, and

first and second subsidiary portions, each including

memory means, storing a respective program for the processor, and

user input means,

wherein

the subsidiary portions can be interchangeably, temporarily arranged relative to the main portion for the communication of codes of said programs to the main portion and communication of data (including commands), generated by operation of the user input means, to the main portion, said data providing inputs for said programs when being run by the processor,

the user input means of the first subsidiary portion is different from the user input means of the second subsidiary portion, and

data capable of being communicated from the first subsidiary portion has the same form as the data capable of being communicated from the second subsidiary portion.

Consequently, the form of the data is independent of the form of the user input means, e.g. whether it is analogue or digital in its operation.

The program code may be transferred en masse to the main portion for storage in the main portion while the program is run. Alternatively, the code can be read from the subsidiary portion while the program is being run.

Preferably, the main portion and the or each subsidiary portion have complementary electrical connector means which, when mated, provide a route for said communication of codes and data. However, the data and codes may be communicated from the subsidiary portion to the main portion through free space by electromagnetic waves.

Preferably, the or each subsidiary portion includes a circuit responsive to operation of its user input means to generate said data for communication to the main portion. In a simple case, the user input means may comprise switches between two contacts of a connector so that circuitry in the main portion can detect whether the switches are open or closed.

Preferably, said data comprise codes comprising a plurality of bits which are all of the same length. Alternatively, said data could each comprise one of a plurality of command codes with optional parameters, e.g. command type + magnitude.

The form of the main portion may be substantially determined by the form of the display device with the subsidiary portion connectable to an edge of the main portion. Preferably, the display device has a side edge and the subsidiary portion is connectable to the side edge of the display device. Preferably, an auxiliary portion having user input means is included and the main portion and auxiliary portion have complementary connector means for the communication of data, generated by operation of the user input means of the auxiliary portion, to the main portion, said data providing inputs for said program when being run by the processor. More preferably, the subsidiary portion and the auxiliary portion are configured to provide handles for the apparatus.

The user input means may take many forms depending on the software in the memory means. For instance, a keyboard would be appropriate for a program requiring text input whereas a conventional "Gameboy" key arrangement would be suitable for a platform game. The user input means need not be a manually operable device and could comprise a microphone.

The memory means may store one or more programs.

Conveniently, the or each memory means comprises a solid-state ROM. However, the memory means could comprise a disk drive and disk.

According to the present invention, there is also provided a subsidiary portion for an apparatus according to the present invention.

Brief Description of the Drawings

Figure 1 is a perspective view of a first embodiment of the present invention;

Figure 2 is an exploded view of the embodiment of Figure 1;

Figure 3 is a block diagram of the embodiment of Figure 1;

Figure 4 is a circuit diagram of the plug-in module shown in Figure 1;

Figure 5 is an exploded view of the embodiment of Figure 1 with a keyboard module;

Figure 6 is a circuit diagram of the keyboard module;

Figure 7 is a front view of a second embodiment of the present invention; and

Figure 8 is a front view of alternative plug-in modules for the embodiment of Figure 7.

Detailed Description of Preferred Embodiment

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings.

Referring to Figures 1 and 2, an apparatus according to the present invention comprises a main body 1 and a plug-in module 2. The main body 1 is rectangular in plan view and has a raised portion 3 extending from one end halfway along the main body 1. A liquid crystal display 4 is mounted in the top of the raised portion 3. A multi-way connector 5 is mounted in the face of the raised portion 3 at the mid-point of the main body 1. A pair of hook members 6, 7 are located at the end of the main body 1 opposite the raised portion 3.

The plug-in module 2 is provided with a multi-way connector (not shown) for connecting to the multi-way connector 5 of the main body 1 and recesses (not shown) for engaging the hook members 6, 7 so that the plug-in module 2 can be releasably connected to the main body 1. With the plug-in module 2 in place, the apparatus becomes rectangular in side view also.

The upper surface of the plug-in module 2 is provided with a cruciform membrane switching element 8 and two circular membrane switching elements 9, 10.

Referring to Figure 3, the main body 1 houses a battery 20 for supplying power to the circuitry of the main body 1 and of the plug-in module 2 via a switch, a microprocessor 21, a display driver 22 for the display 4, a ROM 23, a RAM 24 and an I/O interface circuit 25. The microprocessor 21, the display driver 22, the ROM 23, the RAM 24 and the an I/O interface circuit 25 are interconnected by a multiplexed address and data bus 26. The bus 26 extends through the connector 5 (Figure 2) into the plug-in module 2 and is connected to a ROM 27 in the plug-in module 2. Consequently, the microprocessor 21 can read program instruction codes from the ROM 27 in the plug-in module 2. The ROM 27 stores a program for a platform game.

The membrane switching elements 8, 9, 10 are connected to a command processing circuit 28 in the plug-in module 2. The command processing circuit 28 outputs 8-bit command codes to the I/O interface circuit 25 and interrupt signals to the microprocessor 21 in response to operation of the membrane switching elements 8, 9, 10. The 8-bit command codes and the interrupt signals pass through the connector 5.

The operation of microcomputers is well known to those skilled in the art and will not be repeated here. However, the generation and processing of user input commands will be described.

Referring to Figure 4, the command processing circuit 28 comprises a first 3-input OR-gate 30 whose inputs are connected to switches operated by respective arms of the cruciform membrane switching element 8, a second 3-input OR-gate 31 whose inputs are connected respectively to the switches operated by the remaining arm of the cruciform membrane switching element 8 and the switches of the circular membrane switching elements 9, 10, a 2-input OR-gate 32 whose inputs are coupled to the outputs of the 3-input OR-gates 30, 31, a clock 33, a 2-input AND-gate 34 whose inputs are connected to the output of the 2-input OR-gate 32 and the clock

33 and an 8-bit latch 35. The latch 35 is arranged to be clocked by the output of the 2-input AND-gate 34.

Six of the inputs of the latch 35 are connected to the switches operated by the arms of the cruciform membrane switching element 8 and the circular membrane switching elements 9, 10. The other two inputs of the latch 35 are connected to 0V. The outputs of the latch 35 are connected to respective contacts of the connector 36 which mates with the connector 5 on the main body 1 (Figure 2). The output of the 2-input AND-gate 34 is connected to another contact of the connector 36.

At rest, the inputs to the 3-input OR-gates 30, 31 and the latch 35 are all at logic 0. When a user presses the first circular membrane switch element 9, the corresponding switch is closed, bringing the first input of the latch 35 and one of the inputs of the second 3-input OR-gate 31 to logic 1. The output of the second 3-input OR-gate then goes to logic 1 and consequently the output of the 2-input OR-gate 32. If a clock pulse occurs while the output of the 2-input OR-gate 32 is at logic 1, the output of the AND-gate 34 goes to logic 1 for the duration of the clock pulse. The pulse output by the AND-gate 34 clocks the latch 35 causing the logic 1 on the latch's first input and the logic 0s on its other inputs to be transferred to its outputs. The pulse output by the AND-gate 34 is also fed to an interrupt port of the microprocessor 21 (Figure 3) via the connector 36. The microprocessor 21 responds to the interrupt by reading the output of the latch 35 via the I/O interface circuit 25 (Figure 3). The response of the microprocessor 21 to the read latch output will depend on the program being run by the microprocessor 21, e.g. the program stored in the ROM 27 in the plug-in module 2.

It can be seen that a similar sequence of events will follow pressing of another of the membrane switching elements and that operation of each element will produce a unique code at the output of the latch 35.

Referring to Figure 5, another plug-in module 40 has a membrane alphanumeric matrix keyboard 41 mounted to its upper face. The module's ROM is programmed with text processing software.

Referring to Figure 6, the switches of the keyboard 41 are arranged in columns and rows. Pulses are sequentially applied to the rows by a ring counter 42. The outputs of the ring counter 42 are also fed to the inputs of an encoder 43. The encoder outputs a 3-bit binary number giving the identity of the row, i.e. 0, 1, 2, 3, 4, 5, to which a pulse is being applied. The columns of the matrix are also connected to the inputs of a similar encoder 44. The outputs of the encoders 43, 44 are connected to the address inputs of an n x 8-bit ROM 45. The 8 outputs of the ROM 45 are connected to respective inputs of an 8-bit latch 46. The outputs of the latch 46 are connected to respective contacts of a connector 47 for mating with the connector 5 on the main body (Figure 2).

Three of the columns of the matrix are connected to the inputs of a first 3-input OR-gate 48. The other three columns are connected to the inputs of a second 3-input OR-gate 49. The outputs of the 3-input OR-gates 48, 49 are connected to the inputs of a 2-input OR-gate 50. The output of the 2-input OR-gate 50 is connected to the read enable input of the ROM 45 and to the input of a delay 51. The output of the delay 51 is connected to the clock input of the latch 46 and a contact of the connector 47.

When a user presses one of the keys of the keyboard 41, e.g. key A, one of the columns (2) is briefly connected to one of the rows (2). In this case, since the ring counter 42 cycles rapidly, a pulse will be applied to row (2) while it is connected to column (2). Consequently, the pulse will be applied to one input of the first 3-input OR-gate 48 and to one input of the second encoder 44. At this point, both encoders 43, 44 output 010 so the address input to the ROM 45 is 010010.

The output of the first 3-input OR-gate 48 goes to logic 1 causing the output of the 2-input OR-gate 50 to go to logic 1 also. The output of the 2-input OR-gate 50 being at logic 1 enables reading of the ROM 45. Consequently, the 8-bit code at location 010010 in the ROM 45 appears at the ROM's output. This code is then input into the latch 46 and transferred to the output of the latch 46 when the pulse

output by the 2-input OR-gate 50 has propagated through the delay 51. The delay provides time for the input to the latch 46 to stabilise before the latch 46 is clocked.

The output of the delay 51 is also carried to an interrupt input of the microprocessor 21 (Figure 3) and causes the microprocessor 21 to read the output of the latch 46 via the I/O interface circuit 25 (Figure 3).

Referring to Figure 7, a second embodiment of the present invention comprises a rectangular panel 60. A liquid crystal display 61 takes up substantially all of one face of the panel 60 First and second clip-on handles 62, 63 are provided on the right and left sides of the panel 60. The first clip-on handle 62 is electrically equivalent to the plug-in modules of the first embodiment described above and an electrical connection is made between the first clip-on handle 62 and microcomputer circuitry in the panel 60. The second clip-on handle 63 lacks a ROM and includes only user input command processing circuitry. An electrical connection is made between the second clip-on handle 63 and the microcomputer circuitry in the panel 60 so that the microcomputer circuitry can receive user input commands therefrom.

The first clip-on handle 62 has three membrane switching elements 64, 65, 66 and the second clip-on handle 63 has a trackball 67.

Referring to Figure 8, the first clip-on handle 72 of an alternative pair has a touch sensitive bar 74 as a user input device and the second clip-on handle 73 has no input devices.

Claims

1. A program-controlled apparatus comprising a main portion including a processor and a display device controllable by the processor for displaying images, and a subsidiary portion including memory means, storing a program for the processor, and user input means, wherein the subsidiary portion can be temporarily arranged relative to the main portion for the communication of codes of said program to the main portion and communication of data, generated by operation of the user input means, to the main portion, said data providing inputs for said program when being run by the processor.

2. A program-controlled apparatus comprising:

a main portion including

a processor, and

a display device controllable by the processor for displaying images, and

first and second subsidiary portions, each including

memory means, storing a respective program for the processor, and

user input means,

wherein

the subsidiary portions can be interchangeably, temporarily arranged relative to the main portion for the communication of codes of said programs to the main portion and communication of data, generated by operation of the user input means, to the main portion, said data providing inputs for said programs when being run by the processor,

the user input means of the first subsidiary portion is different from the user input means of the second subsidiary portion, and

data capable of being communicated from the first subsidiary portion has the same form as data capable of being communicated from the second subsidiary portion.

3. An apparatus according to claim 1 or 2, wherein the main portion and the or each subsidiary portion have complementary electrical connector means which, when mated, provide a route for said communication of codes and data

4. An apparatus according to claim 1, 2 or 3, wherein the or each subsidiary portion includes a circuit responsive to operation of its user input means to generate said data for communication to the main portion.

5. An apparatus according to any preceding claim, wherein said data comprise codes comprising a plurality of bits which are all of the same length.

6. An apparatus according to any one of claims 1 to 4, wherein said data each comprise one of a plurality of command codes.

7. An apparatus according to claim 6, wherein an element of the data comprises additionally a parameter.

8. An apparatus according to any preceding claim, wherein the form of the main portion is substantially determined by the form of the display device and the subsidiary portion is connectable to an edge of the main portion.

9. An apparatus according to claim 8, wherein the display device has a side edge and the subsidiary portion is connectable to the side edge of the display device.

10. An apparatus according to claim 8 or 9, including an auxiliary portion having user input means, wherein the main portion and auxiliary portion have complementary connector means for the communication of data, generated by operation of the user input means of the auxiliary portion, to the main portion, said data providing inputs for said program when being run by the processor.

11. An apparatus according to claim 10, wherein the subsidiary portion and the auxiliary portion are configured to provide handles for the apparatus.

12. An apparatus according to any preceding claim, wherein the user input means comprises a keyboard.

13. An apparatus according to any preceding claim, wherein the or each memory means comprises a solid-state ROM.

14. A subsidiary portion for an apparatus according to any preceding claim.