BILAYER HDP CVD / PE CVD CAP IN ADVANCED BEOL INTERCONNECT STRUCTURES AND METHOD THEREOF

Technical Field

This invention relates generally to the manufacture of high speed semiconductor microprocessors, application specific integrated circuits (ASICs), and other high speed integrated circuit devices. More particularly, this invention relates to a novel bilayer cap in advanced back-end-of-line (BEOL) interconnect structures for semiconductor devices using low-k dielectric materials. The invention is specifically directed to a bilayer cap comprising high-density plasma chemical vapor deposition (HDP CVD) materials and plasma-enhanced chemical vapor deposition (PE CVD) material in advanced BEOL metallization structures, and a method of forming the bilayer cap.

Background Art

In semiconductor devices, aluminum and aluminum alloys have been used as the traditional interconnect metallurgies. While aluminum-based metallurgies have
been the material of choice for use as metal interconnects over the past years, concern now exists as to whether aluminum will meet the demands required as circuit
density and speeds for semiconductor devices increase. Because of these growing concerns, other materials have been investigated as possible replacements for aluminum-based metallurgies.

One highly advantageous material now being considered as a potential replacement for aluminum metallurgies is copper, because of its lower

susceptibility to electromigration failure as compared to aluminum, as well as its lower resistivity.

Despite these advantages, copper suffers from an important disadvantage. Copper readily diffuses into the surrounding dielectric material during subsequent processing steps. To inhibit the diffusion of copper, copper interconnects are often capped with a protective barrier layer. One method of capping involves the use of a conductive barrier layer of tantalum, titanium or tungsten, in pure or alloy form, along the sidewalls and bottom of the copper interconnection. To cap the upper surface of the copper interconnection, a dielectric material such as silicon nitride (Si_3N_4) is typically employed.

Figure 1 illustrates a conventional BEOL interconnect structure utilizing copper metallization and the protective cap layers described above. The interconnect structure comprises a lower substrate (10) which may contain logic circuit elements such as transistors. A dielectric layer (12), commonly known as an inter-layer dielectric (ILD), overlies the substrate (10). ILD layer (12) may be formed of silicon dioxide (SiO_2). However, in advanced interconnect structures, ILD layer (12) is preferably a low-k polymeric thermoset material such as SiLK™ (an aromatic hydrocarbon thermosetting polymer available from The Dow Chemical Company). An adhesion promoter layer (11) may be disposed between the substrate (10) and ILD layer (12). A layer of silicon nitride (13) is optionally disposed on ILD layer (12). Silicon nitride layer (13) is commonly known as a hardmask layer or polish stop layer. At least one conductor (15) is embedded in ILD layer (12). Conductor (15) is preferably copper in advanced interconnect structures, but alternatively may be aluminum or other conductive material. When conductor (15) is copper, a diffusion barrier liner (14) is preferably disposed between ILD layer (12) and conductor (15). Diffusion barrier liner (14) is typically comprised of tantalum, titanium, tungsten or nitrides of these metals. The top surface of conductor (15) is made coplanar with the top surface of silicon nitride layer (13), usually by a chemical-mechanical polish (CMP) step. A cap layer (16), also typically of silicon nitride, is disposed on conductor (15) and silicon nitride layer (13). Cap layer (16) acts as a diffusion barrier to prevent diffusion of copper

from conductor (15) into the surrounding dielectric material during subsequent processing steps.

A first interconnect level is defined by adhesion promoter layer (11), ILD layer (12), silicon nitride layer (13), diffusion barrier liner (14), conductor (15), and cap layer (16) in the interconnect structure shown in Figure 1. A second interconnect level, shown above the first interconnect level in Figure 1, includes adhesion promoter layer (18), ILD layer (19), silicon nitride layer (20), diffusion barrier liner (21), conductor (22), and cap layer (23). The first and second levels may be formed by conventional damascene processes. For example, formation of the second interconnect level begins with deposition of adhesion promoter layer (18). Next, the ILD material (19) is deposited onto adhesion promoter layer (18). If the ILD material is a low-k polymeric thermoset material such as SiLK™, the ILD material is typically spin-applied, given a post apply hot bake to remove solvent, and cured at elevated temperature. Next, silicon nitride layer (20) is deposited on the ILD. Silicon nitride layer (20), ILD layer (19), adhesion promoter layer (18) and cap layer (16) are then patterned, using a conventional photolithography and etching process, to form at least one trench and via. The trenches and vias are typically lined with diffusion barrier liner (21). The trenches and vias are then filled with a metal such as copper to form conductor (22) in a conventional dual damascene process. Excess metal is removed by a CMP process. Finally, cap layer (23) is deposited on copper conductor (22) and silicon nitride layer (20).

Due to the need for low temperature processing after copper deposition, cap layers are typically deposited at temperatures below 450°C. Accordingly, cap layer deposition is typically performed using plasma-enhanced chemical vapor deposition (PE CVD) or high density plasma chemical vapor deposition (HDP CVD) wherein the deposition temperature generally ranges from about 200°C to about 500°C.

PE CVD and HDP CVD films have been used for many other applications in semiconductor device manufacturing. However, in using a cap layer such as

silicon nitride for copper interconnects, conventional PE CVD or HDP CVD silicon nitride films create reliability problems.

HDP CVD films such as silicon nitride provide superior electromigration protection, as compared to PE CVD films, because HDP CVD films more readily stop the movement of copper atoms along the interconnect surface in the cap layer. However, in a conventional HDP deposition process, a seam is formed in the HDP CVD cap layer, and a crack in the cap layer often develops at this seam due to stress within the structure. If the crack develops in a portion of the cap layer overlying a copper conductor, the copper conductor may be readily exposed to moisture and other sources of oxygen. If the crack develops in a portion of the cap layer overlying the ILD, the copper conductor may be exposed to moisture diffusing through the ILD. In the latter case, the seam is of relatively minor concern in interconnect structures utilizing silicon dioxide as the ILD material, because the rate of moisture diffusion through silicon dioxide is very low. However, in interconnect structures utilizing low-k polymeric thermoset dielectric materials such as SiLK™, this seam is of greater concern, because the rate of moisture diffusion through most spin-on and CVD low-k materials is relatively high.

Moreover, any crack in the cap layer may lead to copper diffusion into the ILD through the seam. As a result of this copper diffusion, a copper nodule may form under the cap layer through the seams. This copper nodule may lead to leakage between adjacent interconnect lines.

Another significant disadvantage occurs when HDP CVD films are integrated with low-k dielectric materials. The energetic reactions of the HDP CVD process can enable interaction with and within the low-k materials causing undesirable changes to occur.

Such changes in low-k dielectric materials can be significantly mitigated by the use of PE CVD films. Moreover, in typical PE CVD films, no seam is formed during the deposition process. For this reason, PE CVD cap layers have been used to cap copper interconnect structures in earlier ground-rule devices, such as the 0.22 μm technology node. However, in more advanced ground-rule devices, such

as the 0.18 μm technology node, PE CVD films have been found to be inferior to cap layers formed by other deposition techniques such as HDP CVD.

In particular, PE CVD films generally exhibit poorer adhesion to the copper surface. Typical PE CVD silicon nitride films exhibit adhesion values in the range of about 5 to less than 10 joules/m^2, whereas typical HDP CVD silicon nitride films exhibit adhesion values of about 20 joules/m^2, as determined by a four-point bend adhesion testing technique. PE CVD films may delaminate and form blisters over patterned copper lines, particularly during subsequent dielectric depositions, metallization, and chemical-mechanical polishing. After being deposited onto copper metallurgy, additional insulating layers generally will be deposited over the cap layer. However, subsequent deposition of insulating layers onto the cap layer will produce stress which can cause the cap layer to peel from the copper surface. This delamination results in several catastrophic failure mechanisms, including lifting interlayer dielectrics, lifting copper conductors, copper diffusion from uncapped copper lines, and electromigration. Such results are generally seen in dual damascene processing where delamination of the silicon nitride hardmask layer generally occurs during copper chemical-mechanical polishing.

Thus, there is a need in the art for an interconnect structure cap layer exhibiting the superior electromigration protection and adhesion characteristics of HDP CVD films, and the superior coverage of PE CVD films.

Disclosure of Invention

The problems described above are addressed through use of the present invention, which is directed to an interconnect structure formed on a substrate. In a preferred embodiment, the structure comprises a dielectric layer overlying the substrate; a hardmask layer on said dielectric layer, said hardmask layer having a top surface; at least one conductor embedded in said dielectric layer and having a surface coplanar with the top surface of said hardmask layer; a first cap layer on said at least one conductor and on said hardmask layer, said first cap layer preferably being formed by a high density plasma chemical vapor deposition (HDP

CVD) process; and at least one second cap layer on said first cap layer. The second cap layer may be formed by any suitable method, such as by a physical vapor deposition (PVD) process, by a spin-on process, or even by a HDP CVD process using process parameters different from those used for the first cap layer. The second cap layer is preferably formed by a plasma-enhanced chemical vapor deposition (PE CVD) process.

The present invention is also directed to a method of forming an interconnect structure on a substrate. In one embodiment, the method comprises the steps of: depositing a dielectric material on the substrate, thereby forming a dielectric layer, depositing a hardmask material on said dielectric layer, thereby forming a hardmask layer or layers, said hardmask layer having a top surface; forming at least one opening in said dielectric layer; filling said opening with a conductive material, thereby forming at least one conductor, said conductor having a surface coplanar with the top surface of said dielectric layer; depositing a first material on said conductor by a high density plasma chemical vapor deposition (HDP CVD) process, thereby forming a first cap layer; and depositing a second material on said first cap layer, preferably by a plasma-enhanced chemical vapor deposition (PE CVD) process, thereby forming a second cap layer.

Brief Description of Drawings

The features of the invention believed to be novel and the elements characteristic of the invention are set forth with particularity in the appended claims. The drawings are for illustration purposes only and are not drawn to scale. Furthermore, like numbers represent like features in the drawings. The invention itself, however, both as to organization and method of operation, may best be understood by reference to the detailed description which follows, taken in conjunction with the accompanying drawings, in which:

Figure 1 is a schematic cross-sectional view of a partially-fabricated integrated circuit device illustrating a prior art interconnect structure;

Figure 2 is a schematic cross-sectional view of a partially-fabricated integrated circuit device illustrating an interconnect structure in accordance with a preferred embodiment of the invention; and

Figures 3(a)-3(j) illustrate a method for forming the interconnect structure of Figure 2.

Best Mode for Carrying Out the Invention

The invention will now be described by reference to the accompanying figures. In the figures, various aspects of the structures have been shown and schematically represented in a simplified manner to more clearly describe and illustrate the invention. For example, the figures are not intended to be to scale. In addition, the vertical cross-sections of the various aspects of the structures are illustrated as being rectangular in shape. Those skilled in the art will appreciate, however, that with practical structures these aspects will most likely incorporate more tapered features. Moreover, the invention is not limited to constructions of any particular shape.

Although certain aspects of the invention will be described with respect to a structure comprising copper, the invention is not so limited. Although copper is the preferred conductive material, the structure of the present invention may comprise any suitable conductive material, such as aluminum.

Referring to Figure 2, a preferred embodiment of the interconnect structure of the invention comprises a lower substrate (110) which may contain logic circuit elements such as transistors. A dielectric layer (112), commonly known as an inter-layer dielectric (ILD), overlies the substrate (110). An adhesion promoter layer (111) may be disposed between the substrate (110) and ILD layer (112). A hardmask layer (113) is preferably disposed on ILD layer (112). At least one conductor (115) is embedded in ILD layer (112) and hardmask layer (113). A diffusion barrier liner (114) may be disposed between ILD layer (112) and conductor (115). The top surface of conductor (115) is made coplanar with the top

surface of hardmask layer (113), usually by a chemical-mechanical polish (CMP) step. A first cap layer (116) is disposed on conductor (115) and hardmask layer (113), and a second cap layer (117) is disposed on first cap layer (116).

A first interconnect level is defined by adhesion promoter layer (111), ILD layer (112), hardmask layer (113), diffusion barrier liner (114), conductor (115), first cap layer (116), and second cap layer (117) in the interconnect structure shown in Figure 2. A second interconnect level, shown above the first interconnect level in Figure 2, includes adhesion promoter layer (118), ILD layers (119), hardmask layer (120), diffusion barrier liner (121), conductor (122), first cap layer (123), and second cap layer (124).

ILD layers (112) and (119) may be formed of any suitable dielectric material, although low-k dielectric materials are preferred. Suitable dielectric materials include carbon-doped silicon dioxide materials; fluorinated silicate glass (FSG); organic polymeric thermoset materials, silicon oxycarbide; SiCOH dielectrics; fluorine doped silicon oxide; spin-on glasses; silsesquioxanes, including hydrogen silsesquioxane (HSQ), methyl silsesquioxane (MSQ) and mixtures or copolymers of HSQ and MSQ; benzocyclobutene (BCB) -based polymer dielectrics, and any silicon-containing low-k dielectric. Examples of spin-on low-k films with SiCOH-type composition using silsesquioxane chemistry include HOSP™ (available from Honeywell), JSR 5109 and 5108 (available from Japan Synthetic Rubber), Zirkon™ (available from Shipley Microelectronics, a division of Rohm and Haas), and porous low-k (ELk) materials (available from Applied Materials). Examples of carbon-doped silicon dioxide materials, or organosilanes, include Black Diamond™ (available from Applied Materials) and Coral™ (available from Novellus). An example of an HSQ material is FOx™ (available from Dow Corning). For this embodiment, preferred dielectric materials are organic polymeric thermoset materials, consisting essentially of carbon, oxygen and hydrogen. Preferred dielectric materials include the low-k polyarylene ether polymeric material known as SiLK™ (available from The Dow Chemical Company), and the low-k polymeric material known as FLARE™ (available from Honeywell). ILD layers (112) and (119) may each be about 100 nm to about 1000

nm thick, but these layers are each preferably about 600 nm thick. The dielectric constant for ILD layers (112) and (119) is preferably about 1.8 to about 3.5, and most preferably about 2.5 to about 2.9.

Alternatively, ILD layers (112) and (119) may be formed of a porous dielectric material, such as MesoELK™ (available from Air Products) and XLK™ (a porous version of FOx, available from Dow Corning). For example, If ILD layers (112) and (119) are formed of such porous dielectric material, the dielectric constant of these layers is preferably less than about 2.6, and is most preferably about 1.5 to 2.5. It is particularly preferred to use an organic polymeric thermoset material having a dielectric constant of about 1.8 to 2.2.

Adhesion promoter layers (111) and (118) are preferably about 9 nm thick, and may be composed of any material suitable for enhancing adhesion of the dielectric material in ILD layers (112) and (119) to the underlying surfaces. For example, if SiLK™ is used for ILD layers (112) and (119), adhesion promoter layers (111) and (118) may be formed of an adhesion promoter known as AP4000 (also available from The Dow Chemical Company).

Hardmask layers (113) and (120) may be formed of any suitable dielectric material. In one preferred embodiment, hardmask layers (113) and (120) are formed of silicon nitride, and preferably have a composition of about 30 to 45 atomic % silicon, about 30 to 55 atomic % nitrogen, and about 10 to 25 atomic % hydrogen. Most preferably, these silicon nitride hardmask layers have a composition of about 41 atomic % silicon, about 41 atomic % nitrogen, and about 17.5 atomic % hydrogen. Alternatively, in another preferred embodiment, hardmask layers (113) and (120) are formed of silicon carbide, and preferably have a composition of about 20 to 40 atomic % silicon, about 20 to 50 atomic % carbon and about 20 to 45 atomic % hydrogen. A particularly preferred composition is about 27 atomic % silicon, about 36 atomic % carbon and about 37 atomic % hydrogen.

Conductors (115) and (122) may be formed of any suitable conductive material, such as copper or aluminum. Copper is particularly preferred as the conductive material, due to its relatively low resistance. Copper conductors (115)

and (122) may contain small concentrations of other elements. Diffusion barrier liners (114) and (121) may comprise one or more of the following materials: tantalum, titanium, tungsten and the nitrides of these metals.

First cap layers (116) and (123) may be formed of silicon nitride, silicon carbide, boron nitride or other suitable dielectric material, and are preferably formed using a HDP CVD process. It has been discovered that materials deposited using a HDP CVD process provide superior adhesion and superior electromigration resistance. However, materials exhibiting similar properties but deposited by other processes may also be used for first cap layers (116) and (123). First cap layers (116) and (123) are most preferably formed of HDP CVD silicon nitride having a composition of about 30 to 50 atomic % silicon, about 40 to 65 atomic % nitrogen and about 5 to 13 atomic % hydrogen. A particularly preferred composition for first cap layers (116) and (123) is about 40 atomic % silicon, about 52 atomic % nitrogen, and about 8 atomic % hydrogen. First cap layers (116) and (123) preferably each have a thickness in the range of about 25 to 700 Å, and most preferably in the range of about 50 to 350 Å.

Second cap layers (117) and (124) may be formed of silicon nitride, silicon carbide, boron nitride, silicon oxide or other suitable dielectric material, but are preferably formed using a PE CVD process. Second cap layers (117) and (124) are most preferably formed of PE CVD silicon nitride having a composition of about 30 to 45 atomic % silicon, about 40 to 65 atomic % nitrogen, and about 10 to 25 atomic % hydrogen. A particularly preferred composition for second cap layers (117) and (124) is about 37 atomic % silicon, about 48 atomic % nitrogen, and about 15 atomic % hydrogen. In another preferred embodiment, second cap layers (117) and (124) are formed of PE CVD amorphous hydrogenated silicon carbide having a composition of about 20 to 40 atomic % silicon, about 20 to 50 atomic % nitrogen, and about 20 to 45 atomic % hydrogen, most preferably about 27 atomic % silicon, about 36 atomic % carbon, and about 37 atomic % hydrogen. In yet another preferred embodiment, second cap layers (117) and (124) are formed of PE CVD amorphous hydrogenated nitrogenated silicon carbide having a composition of about 20 to 34 atomic % silicon, about 12 to 34 atomic % carbon, about 5 to 30

atomic % nitrogen and about 20 to 50 atomic % hydrogen, most preferably about 22 to 30 atomic % silicon, about 15 to 30 atomic % carbon, about 10 to 22 atomic % nitrogen and about 30 to 45 atomic % hydrogen. Second cap layers (117) and (124) preferably each have a thickness in the range of about 100 to 1000 Å, and most preferably in the range of about 250 to 700 Å.

Second cap layers (117) and (124) may be formed of a series of thin PE CVD films, where the total thickness is in the range of about 100 to 1000 Å. In one embodiment, these thin PE CVD films each may be formed of the same material, such as silicon nitride. In another embodiment, the thin PE CVD films may be formed of different materials, such as silicon nitride, silicon carbide, silicon oxide, silicon oxycarbide, and/or silicon oxycarbonitride. The second cap layer also may be formed of alternating layers of high-permeability or high-affinity dielectric films and low-permeability or low-affinity dielectric films, such as the laminated diffusion barrier described in co-pending U.S. Application Ser. No. 09/858,687, filed May 16, 2001 and titled "Laminated Diffusion Barrier," the disclosure of which is incorporated herein by reference. The second cap layer may comprise alternating films of different material or a series of films of the same material together with films of a different material. For example, the second cap layer may comprise: three thin films of PE CVD silicon nitride, each having a thickness of about 5 nm; a thin film of PE CVD silicon oxide having a thickness of about 5 nm; a thin film of PE CVD silicon nitride having a thickness of about 5 nm; and a thin film of PE CVD silicon nitride having a thickness of about 5 nm. As another example, the second cap layer may be formed of a series of PE CVD films comprising: a thin film of PE CVD silicon nitride having a thickness of about 5 nm; a thin film of PE CVD silicon oxide having a thickness of about 5 nm; a thin film of PE CVD silicon nitride having a thickness of about 5 nm; a thin film of PE CVD silicon oxide having a thickness of about 5 nm; a thin film of PE CVD silicon nitride having a thickness of about 5 nm; and a thin film of PE CVD silicon oxide having a thickness of about 5 nm. The series of films may comprise up to 6 layers of the same or different material, or may comprise more than 6 layers of the same or different material.

Alternatively, second cap layers (117) and (124) may be formed by a physical vapor deposition (PVD) process, by a spin-on process, or even by a HDP CVD process using process parameters different from those used for the first cap layer.

The interconnect structure of Figure 2 may be formed by a damascene or dual damascene process, such as the process shown in Figures 3(a)-3(j). The process preferably begins with deposition of adhesion promoter layer (111) on substrate (110), and is followed by deposition of ILD layer (112) on adhesion promoter layer (111), as shown in Figure 4(a). Adhesion promoter layer (111) and ILD layer (112) may be deposited by any suitable method. For example, if adhesion promoter layer (111) is formed of AP4000, the adhesion promoter solution may be applied by a spin-coating process, followed by a baking step. If SiLK™ is used for ILD layer (112), the resin may be applied by a spin-coating process, followed by a baking step to remove solvent and then a thermal curing step.

Hardmask layer (113) is then deposited on ILD layer (112), as shown in Figure 3(a). Hardmask layer (113) may be deposited by any suitable method, but is preferably deposited by chemical vapor deposition (CVD) directly onto ILD layer (112). In one preferred embodiment, a silicon nitride hardmask layer (113) is deposited in a CVD reactor at a pressure in the range of about 0.1 to 10 torr, most preferably in the range of about 1 to 5 torr, using a combination of gases that may include, but are not limited to, silane (SiH_4), ammonia (NH_3), nitrogen (N_2) and helium (He). A typical deposition process uses a flow of SiH_4 in the range of about 100 to 700 sccm, a flow of NH_3 in the range of about 100 to 5000 sccm, and a flow of N_2 in the range of about 100 to 5000 sccm. The deposition temperature is typically within the range of about 150 to 500°C, most preferably in the range of about 350 to 450°C. The high-frequency radio-frequency (RF) power is typically in the range of about 50 to 700 watts per showerhead, and the low frequency RF power is typically in the range of about 50 to 500 watts per showerhead. The final deposition thickness is preferably in the range of about 10 to 100 nm, and most preferably in the range of about 25 to 70 nm. This silicon nitride hardmask film

preferably has a composition of about 30 to 45 atomic % silicon, about 30 to 55 atomic % nitrogen, and about 10 to 25 atomic % hydrogen. Most preferably, this silicon nitride hardmask film has a composition of about 41 atomic % silicon, about 41 atomic % nitrogen, and about 17.5 atomic % hydrogen.

In another preferred embodiment, a silicon carbide hardmask layer (113) is deposited in a CVD reactor at a pressure of about 0.1 to 20 torr, most preferably in the range of about 1 to 10 torr, using a combination of gases that may include, but are not limited to, SiH_4, NH_3, N_2, He, trimethylsilane (3MS), and/or tetramethylsilane (4MS). A typical deposition process uses a flow of 3MS in the range of about 50 to 500 sccm and a flow of He in the range of about 50 to 2000 sccm. The deposition temperature is typically within the range of about 150 to 500°C, most preferably in the range of about 300 to 400°C. The RF power is typically in the range of about 150 to 700 watts per showerhead, most preferably in the range of about 100 to 500 watts per showerhead. The final deposition thickness is preferably in the range of about 10 to 100 nm, and most preferably in the range of about 25 to 70 nm. This amorphous hydrogenated silicon carbide hardmask film preferably has a composition of about 27 atomic % silicon, about 36 atomic % carbon and about 37 atomic % hydrogen.

Hardmask layer (113) may function as a patterning layer to assist in later etching of ILD layer (112) to form a trench for conductor (115). Hardmask layer (113) may also serve as a polish stop layer during a subsequent CMP step to remove excess metal.

Following deposition of a silicon nitride or silicon carbide hardmask film, as described above, additional sacrificial hardmask layers (not shown) may be deposited. For example, a series of hardmask layers may be deposited, such as the hardmask layers described in co-pending U.S. Patent Application Ser. No. 09/550,943, filed April 14, 2000 and titled "Protective Hardmask for Producing Interconnect Structures," the disclosure of which is incorporated herein by reference. Alternatively, an additional silicon nitride film may be deposited, followed by a silicon oxide deposition. In one preferred embodiment, an additional silicon nitride hardmask film is deposited in a CVD reactor at a pressure in the

range of about 0.1 to 10 torr, most preferably in the range of about 1 to 5 torr, using a combination of gases that may include, but are not limited to, SiH_4, NH_3, N_2 and/or He. A typical deposition process uses a flow of SiH_4 in the range of about 100 to 700 sccm, a flow of NH_3 in the range of about 100 to 5000 sccm, and a flow of N_2 in the range of about 100 to 5000 sccm. The deposition temperature is typically within the range of about 150 to 500°C, most preferably in the range of about 350 to 450°C. The high frequency RF power is typically in the range of about 50 to 700 watts per showerhead, and the low frequency RF power is typically in the range of about 50 to 500 watts per showerhead. The final deposition thickness is preferably in the range of about 10 to 100 nm, most preferably in the range of about 25 to 60 nm. This additional silicon nitride hardmask film preferably has a composition of about 41 atomic % silicon, about 41 atomic % nitrogen, and about 17.5 atomic % hydrogen.

The subsequent silicon oxide hardmask layer is deposited in a CVD reactor at a pressure in the range of about 0.1 to 10 torr, most preferably in the range of about 1 to 5 torr, using a combination of gases that may include, but are not limited to, SiH_4, N_2O, N_2, and O_2. A typical deposition uses a flow of SiH_4 in the range of about 10 to 700 sccm, a flow of N_2O in the range of about 100 to 20000 sccm, and a flow of N_2 in the range of about 100 to 3000 sccm. The deposition temperature is typically in the range of about 150 to 500°C, most preferably in the range of about 350 to 450°C. RF power is typically in the range of about 150 to 500 watts per showerhead, most preferably in the range of about 50 to 3000 watts per showerhead. The final deposition thickness is preferably in the range of about 30 to 250 nm, most preferably in the range of about 50 to 200 nm. This additional silicon oxide hardmask layer preferably has a composition of about 33 atomic % silicon, about 63 atomic % oxygen, and less than about 1 atomic % hydrogen.

In Figure 3(b), at least one trench (115*a*) is formed using a conventional photolithography patterning and etching process. In a typical photolithography process, a photoresist material (not shown) is deposited on hardmask layer (113). The photolithography material is exposed to ultraviolet (UV) radiation through a mask, and then the photoresist material is developed. Depending on the type of

photoresist material used, exposed portions of the photoresist may be rendered either soluble or insoluble during development. These soluble portions of the photoresist are then removed, leaving behind a photoresist pattern matching the desired pattern of trenches. Trench (115*a*) is then formed by removing hardmask layer (113) and a portion of ILD layer (112) by, for example, reactive ion etching (RIE), in areas not protected by the photoresist. Hardmask layer (113) may assist in this etching step as follows. Hardmask layer (113) may be etched first in areas not covered by the photoresist, then the photoresist may be removed, leaving behind a patterned hardmask layer (113) matching the photoresist pattern. Then, ILD layer (112) may be etched in areas not covered by hardmask layer (113).

Following formation of trench (115*a*), the trench is preferably lined with diffusion barrier liner (114), and then a conductive material is deposited in trench (115*a*) to form conductor (115). Diffusion barrier liner (114) may be deposited by any suitable method, such as by physical vapor deposition (PVD), chemical vapor deposition (CVD) or ionized physical vapor deposition (I-PVD). Conductive material (115) may deposited in trench (115*a*) by any suitable method, such as by plating technology. Excess liner (114) and conductive material (115) may be removed in a CMP process, in which the top surface of conductor (115) is made coplanar with the top surface of hardmask layer (113). Hardmask layer (113) may serve as a polish-stop layer during this CMP step, thereby protecting ILD layer (112) from damage during polishing. Sacrificial hardmask layers (not shown) may also be removed during this CMP step.

First cap layer (116) is then deposited on conductor (115) and hardmask layer (113), as shown in Figure 3(d). First cap layer (116) is preferably deposited by a HDP CVD process, but may be deposited by other processes such as by PVD, PE CVD, or spin-on techniques. First cap layer (116) may be formed of silicon nitride, silicon carbide, boron nitride or other suitable dielectric material.

Most preferably, first cap layer (116) is a HDP CVD silicon nitride film deposited in a CVD reactor at a pressure in the range of about 0.1 to 50 milli-torr, most preferably at a pressure in the range of about 5 to 20 milli-torr. The deposition gases may include, but are not limited to, SiH_4, N_2, and Ar or He. A

typical deposition uses a flow of SiH_4 in the range of about 5 to 125 sccm, a flow of N_2 in the range of about 50 to 1000 sccm, and a flow of Ar in the range of about 20 to 1000 sccm. The deposition temperature is typically in the range of about 200 to 500°C, with a range of about 300 to 450°C most preferred. Radiofrequency (RF) power is typically in the range of about 1700 to 2500 watts per showerhead, and most preferably in the range of about 1750 to 1950 watts per showerhead. The final deposition thickness is preferably in the range of about 25 to 700 Å, and most preferably in the range of about 50 to 350 Å. This HDP silicon nitride cap layer preferably has a composition of about 30 to 50 atomic % silicon, about 40 to 65 atomic % nitrogen, and about 5 to 13 atomic % hydrogen, most preferably about 40 atomic % silicon, about 52 atomic % nitrogen, and about 8 atomic % hydrogen.

Following deposition of first cap layer (116), a second cap layer (117) is deposited, as shown in Figure 3(e). Second cap layer (117) is preferably deposited by a PE CVD process, but may also be deposited by a physical vapor deposition (PVD) process, by a spin-on process, or even by a HDP CVD process using process parameters different from those used for the first cap layer. Second cap layer (117) may be formed of silicon nitride, silicon carbide, boron nitride or other suitable dielectric. These PE CVD films may be either hydrogenous or amorphous or both. While it is most preferred that deposition of second cap layer (117) occurs without interruption of the vacuum environment of the first cap layer (116) deposition and without exposing the substrate to atmospheric pressure, it is possible for the second cap layer deposition to occur with a vacuum interruption after the first cap layer (116) deposition.

In a most preferred embodiment, second cap layer (117) is a PE CVD silicon nitride layer, and is deposited in a CVD reactor at a pressure in the range of about 0.1 to 10 torr, most preferably in the range of about 1 to 7 torr, using a combination of gases that may include, but are not limited to, SiH_4, NH_3, N_2 and He. A typical deposition uses a flow of SiH_4 in the range of about 10 to 500 sccm, a flow of NH_3 in the range of about 100 to 3000 sccm, and a flow of N_2 in the range of about 500 to 25000 sccm. The deposition temperature is typically in the range of about 150 to 500°C, most preferably in the range of about 350 and 450°C.

The high frequency RF power is typically in the range of about 25 to 700 watts per showerhead, most preferably in the range of about 50 to 250 watts per showerhead. The low frequency RF power is typically in the range of about 0 to 500 watts per showerhead. The final deposition thickness is preferably in the range of about 100 to 1000 Å, and most preferably in the range of about 250 to 700 Å. This PE CVD silicon nitride cap layer preferably has a composition of about 30 to 45 atomic % silicon, about 40 to 65 atomic % nitrogen, and about 10 to 25 atomic % hydrogen. A particularly preferred composition for second cap layer (117) is about 37 atomic % silicon, about 48 atomic % nitrogen, and about 15 atomic % hydrogen.

In another preferred embodiment, second cap layer (117) is a PE CVD amorphous hydrogenated silicon carbide layer, and is deposited in a CVD reactor at a pressure in the range of about 0.1 to 20 torr, most preferably in the range of about 1 to 10 torr, using a combination of gases that may include, but is not limited to, SiH_4, NH_3, N_2, He, trimethylsilane (3MS), or tetramethylsilane (4MS). A typical deposition uses a flow of 3MS in the range of about 50 to 500 sccm, and a flow of He in the range of about 50 to 2000 sccm. The deposition temperature is typically in the range of about 150 to 500°C, most preferably in the range of about 300 to 400°C. The RF power is typically in the range of about 150 to 700 watts per showerhead, most preferably in the range of about 100 to 500 watts per showerhead. The final deposition thickness is preferably in the range of about 100 to 1000 Å, and most preferably in the range of about 250 to 700 Å. This amorphous hydrogenated silicon carbide film preferably has a composition of about 20 to 40 atomic % silicon, about 20 to 50 atomic % carbon, and about 20 to 45 atomic % hydrogen, most preferably about 27 atomic % silicon, about 36 atomic % carbon, and about 37 atomic % hydrogen.

In yet another preferred embodiment, second cap layer (117) is a PE CVD amorphous hydrogenated nitrogenated silicon carbide layer, and is deposited in a CVD reactor at a pressure in the range of about 0.1 to 20 torr, most preferably in the range of about 1 to 10 torr, using a combination of gases that may include, but is not limited to, SiH_4, NH_3, N_2, He, 3MS, 4MS and other methyl silanes. This second cap layer (117) is preferably deposited using 3MS or 4MS at a flow rate in

the range of about 50 to 500 sccm, and N_2 at a flow rate in the range of about 50 to 500 sccm. The deposition temperature is preferably in the range of about 150 to 500°C, most preferably in the range of about 300 to 400°C. The RF power is preferably in the range of about 100 to 700 watts per showerhead, most preferably in the range of about 200 to 500 watts. The final deposition thickness is preferably in the range of about 100 to 1000 Å, and most preferably in the range of about 250 to 700 Å. This amorphous hydrogenated nitrogenated silicon carbide film preferably has a composition of about 20 to 34 atomic % silicon, about 12 to 34 atomic % carbon, about 5 to 30 atomic % nitrogen and about 20 to 50 atomic % hydrogen, most preferably about 22 to 30 atomic % silicon, about 15 to 30 atomic % carbon, about 10 to 22 atomic % nitrogen and about 30 to 45 atomic % hydrogen.

Second cap layer (117) may be formed of a series of thin PE CVD films, where the total thickness is in the range of about 100 to 1000 Å. These thin PE CVD films may be formed of the same material, such as silicon nitride, or they may be formed of different or alternating materials, such as silicon nitride, silicon carbide, silicon oxide, silicon oxycarbide and/or silicon oxycarbonitride. As discussed previously, second cap layer (117) may comprise alternating films of different material or a series of films of the same material together with films of a different material.

Prior to deposition of first cap layer (116), a plasma pre-cleaning step may be performed in the CVD reactor. A typical plasma pre-cleaning step uses a source of hydrogen such as NH_3 or H_2 at a flow rate in the range of about 50 to 700 sccm, and is performed at a substrate temperature in the range of about 15 to 500°C, most preferably at a substrate temperature in the range of about 20 to 400°C, for a time of about 5 to 500 seconds and most preferably about 10 to 100 seconds. The RF power is in the range of about 100 to 10,000 watts, and most preferably in the range of about 1000 to 5000 watts during this cleaning step. Optionally, other gases such as He, argon (Ar) or N_2 may be added at a flow rate in the range of about 50 to 20,000 sccm.

Figures 3(a)-3(e) illustrate the formation of the first interconnect level, which consists of adhesion promoter layer (111), ILD layer (112), hardmask layer (113), diffusion barrier liner (114), conductor (115), first cap layer (116), and second cap layer (117). In Figure 3(f), the formation of the second interconnect level begins with deposition of adhesion promoter layer (118), ILD layer (119) and hardmask layer (120). Adhesion promoter layer (118) may be deposited using the same method as that for adhesion promoter layer (111). Likewise, ILD layer (119) may be deposited using the same method as that for ILD layer (112), and hardmask layer (120) may be deposited using the same method as that for hardmask layer (113). Additional sacrificial hardmask layers (not shown) may be deposited on primary hardmask layer (120).

Figures 3(g) and 3(h) illustrate the formation of via (122*a*) and trench (122*b*). First, at least one via (122*a*) may be formed in hardmask layer (120), ILD layer (119), adhesion promoter layer (118) and cap layers (117) and (116), using a conventional photolithography patterning and etching process, as shown in Figure 3(g). Then, at least one trench (122*b*) may be formed in hardmask layer (120) and a portion of ILD layer (119), using a conventional photolithography process, as shown in Figure 3(h). Via (122*a*) and trench (122*b*) may be formed using the same photolithography process as that used to form trench (115*a*).

Alternatively, via (122*a*) and trench (122*b*) may be formed by first patterning and etching a trench in hardmask layer (120) and ILD layer (119), where the trench has a depth equal to the depth of trench (122*b*), but has a length equal to the length of trench (122*b*) and the width of via (122*a*) combined. Then via (122*a*) may then be formed by etching through the remainder of ILD layer (119), adhesion promoter layer (118) and cap layers (117) and (116).

Following formation of via (122*a*) and trench (122*b*), the via and trench are preferably lined with diffusion barrier liner (121), and then a conductive material is deposited in the via and trench to form conductor (122), as shown in Figure 3(i). Diffusion barrier liner (121) may be deposited by the same method used for diffusion barrier liner (114), and conductive material (122) may deposited by the same method used for conductor (115). Excess liner (121) and conductive material

(122) may be removed in a CMP process, in which the top surface of conductor (122) is made coplanar with the top surface of hardmask layer (120). Sacrificial hardmask layers (not shown) may also be removed during this CMP step. Hardmask layer (120) may serve as a polish-stop layer during this CMP step, thereby protecting ILD layer (119) from damage during polishing.

Cap layers (123) and (124) are then deposited on conductor (122) and hardmask layer (120), as shown in Figure 3(j). First cap layer (123) may be deposited using the same process as that for first cap layer (116), and second cap layer (124) may be deposited using the same process as that for second cap layer (117).

While the present invention has been particularly described in conjunction with a specific preferred embodiment and other alternative embodiments, it is evident that numerous alternatives, modifications and variations will be apparent to those skilled in the art in light of the foregoing description. It is therefore intended that the appended claims embrace all such alternatives, modifications and variations as falling within the true scope and spirit of the present invention.

Industrial Applicability

The present invention is useful in the manufacture of high speed semiconductor microprocessors, application specific integrated circuits (ASICs), and other high speed integrated circuit devices. More particularly, the bilayer cap of this invention is useful in advanced back-end-of-line (BEOL) interconnect structures for semiconductor devices using low-k dielectric materials.

Claims

1. An interconnect structure formed on a substrate (110), the structure comprising:

a dielectric layer (112, 119) overlying the substrate (110);

a hardmask layer (113, 120) on said dielectric layer (112, 119), said hardmask layer (113, 120) having a top surface;

at least one conductor (115, 122) embedded in said dielectric layer (112, 119) and having a top surface coplanar with the top surface of said hardmask layer (113, 120);

a first cap layer (116, 123) on said at least one conductor (115, 122) and on said hardmask layer (113, 120); and

at least one second cap layer (117, 124) on said first cap layer (116, 123).

2. The interconnect structure according to Claim 1, wherein said first cap layer (116, 123) is formed by a high density plasma chemical vapor deposition (HDP CVD) process, and said second cap layer (117, 124) is formed by a plasma-enhanced chemical vapor deposition (PE CVD) process.

3. The interconnect structure according to Claim 1, further comprising a conductive liner (114, 121) disposed between said conductor (115, 122) and said dielectric layer (112, 119).

4. The interconnect structure according to Claim 1, further comprising an adhesion promoter layer (111, 118) disposed between said dielectric layer (112, 119) and the substrate (110).

5. The interconnect structure according to Claim 1, wherein said dielectric layer (112, 119) comprises an organic thermoset polymer having a dielectric constant of about 1.8 to about 3.5.

6. The interconnect structure according to Claim 5, wherein said dielectric layer (112, 119) comprises a polyarylene ether polymer.

7. The interconnect structure according to Claim 1, wherein said first cap layer (116, 123) comprises a dielectric material selected from the group consisting of silicon nitride, silicon carbide and boron nitride.

8. The interconnect structure according to Claim 1, wherein said first cap layer (116, 123) comprises silicon nitride having a composition of about 40 atomic % silicon, about 52 atomic % nitrogen, and about 8 atomic % hydrogen.

9. The interconnect structure according to Claim 1, wherein said second cap layer (117, 124) comprises a dielectric material selected from the group consisting of silicon nitride, silicon carbide and boron nitride.

10. The interconnect structure according to Claim 1, wherein said second cap layer (117, 124) comprises silicon nitride having a composition of about 37 atomic % silicon, about 48 atomic % nitrogen, and about 15 atomic % hydrogen.

11. The interconnect structure according to Claim 1, wherein said second cap layer (117, 124) comprises silicon carbide having a composition of about 27 atomic % silicon, about 36 atomic % carbon, and about 37 atomic % hydrogen.

12. The interconnect structure according to Claim 1, wherein said second cap layer (117, 124) comprises amorphous hydrogenated nitrogenated silicon carbide having a composition of about 22 to 30 atomic % silicon, about 15 to 30 atomic % carbon, about 10 to 22 atomic % nitrogen and about 30 to 45 atomic % hydrogen.

13. The interconnect structure according to Claim 1, wherein said conductor (115, 122) comprises copper.

14. The interconnect structure according to Claim 1, wherein said second cap layer (117, 124) comprises a plurality of thin films each formed by a plasma-enhanced chemical vapor deposition (PE CVD) process.

15. The interconnect structure according to Claim 14, wherein the plurality of thin films comprises at least one silicon nitride film and at least one film selected from the group consisting of silicon oxide, silicon carbide, boron nitride, silicon oxycarbide and silicon oxycarbonitride.

16. The interconnect structure according to Claim 1, wherein said dielectric layer (112, 119) comprises silicon oxide.

17. A method for forming an interconnect structure on a substrate (110), the method comprising the steps of:

depositing a dielectric material on the substrate (110), thereby forming a dielectric layer (112, 119);

depositing a hardmask material on said dielectric layer (112, 119), thereby forming a hardmask layer (113, 120), said hardmask layer (113, 120) having a top surface;

forming at least one opening (115*a*, 122*a*, 122*b*) in said dielectric layer (112, 119);

filling said opening (115*a*, 122*a*, 122*b*) with a conductive material, thereby forming at least one conductor (115, 122), said conductor (115, 122) having a top surface coplanar with the top surface of said hardmask layer (113, 120);

depositing a first material on said conductor (115, 122), thereby forming a first cap layer (116, 123); and

depositing a second material on said first cap layer (116, 123), thereby forming a second cap layer (117, 124).

18. The method according to Claim 17, wherein said first material is deposited by a high density plasma chemical vapor deposition (HDP CVD) process, and said second material is deposited by a plasma-enhanced chemical vapor deposition (PE CVD) process.

19. The method according to Claim 18, wherein said first material is silicon nitride, and said HDP CVD process includes placing the substrate into a reactor chamber at a pressure of about 0.1 milli-torr to about 50 milli-torr and at a temperature of about 200°C to about 500°C, and exposing the substrate to at least one gas selected from the group consisting of silane, nitrogen, argon and helium.

20. The method according to Claim 18, wherein said second material is silicon nitride, and said PE CVD process includes placing the substrate into a reactor chamber at a pressure of about 0.1 torr to about 10 torr and a temperature of about 150°C to about 500°C, and exposing the substrate to at least one gas selected from the group consisting silane, ammonia, nitrogen and helium.

21. The method according to Claim 17, wherein said first material is deposited by a HDP CVD process under vacuum and said second material is deposited by a PE CVD process under vacuum, without exposing the substrate to atomospheric pressure prior to deposition of said second material.

22. The method according to Claim 17, further comprising, after formation of said conductor (115, 122) and prior to deposition of said first material, the step of:

performing a plasma pre-cleaning process which includes heating the substrate to a temperature of about 150°C to about 500°C and exposing the substrate to a source of hydrogen for a time of about 5 to about 500 seconds.