

PATENT SPECIFICATION

DRAWINGS ATTACHED

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COMPLETE SPECIFICATION

Semiconductor Devices

We, TEXAS INSTRUMENTS INCORPORATED, a Corporation organized according to the laws of the State of Delaware, United States of America, of 13500 North Central Expressway, Dallas, Texas, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to semiconductor devices, and more particularly to an electrode arrangement for reducing the effects of surface inversion in semiconductor devices.

A problem long existing in semiconductor technology is the degradation of back biased p-n junctions in devices subjected to high operating temperatures. The major contributing factor to this degradation is surface inversion, a tendency for the semiconductor material at the surface to invert from one conductivity type to the opposite type. This effect is especially prevalent in p-type silicon having a silicon oxide layer thereon, the surface tending to invert to n-type. Also, since the collector-base junction of a transistor is heavily reverse biased, and the collector region of a transistor usually doped more lightly than the base and emitter, the detrimental effects of surface inversion are most noticeable in the collector-base characteristics of p-n-p silicon planar transistors. Inversion is reduced by doping the p-type collector region more heavily, but this limits the transistor to low collector-base breakdown voltages. A partial solution to the inversion problem is provided by employing high resistivity p-type material for the collector, then forming a heavily-doped p+ region near the wafer surface in the collector region surrounding but spaced from the base region. In this

construction, the p+ region is referred to as a "guard ring", although in many cases the region is not ring-shaped or circular but instead is square or rectangular, but in any event is of closed configuration. The guard ring retards degradation due to surface inversion, but yet permits the collector region to be of high resistivity so that the back breakdown voltage can be high.

Although it has been found that the guard ring construction is quite effective on conventional transistors, its effectiveness is lost when metallic strips are placed over the silicon oxide layer which covers the surface of the device, this arrangement being necessary in integrated circuits for interconnections and in expanded contact transistors. The conductive strip, if biased heavily positive with respect to the underlying semiconductor material, enhances the inversion layer at the surface, producing a heavy concentration of electrons (n-type carriers) in the silicon just beneath the strip. Thus, in effect, an n+ region is formed, and where the n+ region adjoins the p+ guard ring region, a p+ to n+ junction results. Such a junction inherently exhibits a very low back breakdown, acting virtually as a short circuit.

Accordingly, it is an object of this invention to reduce the effects of surface inversion in semiconductor devices.

The present invention is a semiconductor device comprising a semiconductor body having a region of a first conductivity type formed adjacent one surface thereof, the material of the semiconductor body adjacent said region being of a second conductivity type, an electrode making electrical contact with the material of the semiconductor body adjacent said region, said electrode having a closed configuration surrounding said region in spaced apart relationship there-

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from and comprising a portion in ohmic contact with said material of the body adjacent said region, and a shield portion extending inwardly from the contact portion toward said region, and spaced from the surface, said electrode serving to counteract the effects of surface inversion in the device.

The present invention is also a method of making a semiconductor device including the steps of:

- (a) diffusing impurities into one face of a semiconductor body using a silicon oxide coating as a mask to form a region in said one face of conductivity type opposite that of the subjacent semiconductor material,
- (b) forming an opening in the silicon oxide coating on said one face which defines a closed configuration surrounding but spaced from said region,
- (c) selectively applying a metal film to said one face to adhere to the silicon surface in said opening and to extend inwardly towards said region over the oxide coating transverse to the opening,
- (d) applying another silicon oxide coating to said one face over the metal film,
- (e) forming an opening in the oxide coating above said region, and
- (f) applying a conductive metal strip over the oxide coating, the strip extending across but being insulated from the metal film, the strip engaging said region in the opening thereover.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, wherein:

Figure 1 is a pictorial view in section of a transistor and is used herein for explaining the principles of the invention;

Figure 2 is an enlarged sectional view of a portion of the transistor of Figure 1;

Figure 3 is a pictorial view in section of a transistor employing the field relief electrode of this invention;

Figure 4 is an enlarged sectional view of a portion of the transistor of Figure 3;

Figures 5 to 8 are sectional views of the transistor of Figures 3 and 4 in successive stages of manufacture;

Figure 9 is a schematic representation, partly in section, of apparatus used in making the transistor of Figures 3 and 4; and

Figures 10, 11, 12 and 13 are pictorial views in section of other embodiments of the invention.

With reference to Figure 1, a p-n-p planar epitaxial transistor is shown which is of the type employing a guard ring to counteract the effects of surface inversion. This transistor includes a silicon wafer 10 having a heavily doped p-type substrate 11 and a lightly doped p-type epitaxial layer 12. An n-type base region 13 is formed in the

central part of the epitaxial layer 12, and a small circular p-type emitter region 14 is formed in the base region in an off-set manner to provide room for a base contact. The base and emitter regions are usually created by successive diffusion operations using silicon oxide masking as set forth in U.S. Patent No. 3,122,817 to Jules Andrus. The silicon oxide formed for masking and during impurity deposition operations remains on the top surface of the wafer 10 as a silicon oxide coating 15 which is seen to be in a stepped configuration of differing thicknesses due to the successive removal of oxide to form the various regions. Various surface effects, including the presence of this oxide coating 15, tend to cause the subjacent surface of the p-type region 12 to invert to n-type, i.e., to form a thin surface-adjacent layer in the silicon, the layer containing an excess of free carriers in the form of electrons. Thus, in accordance with the teaching of U.S. Patent No. 3,197,681, a heavily doped p-type annular region 16 is formed in the top surface of the wafer. This region 16 may be formed at the same time as the emitter diffusion. The base and emitter contacts to this transistor are provided by metal strips 17 and 18 which extend into holes etched in the oxide coating 15 to make ohmic connection to the appropriate regions. The strips terminate in enlarged bonding pads 19 and 20. This expanded contact arrangement is necessary in high frequency devices because of the extreme small size of the active regions, the emitter being only a few hundredths of a square mil in area in some cases. If the contacts are no larger than the active regions in such cases, it is virtually impossible to bond lead wires thereto, and so the expanded contacts with enlarged bonding pads are needed. The transistor of Figure 1 is completed by securing the substrate 11 down to a metal electrode, such as a header, with contact metal 21 to provide the collector electrode, and then bonding lead wires from the pads 19 and 20 to suitable base and emitter electrodes.

In operation of the transistor of Figure 1, bias voltages are applied between the base and collector and between the emitter and collector, often at elevated temperatures. These factors result in breakdown or shorting of the device, rendering it useless except at low operating bias levels and/or low temperatures. This breakdown is caused by what occurs in the region closely adjacent the annular region 16, which will now be examined in detail. With reference to Figure 2, an enlarged view of a portion of Figure 1 beneath the expanded base contact 17, it will be noted that a shallow channel 23 is created beneath the oxide coating

15. This channel or inversion layer has a fairly high concentration of carriers, electrons in this case, and so may be considered to be n-type. Heavily doped p-type silicon is not as easily inverted to n-type, however, so the annular region 16 prevents failure because the channel 23 is not continuous from the base to collector. This structure is effective so long as expanded contacts are not used.

The metal strip 17 extending from the base 13 across portions of the collector region sets up an electric field E in the dielectric and at the silicon surface due to the collector-base bias. This field increases the free carrier concentration in the channel 23, forming in effect an n^+ region. The junction between the annular region 16 and the channel 23, particularly that portion 24 which is reverse biased, is now very easy to break down since it has a high carrier concentration on both sides. The adverse effects of the expanded contacts are made worse by the presence of heat, which not only tends to increase the inversion in the silicon surface, but also may create a permanent electric field in the dielectric due to the electret effect.

In accordance with the present invention, reverse breakdown due to the effects discussed above is prevented by shielding the critical area adjacent the annular region from the electric field. As will be seen in Figure 3, this shielding is accomplished by an additional electrode beneath the expanded leads.

Figure 3 shows a p-n-p epitaxial planar transistor similar to Fig. 1 but using an electrode of this invention referred to hereinafter as a field relief electrode. As above, the transistor comprises a silicon wafer 30 having a heavily-doped substrate 31 and a lightly doped p-type epitaxial layer 32. Formed in the epitaxial layer is a diffused n-type base region 33 and a diffused p-type emitter region 34. A heavily-doped p-type region 36 surrounds the base region at the top surface of the wafer to reduce the undesirable effects of surface inversion. Two different coatings of silicon oxide exist on the top surface of the wafer. The first of these is a coating 37 of thermal oxide which is used as a diffusion mask in forming the base, emitter and annular regions. This coating 37 is in a stepped configuration due to the several stages of oxide formation and removal and impurity deposition. In addition to the thermal oxide, a coating 38, of pyrolytically deposited silicon oxide is provided on the top surface of the wafer. This coating 38 serves to insulate the expanded contacts from the field relief electrode. Electrical connections to the base and emitter regions are provided by metal strips 39 and 40 which engage the silicon surface in holes etched through the oxide layers, then

extend out over the oxide to bonding pads 41 and 42. Surrounding the inner edge of the heavily-doped region 36 is a field relief electrode 43 which is the principal feature of this invention. The electrode is ohmically connected at its outer periphery to the region 36 through an opening etched in the oxide layer 37, and from there extends inwardly over top of the thermal oxide coating 37. The electrode 43 is electrically insulated from the expanded leads 39 and 40 by the pyrolytically deposited oxide coating 38. As may best be seen in the enlarged view of Figure 4, the critical area 44 just inside the innermost part of the region 36 is shielded from the electric field E which results when the collector-base is reverse biased, i.e., when a positive voltage is applied between the strip 39 and the collector region 31, 32. While some inversion will occur due to the presence of silicon oxide, the effect of the electric field is eliminated. Accordingly, in combination with the advantages of the guard ring 36, the field relief electrode provides a marked improvement in breakdown voltage at elevated temperature.

A method of manufacturing the device of Figures 3 and 4 will now be described. With reference to Figure 5, the starting material is the substrate 31, a wafer perhaps thirty mils square, which is at this point merely an individual segment of a large slice of monocrystalline p-type silicon about one inch in diameter and 10 mils thick. A layer 32 of higher resistivity p-type material is epitaxially grown upon the top surface of the substrate, then the initial oxide coating is formed over the epitaxial layer and an opening 46 made therein by photoresist masking and etching techniques. The slice including the wafer 30 is then subjected to an n-type diffusion operation wherein a donor impurity such as phosphorus is diffused into the top of the epitaxial region 32 to form the base region 33, while at the same time silicon oxide reforms over the opening 46. Referring now to Figure 6, a smaller opening 47 is made in the regrown part of the oxide coating 37, and a peripheral opening 48 is also made, both of these being cut in the same photoresist masking and etching operation. The slice is then subjected to a p-type diffusion operation during which boron or other acceptor impurity is diffused into the top surface through the openings and oxide is reformed, creating the emitter region 34 and the peripheral guard ring region 36 as seen in Figure 7. The device is now ready for forming the field relief electrode thereon. To this end, a peripheral opening 49 is made in the oxide coating 37, and a film of conductive metal such as molybdenum or chromium is deposited over the entire top

surface of the wafer or slice. In the opening 49 the metal adheres to the silicon surface and makes ohmic contact thereto. The metal used for this electrode must be fairly nonreactive with silicon or silicon oxide at the temperatures used in the subsequent oxide deposition. The metal film is removed in unwanted areas by a photoresist operation, leaving only the field relief electrode 43 surrounding the transistor base region on the top face of the wafer. Expanded contacts must now be made to the base and emitter regions, and since these must pass over the electrode 43 some provision must be made for insulation. Accordingly, the layer 38 of silicon oxide is applied, preferably by deposition at low temperature from a vapour of an oxysilane compound in the presence of oxygen. Apparatus for carrying out this preferred method of oxide deposition is illustrated in Figure 9, where a tube furnace 50 is shown having a heater 51 for maintaining the temperature therein at perhaps 500°C. A plurality of slices are placed in a boat 52 within the furnace, each slice of silicon containing many of the wafers 30 in undivided form. The reaction gases are introduced into the furnace by an arrangement including a conduit 53 through which oxygen is forced at about one cubic foot per minute. The gas bubbles through a quantity of liquid tetraethylorthosilicate 54 in a flask 55, where vapour of the oxysilane is entrained, then the gaseous mixture passes into the furnace through a conduit 56. Additional oxygen gas is introduced into the stream by a conduit 57 at a rate of about one cubic foot per minute. With this apparatus, the silicon oxide layer 38 can be deposited at a rate of 2000 Å per hour, with a thickness of about 4000 Å being adequate for insulation purposes. Following the deposition of the oxide coating 38, openings 58 and 59 are made in the oxide over the base and emitter regions to expose the silicon surface for the purpose of making ohmic connections to these regions of the transistor. A film of contact metal is then evaporated over the entire top surface in such a manner that the metal adheres and makes nonrectifying contact to the silicon surface in the openings 58 and 59. Thereafter, unwanted metal is removed to leave the desired contact and expanded lead pattern including the strips 39 and 40 and bonding pads 41 and 42 as seen in Figure 3. The slice of silicon with a large number of the devices of Figure 3 formed therein is now scribed and broken into individual wafers 30, which may then be mounted on transistor headers in accordance with standard practice. At this point a collector contact 60 is provided, the contact member representing either the solder used

to secure the wafer to the header, a metal header itself, or a metallized area on a ceramic transistor package. Connections are then made to the base and emitter bonding pads 41 and 42 by small gold wires which extend to suitable posts or electrodes in the header, and the encapsulation is completed by securing a can or other closure to the header.

The field relief electrode of this invention may be utilized in a semiconductor integrated circuit device of the type illustrated in Figure 10. This device comprises a wafer 64 of monocrystalline n-type silicon having a transistor and a resistor formed therein, the transistor including a p-type collector region 65, an n-type base region 66, and a p-type emitter region 67 while the resistor includes a p-type isolating region 68 and an n-type region 69 which forms the resistor itself. Of course, the same wafer would ordinarily include many more transistors and resistors, as well as other circuit components such as diodes and capacitors, only two components being shown to illustrate the principle. The transistor and resistor are electrically isolated from one another by p-n junctions in the wafer, the collector region 65 being separated from the resistor 69 by three such junctions between regions 65, 64, 68 and 69. However, isolation between components, as well as isolation between a component and the wafer or substrate 64 which is usually grounded, can be lost by the formation of a surface inversion layer just as in the case of a transistor as discussed above. To reduce inversion, the p-type regions have formed therein annular heavily-doped p+ regions 70 and 71. This alone may prove to be inadequate, however, because of the expanded contacts and interconnections as will be discussed below. The wafer 64 has a silicon oxide coating 72 covering the top surface thereof, except where ohmic contacts are made, and this coating will be in various thicknesses due to the process used to form the transistor and resistor regions, i.e., successive depositions and diffusions with oxide masking. Annular openings are made in the oxide coating 72 over the p+ regions 70 and 71, and contact metal is selectively applied to form field relief electrodes 73 and 74. An oxide coating 75 is deposited over the field relief electrodes 73 and 74 to insulate these electrodes from the leads which cross over. This coating 75 is formed at a relatively low temperature by the oxidative deposition technique discussed above with reference to Figure 9. Openings are cut through both oxide layers 72 and 75 in the areas where contact is to be made, then metal is selectively applied over the oxide and in the openings to provide a conductive strip 76 for a connection to the transistor

emitter, a strip 77 for the collector connection, a strip 78 for an interconnection between the transistor base and one end of the resistor 69, and a strip 79 for a connection to the other end of the resistor.

In operation of the device of Figure 10, several bias conditions could be present which would tend to destroy isolation between the components due to shorting through an inversion layer. For example, if the strip 78 is positive with respect to the substrate 64, there would be a tendency for the left end of the resistor 69 to short out to the substrate due to inversion beneath the strip were the electrode 74 not present. Likewise, under these conditions the base of the transistor may tend to short to the substrate. Also, if the lead 78 is positive with respect to the collector region 65 but negative with respect to the substrate, shorting would be in the other direction, i.e., from the substrate to the base region 66. For this reason, the field relief electrodes 73 and 74 extend in both directions from the point of contact with the silicon surface.

In an integrated circuit employing a p-type substrate 80 and n-p-n transistors as seen in Figure 11, a field relief electrode 81 would surround the collector region 82 over a heavily-doped annular region 83. This same electrode may surround other adjacent components such as a resistor 84. As above, conductive strips over pyrolytically deposited oxide make connections to the regions of the transistor and resistor, and interconnections between components.

Many epitaxial type semiconductor devices employ a p-type substrate with an n-type epitaxial layer in which components are formed by diffusion. In an integrated circuit of this type, an example of which is illustrated in Figure 12, the n-type epitaxial layer 91 would function as the collector of n-p-n transistors 92 and 93, with the base and emitter being diffused therein. To isolate the collector regions of transistors 92 and 93 in the integrated circuit, a p+ isolation diffusion forms a grid of heavily-doped regions 94. Even though these regions are of high acceptor concentration, there is a possibility that the surface can invert to n-type under extreme operating conditions, thus destroying isolation between components. Thus, a field relief electrode 95 surrounds each component over the heavily-doped region 94. The field relief electrode 95 engages the silicon surface at the isolation regions 94, then extends over the thermal oxide coating in both directions, overlying part of the n-type region 91 so that inversion of the n-type region is also inhibited. The same inversion problem would occur in other epitaxial devices having expanded contacts, such as an epitaxial base transistor and an

epitaxial channel field-effect transistor. In each case, a field relief electrode is added over the p+ isolation diffusion to prevent shorting due to surface inversion.

The field relief electrode of this invention is effective in reducing surface inversion due to electric fields, and may be used in some cases without the heavily-doped guard ring. Consider the transistor of Figure 3 without the heavy doping of the region 36 but with the electrode 43 in place. The area beneath the guard ring would be shielded from the electric field, and surface inversion would be substantially reduced.

In a semiconductor device using conventional contacts of the nonexpanded type, i.e., not having conductive strips extending over junctions on top of an oxide coating, surface inversion apparently due to an electric field effect also occurs. Improved characteristics can be provided in such a device by the use of the field relief electrode of this invention. With reference to Figure 13 a p-n-p transistor is shown comprising a wafer 100 of p-type silicon forming the transistor collector, an n-type base region 101, and a p-type emitter region 102. An oxide coating 103 covers the top surface and base and emitter contacts 104 and 105 are formed by metal deposited in openings in the oxide. A collector contact 106 engages the back surface of the wafer. When reverse bias is applied between the base and collector, contact 104 being positive with respect to contact 106, an electric field appears to be established vertically through the oxide layer 103 even though no metal strips extend over the oxide. It is believed that this effect is due to ionization of the upper surface of the oxide layer, permitting a positive charge to be built up as electrons flow to the positive contact 104. The surface of the p-type silicon underlying the oxide may be inverted by the corresponding concentration of electrons. This effect is increased with temperature. The oxide layer may become polarized, perhaps by migration of ions, so that the field and inversion layer remain after the reverse bias has been removed and the temperature lowered. The formation of an electric field, and the resultant inversion, may be prevented by the use of a field relief electrode 107 which surrounds the base region but is spaced therefrom. The electrode 107 makes ohmic contact to the surface of the p-type silicon of the collector region, then extends inwardly over top of the oxide layer 103. The presence of the metal electrode on the oxide surface prevents the build up of charge or field, underneath the metal at least, since this part of the top surface of the oxide is shorted to the underlying sili-

con. Thus a channel shorting the base contact to the collector cannot be completed.

The field relief electrode of this invention has utility in semiconductor devices other than the transistors, etc., illustrated above. For example, the reverse characteristics of a diode are distinctly improved by the use of this invention. The base-collector junctions of the transistors described herein may be considered as diodes, ignoring the emitters and emitter contacts.

Primary emphasis has been placed upon the use of the field relief electrode to avoid degradation due to inversion of p-type silicon since this appears to be the situation in which the effect is most troublesome. Inversion of n-type silicon also occurs, however, and so it will be understood that the principles of the invention apply equally well to n-p-n transistors or the like corresponding in structure to the p-n-p devices shown. It may be noted that lightly doped n-type silicon exhibits the inversion effect rather noticeably, but in fairly doped n-type silicon inversion is not ordinarily detected. Consider the transistor of Figure 3, but with the collector regions 31 and 32, and the emitter region 34 being n-type and the base region 33 being p-type. Here the guard ring 36 would be n+ rather than p+. Biasing the base negative with respect to the collector will produce a field beneath the strip 39 which tends to place a positive charge adjacent the silicon surface, thus tending to invert the surface of the n-type collector to p-type. The electrode 43 will prevent this from occurring by eliminating the field just as in the p-n-p arrangement.

Devices constructed using semiconductor materials other than silicon, such as germanium or the III-V compounds, may utilize this invention to advantage in some cases. Silicon has been used as an example because the inversion effect appears most prevalent in this material.

WHAT WE CLAIM IS:

1. A semiconductor device comprising a semiconductor body having a region of a first conductivity type formed adjacent one surface thereof, the material of the semiconductor body adjacent said region being of a second conductivity type, an electrode making electrical contact with the material of the semiconductor body adjacent said region, said electrode having a closed configuration surrounding said region in spaced apart relationship therefrom and comprising a portion in ohmic contact with said material of the body adjacent said region, and a shield portion inwardly extending from the contact portion toward said region and spaced from the

surface, said electrode serving to counteract the effects of surface inversion in the device.

2. A semiconductor device according to claim 1, wherein said region is a part of an electrical component.

3. A semiconductor device according to claim 1 or 2, wherein a first insulating coating covers at least a portion of said surface.

4. A semiconductor device according to Claim 1, wherein said electrode does not extend over the junction between said region and the material of the semiconductor body adjacent said region.

5. A semiconductor device comprising a semiconductor body having a region of a first conductivity type formed adjacent one surface thereof, the material of the semiconductor body adjacent said region being of a second conductivity type, an electrode making electrical contact with the material of the semiconductor body adjacent said region only, said electrode having a closed configuration surrounding said region in spaced relationship therefrom and comprising a portion in ohmic contact with said material of the body adjacent said region, and a shield portion inwardly extending from the contact portion toward said region and spaced from the surface, said electrode serving to counteract the effects of surface inversion in the device.

6. A semiconductor device according to any preceding claim 3 wherein a second insulating coating covers said shield portion.

7. A semiconductor device according to Claim 6, wherein a conductive strip overlies said second insulating coating and the shield portion and makes electrical contact with said region.

8. A semiconductor device according to claim 6, wherein a second region is formed adjacent said surface within said region, which region is of the second conductivity type and wherein conductive strips overlie said second insulating coating and the shield portion and make separate electrical contact with the first and second regions.

9. A semiconductor device according to claim 8, wherein said device is a PNP planar transistor, said semiconductor body is of P-type conductivity, said first region is of N-type conductivity, said second region is of P-type conductivity and said electrode contacts a more heavily doped P+ type conductivity region.

10. A method of making a semiconductor device including the steps of:

(a) diffusing impurities into one face of a semiconductor body using a silicon oxide coating as a mask to form a region in said one face of conductivity type



con. Thus a channel shorting the base contact to the collector cannot be completed.

The field relief electrode of this invention has utility in semiconductor devices other than the transistors, etc., illustrated above. For example, the reverse characteristics of a diode are distinctly improved by the use of this invention. The base-collector junctions of the transistors described herein may be considered as diodes, ignoring the emitters and emitter contacts.

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Devices constructed using semiconductor materials other than silicon, such as germanium or the III-V compounds, may utilize this invention to advantage in some cases. Silicon has been used as an example because the inversion effect appears most prevalent in this material.

WHAT WE CLAIM IS:

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surface, said electrode serving to counteract the effects of surface inversion in the device.

2. A semiconductor device according to claim 1, wherein said region is a part of an electrical component.

3. A semiconductor device according to claim 1 or 2, wherein a first insulating coating covers at least a portion of said surface.

4. A semiconductor device according to Claim 1, wherein said electrode does not extend over the junction between said region and the material of the semiconductor body adjacent said region.

5. A semiconductor device comprising a semiconductor body having a region of a first conductivity type formed adjacent one surface thereof, the material of the semiconductor body adjacent said region being of a second conductivity type, an electrode making electrical contact with the material of the semiconductor body adjacent said region only, said electrode having a closed configuration surrounding said region in spaced relationship therefrom and comprising a portion in ohmic contact with said material of the body adjacent said region, and a shield portion inwardly extending from the contact portion toward said region and spaced from the surface, said electrode serving to counteract the effects of surface inversion in the device.

6. A semiconductor device according to any preceding claim 3 wherein a second insulating coating covers said shield portion.

7. A semiconductor device according to Claim 6, wherein a conductive strip overlies said second insulating coating and the shield portion and makes electrical contact with said region.

8. A semiconductor device according to claim 6, wherein a second region is formed adjacent said surface within said region, which region is of the second conductivity type and wherein conductive strips overlie said second insulating coating and the shield portion and make separate electrical contact with the first and second regions.

9. A semiconductor device according to claim 8, wherein said device is a PNP planar transistor, said semiconductor body is of P-type conductivity, said first region is of N-type conductivity, said second region is of P-type conductivity and said electrode contacts a more heavily doped P+ type conductivity region.

10. A method of making a semiconductor device including the steps of:

(a) diffusing impurities into one face of a semiconductor body using a silicon oxide coating as a mask to form a region in said one face of conductivity type

- opposite that of the subjacent semiconductor material,
- (b) forming an opening in the silicon oxide coating on said one face which defines a closed configuration surrounding but spaced from said region,
- (c) selectively applying a metal film to said one face to adhere to the silicon surface in said opening and to extend inwardly towards said region of the oxide coating transverse to the opening,
- (d) applying another silicon oxide coating to said one face over the metal film,
- (e) forming an opening in the oxide coating above said region, and
- (f) applying a conductive metal strip over the oxide coating, the strip extending across but being insulated from the metal film, the strip engaging said region in the opening thereover.
11. A method according to claim 10, which includes a plurality of diffusion steps for forming regions in said semiconductor body.
12. A semiconductor device, substantially as described herein with reference to and as illustrated by Fig. 3 and Fig. 4 or any of Figs. 10 to 13 of the accompanying drawings.
13. A method for making a semiconductor device, substantially as described herein with reference to Figs. 5 to 8 of the accompanying drawings.
- H. D. FITZPATRICK & CO.,
Chartered Patent Agents of
27 Chancery Lane, London W.C.2
and
14-18 Cadogan Street, Glasgow C.2.

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