FIG. 1

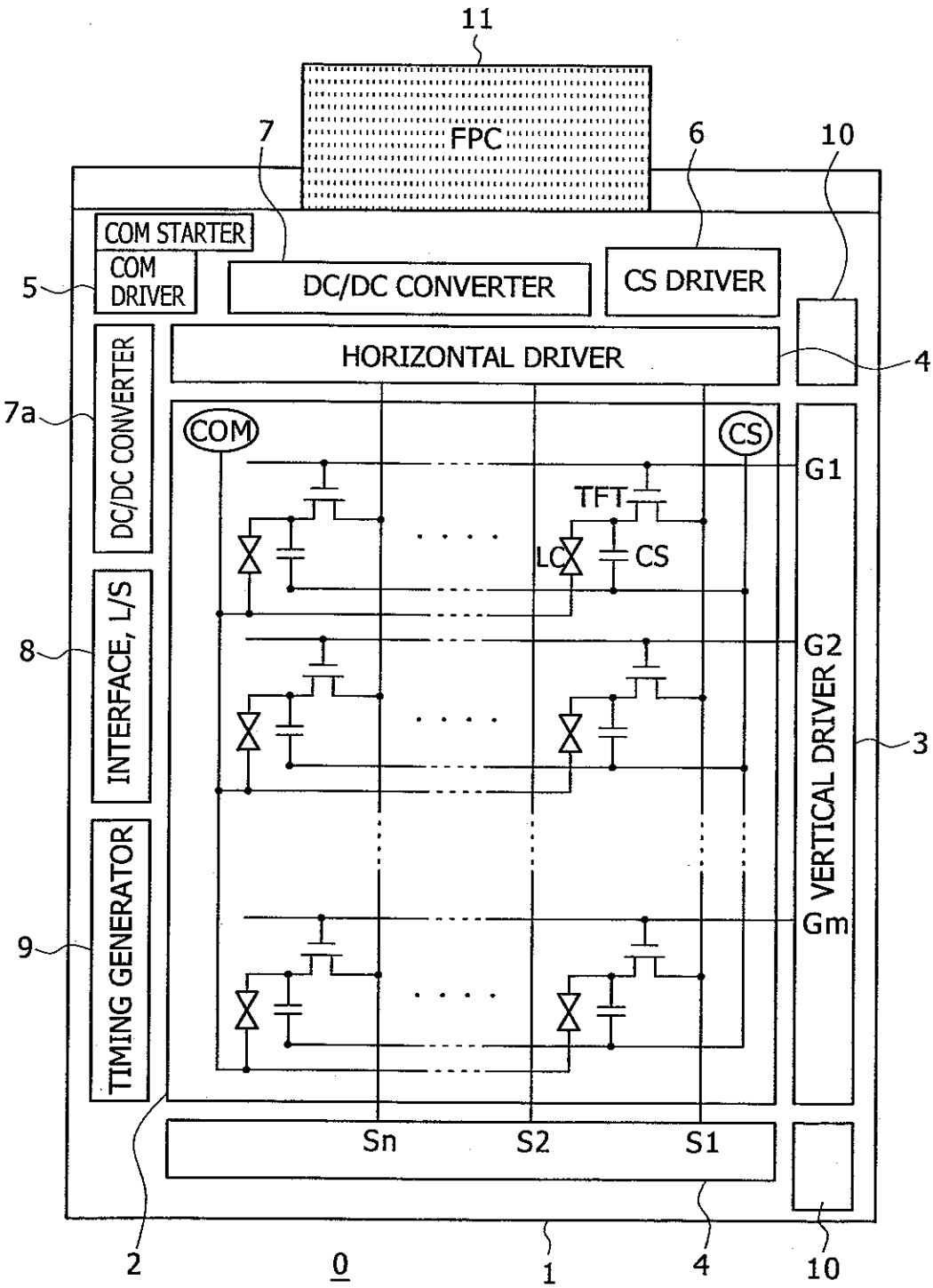

11
FPC
7
6
10
COM STARTER
COM DRIVER
5
DC/DC CONVERTER
CS DRIVER
HORIZONTAL DRIVER
4
7a
DC/DC CONVERTER
COM
CS
G1
TFT
LC
CS
G2
8
INTERFACE, L/S
VERTICAL DRIVER
3
9
TIMING GENERATOR
Gm
Sn
S2
S1
2
0
1
4
10

FIG. 2A

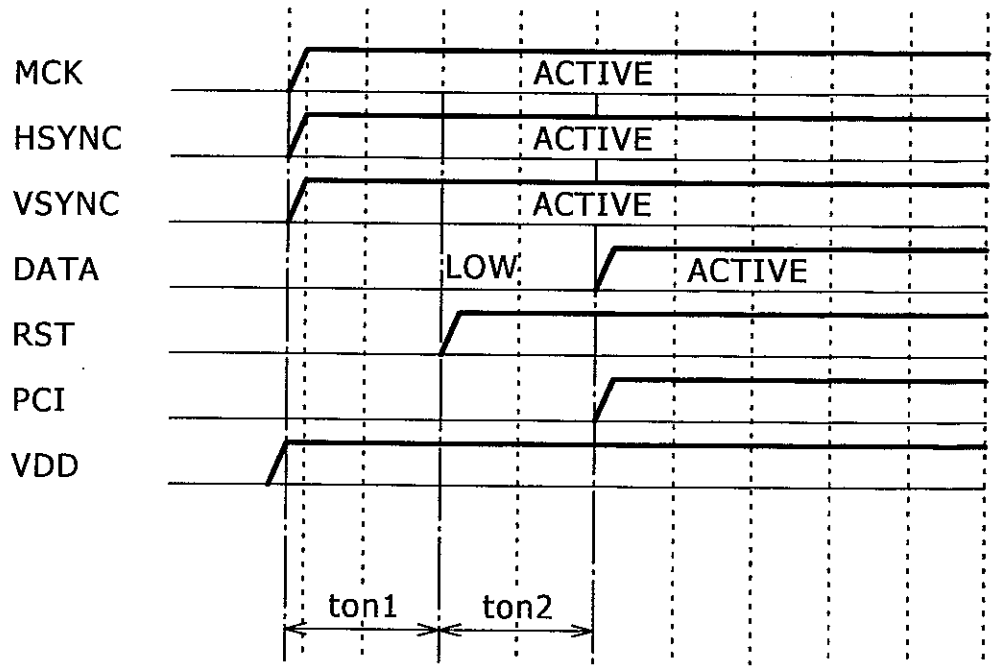

MCK
HSYNC
VSYNC
DATA
RST
PCI
VDD
ACTIVE
ACTIVE
ACTIVE
LOW
ACTIVE
ton1
ton2

FIG. 2B

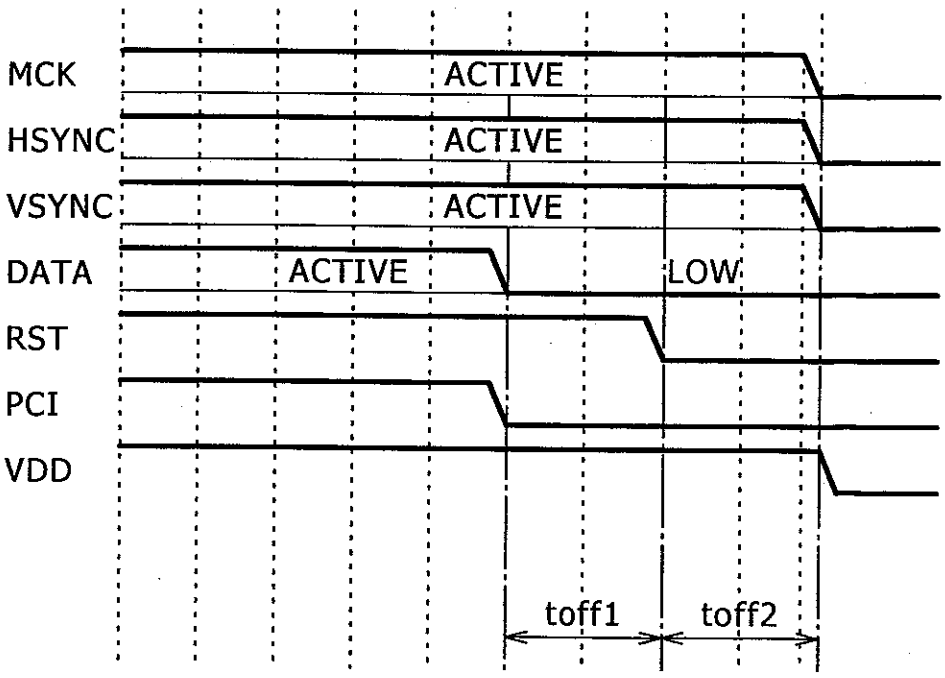

MCK
HSYNC
VSYNC
DATA
RST
PCI
VDD
ACTIVE
ACTIVE
ACTIVE
ACTIVE
LOW
toff1
toff2

FIG. 3A

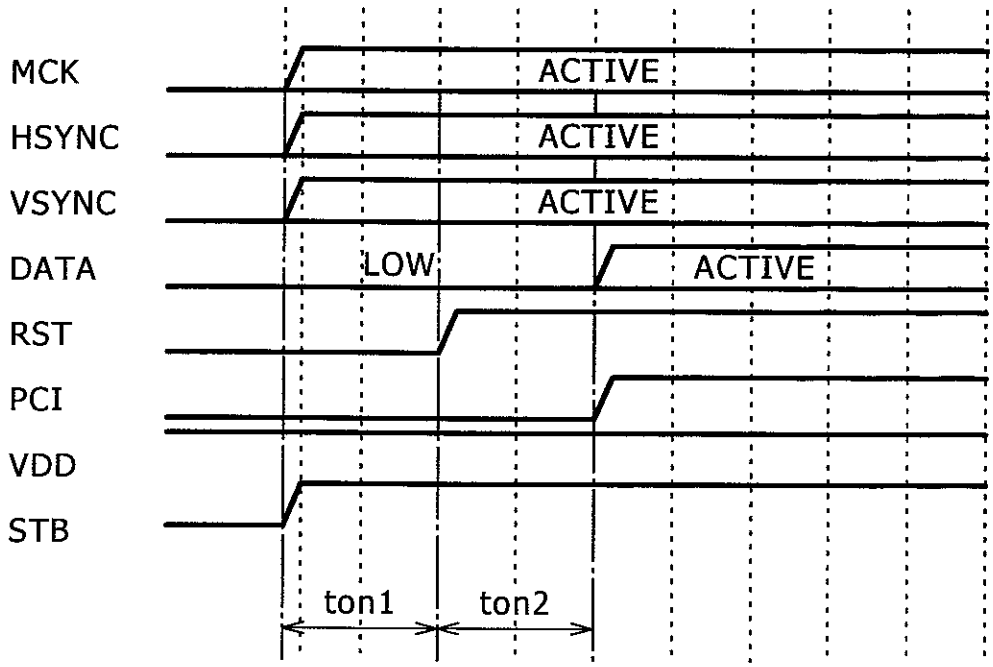

MCK
HSYNC
VSYNC
DATA
RST
PCI
VDD
STB
ACTIVE
ACTIVE
ACTIVE
LOW
ACTIVE
ton1
ton2

FIG. 3B

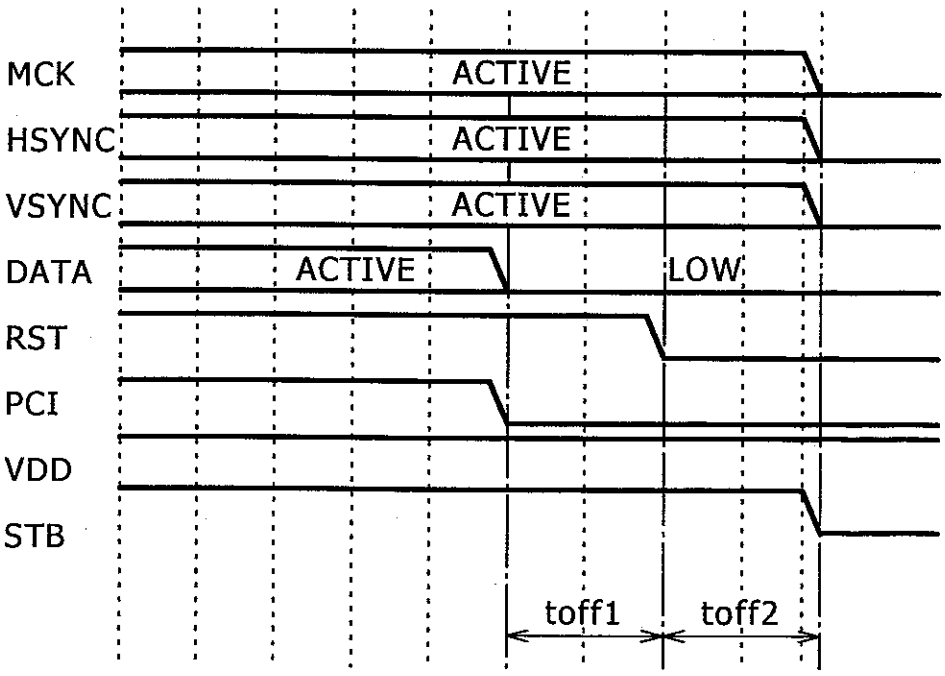

MCK
HSYNC
VSYNC
DATA
RST
PCI
VDD
STB
ACTIVE
ACTIVE
ACTIVE
ACTIVE
LOW
toff1
toff2

FIG. 4

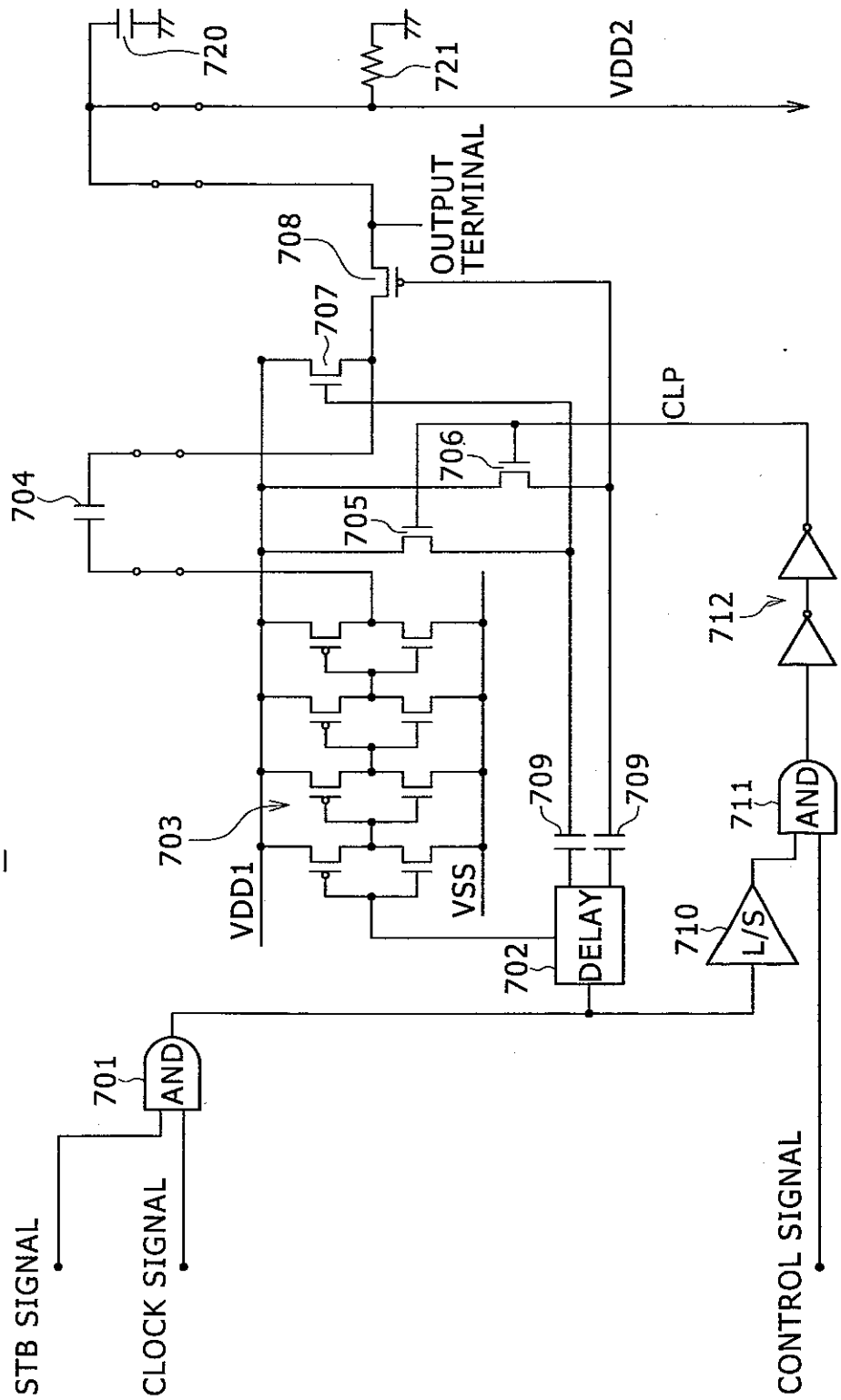

7
STB SIGNAL
CLOCK SIGNAL
CONTROL SIGNAL
701
AND
702
DELAY
703
704
705
706
707
708
709
709
710
L/S
711
AND
712
720
721
VDD1
VSS
VDD2
OUTPUT TERMINAL
CLP

FIG. 5

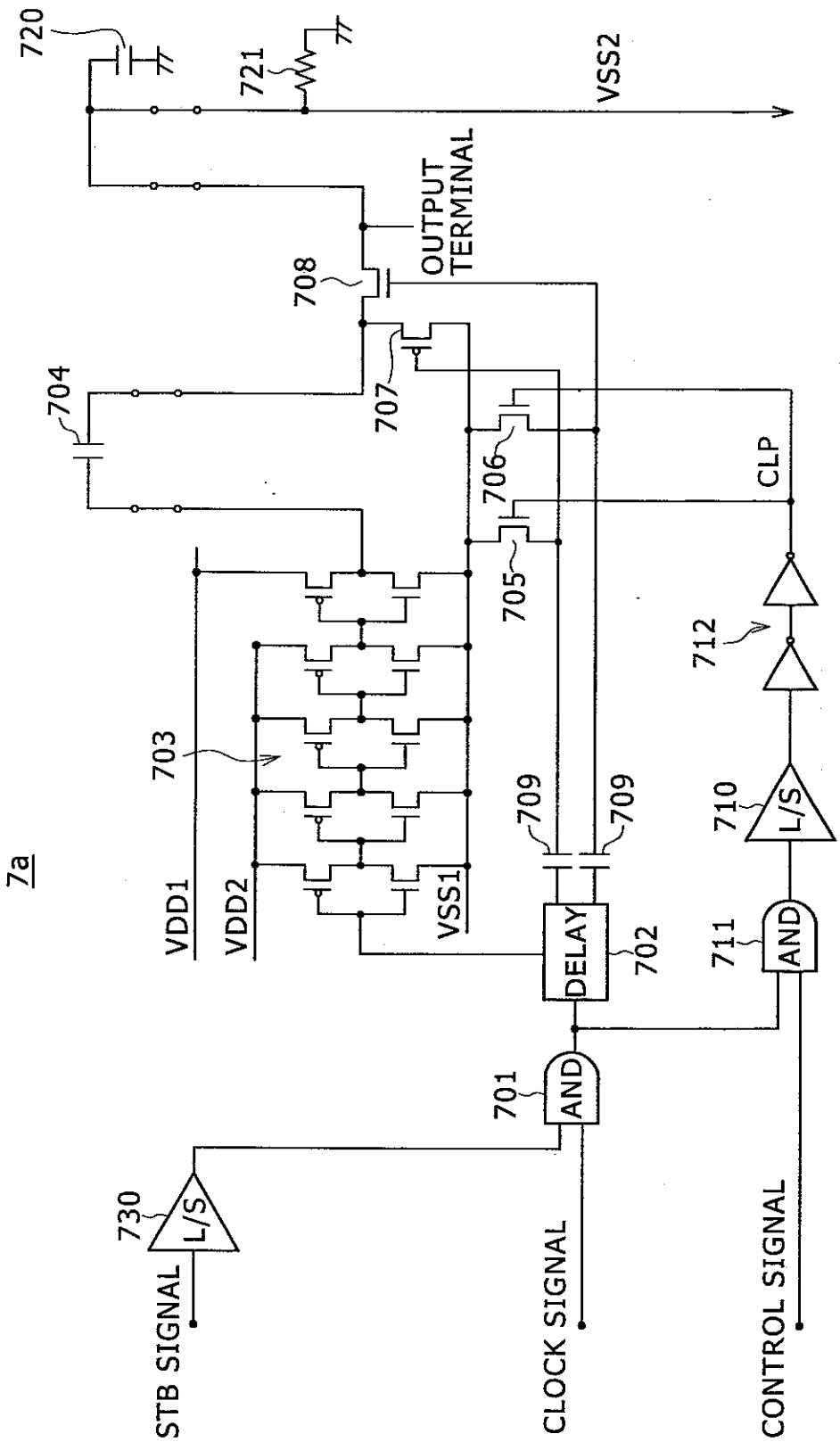

7a
720
721
VSS2
OUTPUT TERMINAL
708
704
707
706
705
CLP
712
703
VDD1
VDD2
VSS1
709
709
710
L/S
DELAY
702
711
AND
701
AND
730
L/S
STB SIGNAL
CLOCK SIGNAL
CONTROL SIGNAL

FIG. 6

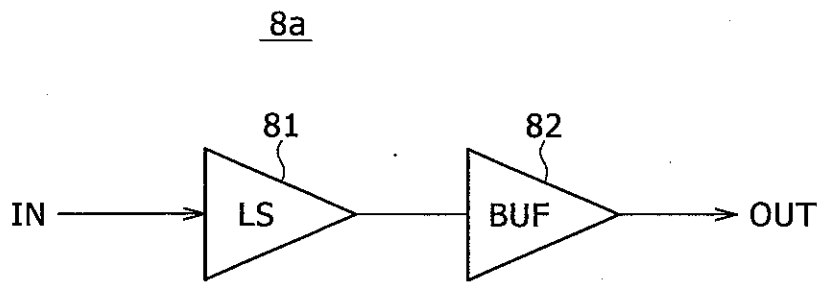


FIG. 7

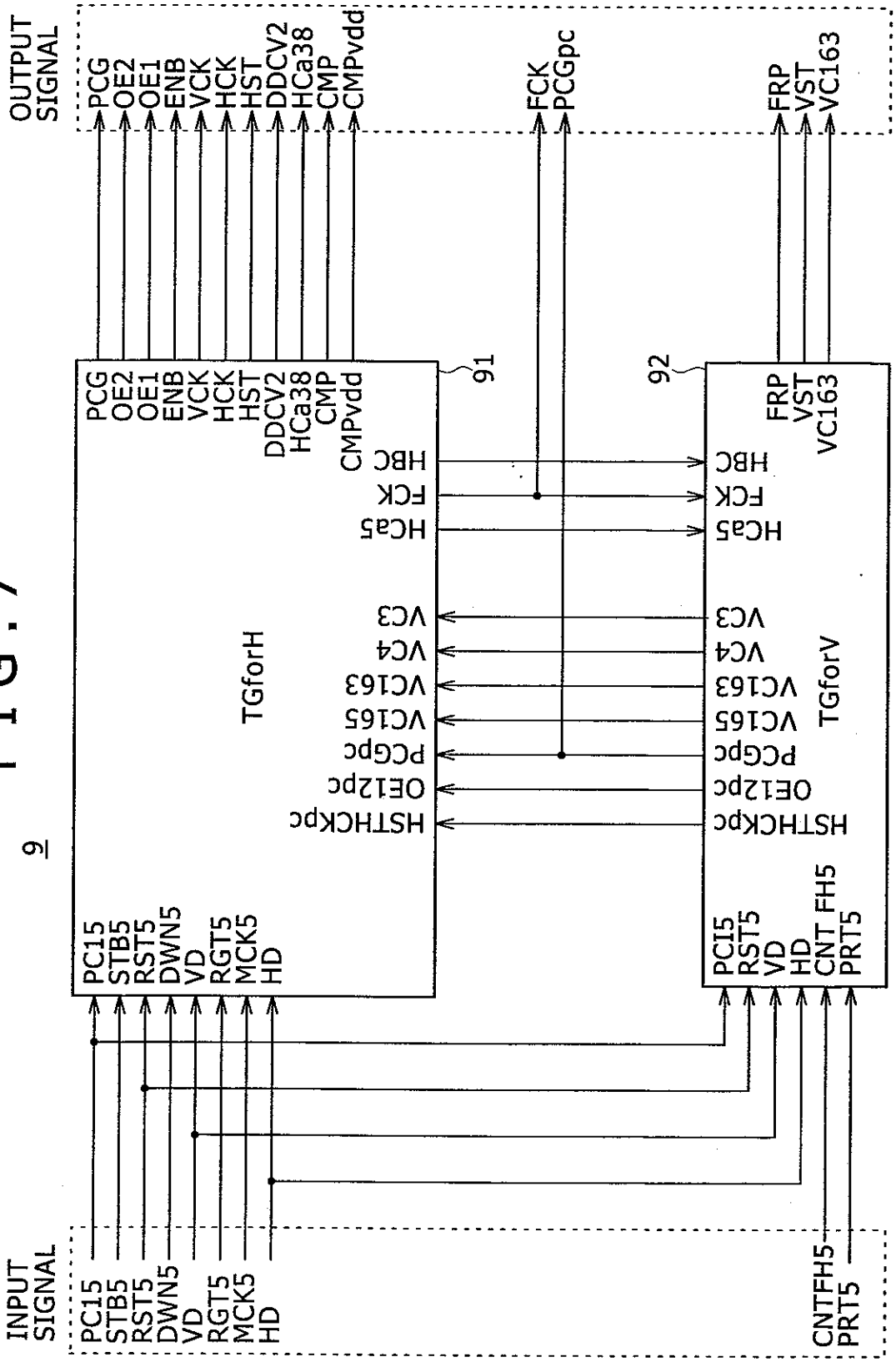

9
OUTPUT SIGNAL
PCG
OE2
OE1
ENB
VCK
HCK
HST
DDCV2
HCa38
CMP
CMPvdd
FCK
PCGpc
FRP
VST
VC163
91
92
TGforH
TGforV
HBC
FCK
HCa5
VC3
VC4
VC163
VC165
PCGpc
OE12pc
HSTHCKpc
PC15
STB5
RST5
DWN5
VD
RGT5
MCK5
HD
PCI5
RST5
VD
HD
CNT FH5
PRT5
INPUT SIGNAL
CNTFH5
PRT5

FIG. 8

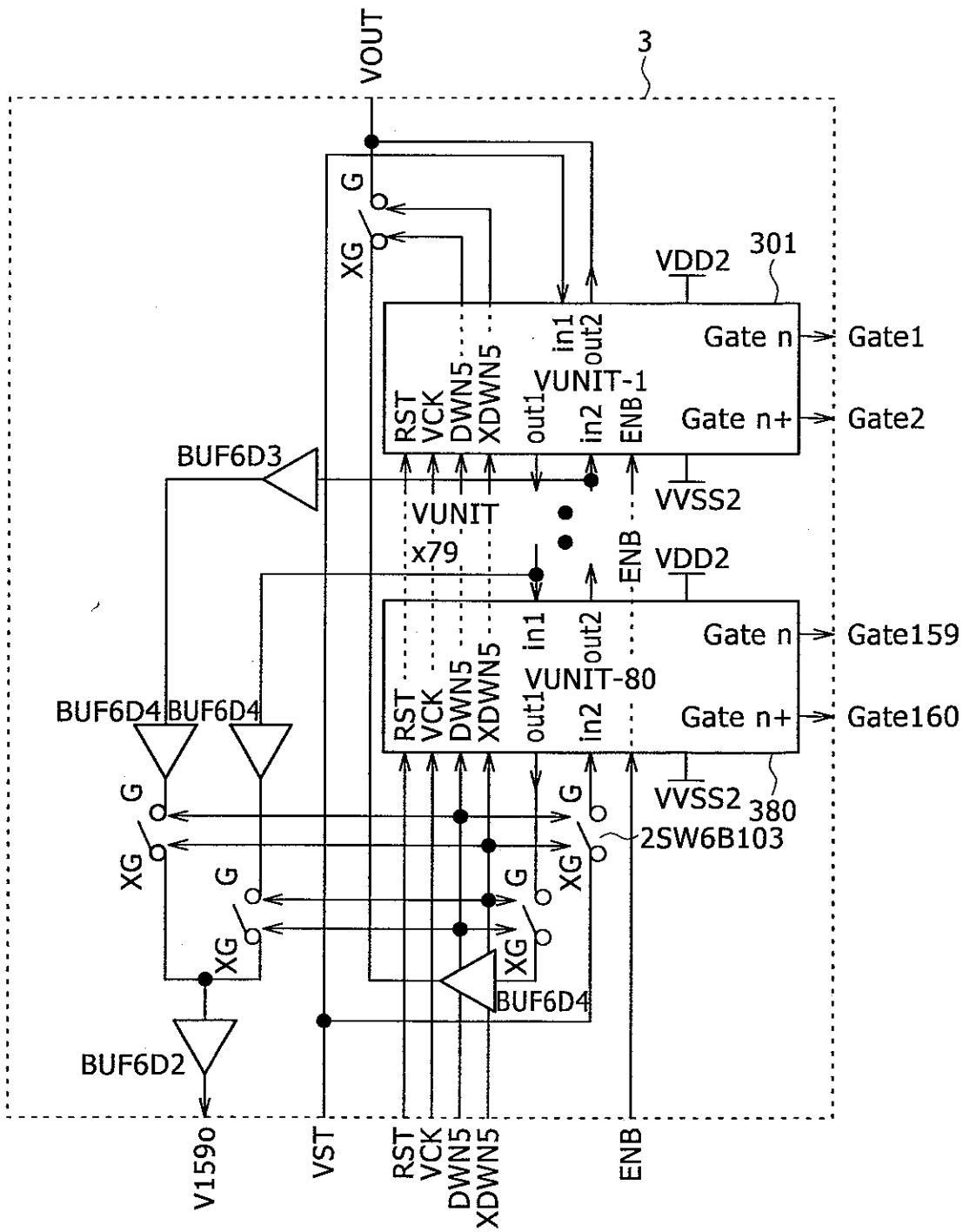

VOUT
3
G
XG
VDD2
301
RST
VCK
DWN5
XDWN5
out1
in1
out2
in2
ENB
VUNIT-1
Gate n
Gate n+
Gate1
Gate2
BUF6D3
VVSS2
VUNIT
x79
VDD2
VUNIT-80
Gate159
Gate160
BUF6D4
BUF6D4
380
2SW6B103
BUF6D4
BUF6D2
V159o
VST
RST
VCK
DWN5
XDWN5
ENB

FIG. 9

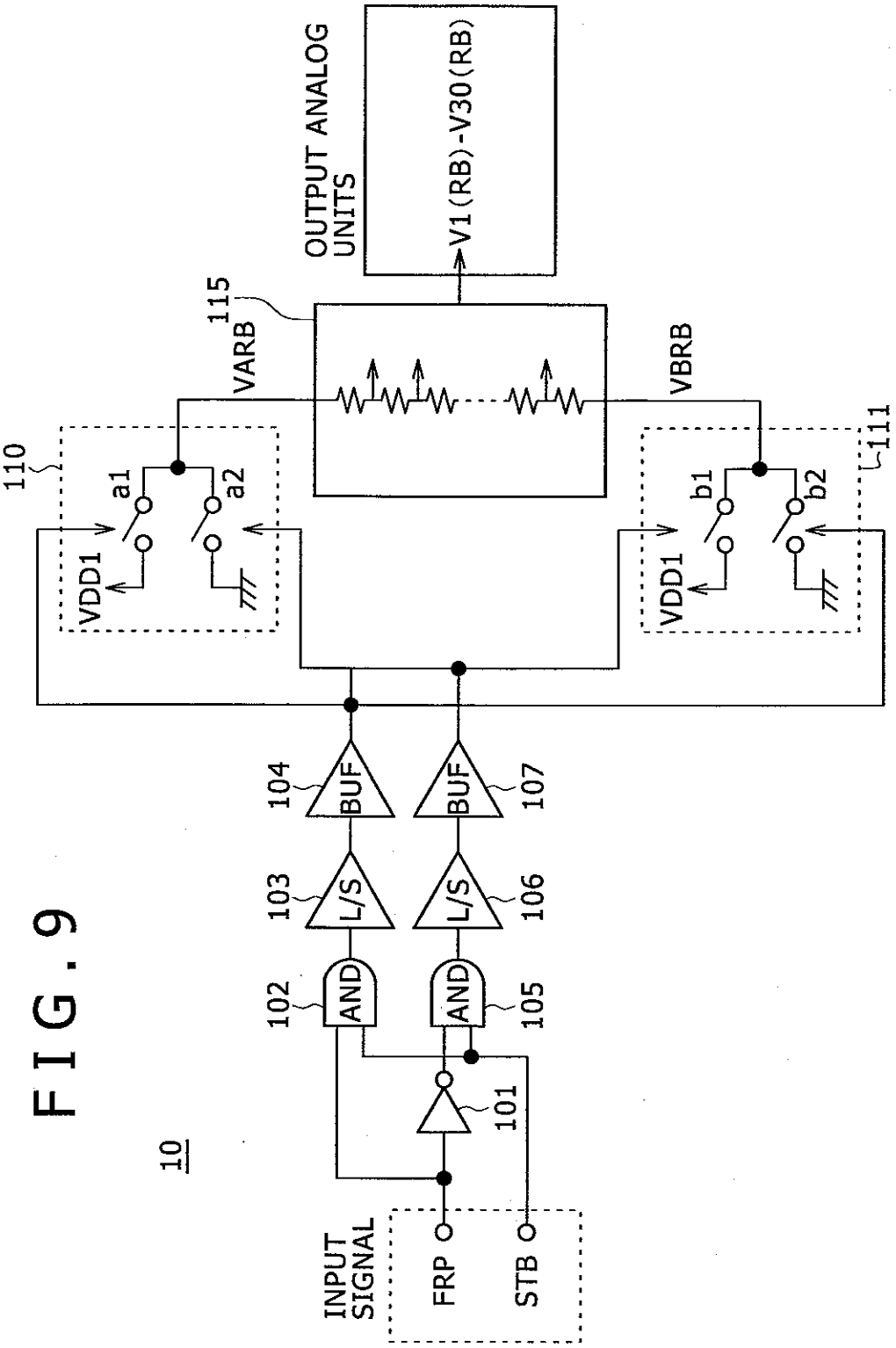

10
INPUT SIGNAL
FRP
STB
101
102
AND
103
L/S
104
BUF
105
AND
106
L/S
107
BUF
110
VDD1
a1
a2
111
VDD1
b1
b2
115
VARB
VBRB
OUTPUT ANALOG UNITS
V1(RB)-V30(RB)

FIG.10

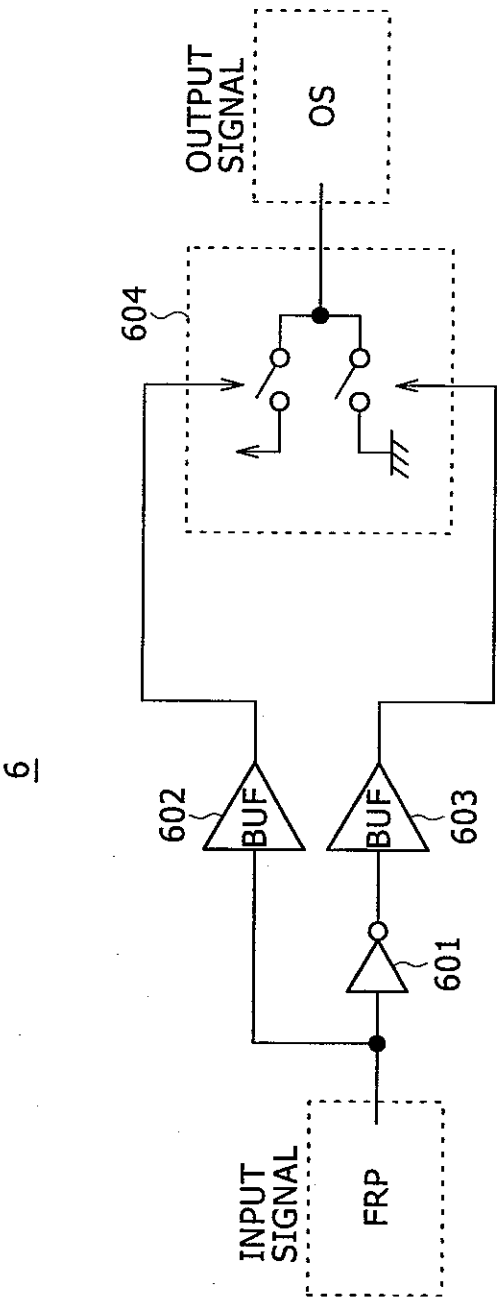


FIG.11

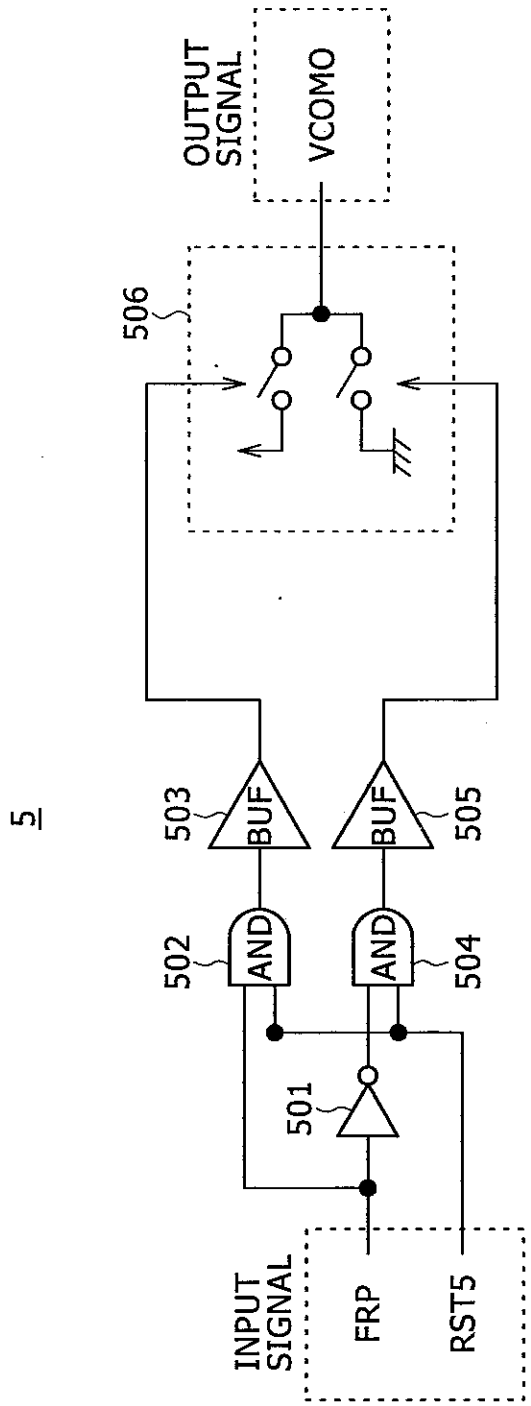
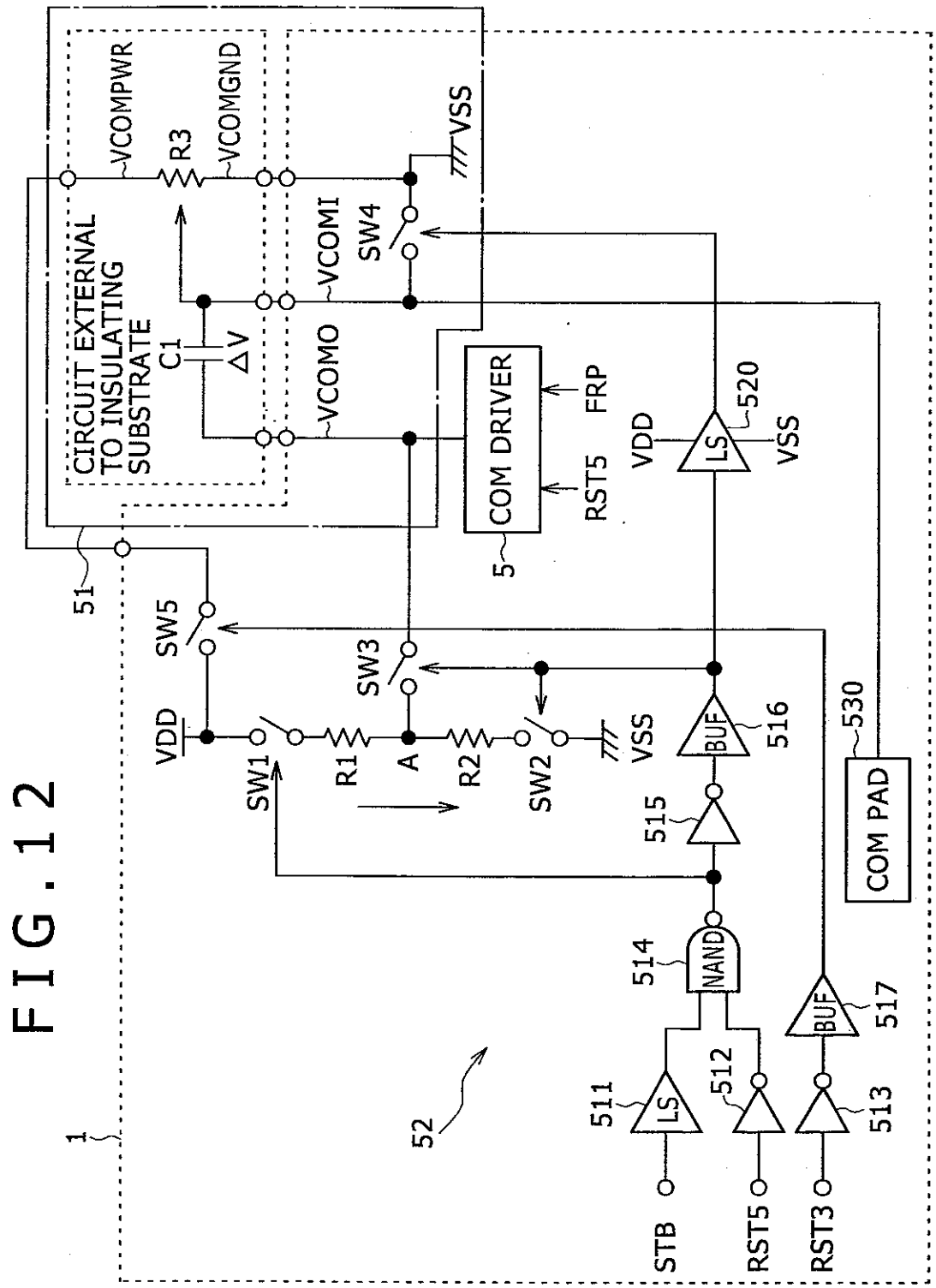

5
OUTPUT SIGNAL
VCOMO
506
503
BUF
505
BUF
502
AND
504
AND
501
INPUT SIGNAL
FRP
RST5

FIG. 12


1
52
CIRCUIT EXTERNAL TO INSULATING SUBSTRATE
VCOMPWR
R3
VCOMGND
VSS
VCOMI
SW4
C1
ΔV
VCOMO
COM DRIVER
FRP
RST5
5
VDD
LS
520
VSS
51
SW5
SW3
VDD
SW1
R1
A
R2
SW2
VSS
BUF
516
530
515
COM PAD
514
NAND
BUF
517
511
LS
512
513
STB
RST5
RST3