

Description

BACKGROUND OF THE INVENTION

This invention relates to a data processing technique and more particularly to a technique which is effective when applied to microcomputers. The present invention relates to a technique which can be utilized effectively, for example, for an output system of an external sync signal in a single-chip microcomputer having a sync signal.

In conventional single-chip microcomputers such as Model "HD6301V", a product of Hitachi, Ltd., a pin is provided for exclusively outputting an external sync signal called an "E clock" to peripheral devices. This single-chip microcomputer HD6301V includes therein a program storage ROM (read-only memory) and a working RAM (random access memory) and operates by itself, or in other words, a microcomputer system is constituted and operates inside the chip. Besides such a single-chip mode, the microcomputer has an external expansion mode in which the chip constitutes integrally a microcomputer system in cooperation with peripheral devices such as ROMs and RAMs that are connected thereto in order to expand the address space.

In this external expansion mode, the E clock described above is outputted from the single-chip microcomputer to the outside as a sync signal for the exchange of signals between the single-chip microcomputer and the peripheral devices. In the single-chip mode where the peripheral devices are not connected, therefore, the external sync signal (E clock) is not necessary.

However, in the conventional single-chip microcomputers of the type in which the external sync signal is generated inside them, the external sync signal is outputted to the output pin not only in the external expansion mode but also in the single-chip mode.

In this case, there occurs the problem that noise develops in the signal supplied to a pin, which is disposed next to the E clock output pin, because adjacent external terminals (pins) have an undesirable coupling capacity. In the single-chip microcomputers such as HD6301V in particular, the pin adjacent to the E clock output pin receives an input strobe signal SC as an input signal in the single-chip mode. Therefore, noise develops in this input strobe signal SC through the coupling capacity, so that erroneous data are likely to be latched.

Furthermore, an output buffer circuit which outputs the E clock as the external sync signal is constituted by circuit elements having greater sizes than other circuit elements because it must provide a great driving force, and the consumed current becomes large.

The single-chip microcomputer HD6301V having the E clock as the external sync signal is described on pages 279 to 31855 of "HITACHI MICROCOMPUTER DATA BOOK, 8-BIT SINGLE-CHIP" published by Hitachi, Ltd., February, 1985.

SUMMARY OF THE INVENTION

It is a primary object of the present invention to prevent an erroneous operation in a single-chip microcomputer having an external sync signal.

It is another object of the present invention to reduce a consumed current in a single-chip microcomputer having an external sync signal.

It is still another object of the present invention to prevent radio wave interference by eliminating current leakage from an output pin in a single-chip microcomputer having an external sync signal. These objects are achieved by the data processor according to Claim 1.

In accordance with the present invention, an external sync signal is supplied to an external terminal through a control gate and a suitable control signal is applied to a control terminal of the control gate. According to this circuit arrangement, it becomes possible to inhibit the supply of the external sync signal to the output terminal when the microcomputer is in the single-chip mode. As a result, it becomes possible to prevent noise from occurring in a signal supplied to an adjacent pin through a coupling capacitance between external terminals. It is further possible to reduce the consumed power of an output buffer that is disposed between the control gate and the output terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block circuit diagram of a single-chip microcomputer in accordance with one embodiment of the present invention; and

Fig. 2 is a block diagram of a system using the single-chip microcomputer shown in Fig. 1.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 shows an embodiment of the present invention applied to a single-chip microcomputer. Each circuit portion shown in the drawing is formed on one semiconductor substrate such as a single crystal silicon substrate.

The single-chip microcomputer shown in the drawing has substantially the same package structure and terminal arrangement as Hitachi Microcomputer HD6301VCG described in the aforementioned literature, though it is not particularly limitative.

Though not particularly limitative, either, the

single-chip microcomputer of this embodiment consists of a central processor unit (CPU) 1 for controlling its internal execution units in accordance with a program, a program ROM 2 storing therein the operation program of CPU1, RAM (random access memory) 3 providing primarily a work area of CPU1, a serial communication interface circuit 4, a timer circuit 5 and four input/output ports 6a to 6d. These circuits are connected to one another by an internal address bus 7a and an internal data bus 7b. Terminals T₁ to T₁₇ are external terminals connected to pins that are extended outside the package.

The address bus 7a and the data bus 7b are connected to the ports 6a and 6d among the input/output ports 6a to 6d, and they can be connected also to the port 6c through a multiplexor 8. There is further disposed a mode selector circuit 9 which determines the operation mode after resetting of the microcomputer by setting suitable external terminals T₁₀ to T₁₂ to a predetermined state. The control signal from this mode selector circuit 9 provides the input/output ports 6a and 6d with the data input/output function or the address output function. Similarly, the port 6c is provided with the data input/output function or the function of multiplexing the data bus and the address bus under the control of the mode selector circuit 9.

According to the circuit construction described above, the address space of the single-chip microcomputer of this embodiment can be expanded.

The mode selector circuit 9 takes in the state of the external terminals T₁₀ - T₁₂ at the time of resetting and holds the state, and the mode that is determined once cannot be changed even if the state of the external terminals T₁₀ to T₁₂ thereafter changes.

Though the detail of CPU 1 is not shown in the drawing, CPU 1 consists, for example, of an arithmetic and logic unit, an execution unit EXEC consisting of exclusive registers such as program counters, stack pointers, status registers and the like, a general-purpose register group REG used as a work area, instruction registers to which the instructions of macroprograms read out from an external memory are sequentially inputted, and a control unit CONT consisting of ROMs (microprogram ROMs) storing the microinstructions corresponding to the macroinstructions, respectively.

The execution unit EXEC is operated in a suitable sequence by a control signal outputted from the control unit CONT, thereby executing desired data processing.

An oscillation circuit 10 and a clock generation circuit 11 are disposed in order to control the operation timing of CPU 1. The oscillation frequency of the oscillation circuit 10 is determined

by a circuit element such as a quartz oscillator or a ceramic oscillator that is coupled between the external terminals T₁ and T₂. The clock generation circuit 11 receives the oscillation output of the oscillation circuit 10, divides suitably the frequency and generates system clocks ϕ_1 , ϕ_2 and E.

Among them, the clock E is supplied as the external sync signal to an output buffer 13, too, through a control gate 12 consisting, for example, of an AND gate, and can be outputted outside the chip from the external terminal T₃ by this output buffer 13.

In this embodiment, a register 15 is disposed for clock control, and one of the bits of this register 15 is used as an output designation flag of the clock E. The content of the output designation flag is supplied to the other of the input terminals of the control gate 12 to which the clock E is supplied.

The clock controlling register 15 is disposed as one of the internal registers and is connected to CPU 1 through the internal address bus 7a and the internal data bus 7b. When write is made to the register 15 by the program, logic "1" is set to the output designation flag or is cleared to "0".

In this embodiment, when the output designation flag is set to "1", the control signal C supplied to the control gate 12 rises to the high level, though this is not particularly limitative. Therefore, the control gate 12 supplies the clock E outputted from the clock generation circuit 11 to the output buffer 13. Upon receiving this E clock, the output buffer 13 is driven and the clock E is outputted as the external sync signal from the external terminal T₃.

On the other hand, when the output designation flag inside the clock controlling register 15 is cleared to the logic "0", the control signal C falls to the low level, so that the control gate 12 is closed and the clock E generated by the clock generation circuit 11 is not supplied to the output buffer 13. As a result, the leakage of harmonic waves at the rise of output, that results from driving of the output buffer 13 under a non-load state, can be eliminated and the consumed current in the output buffer 13 can be reduced. Since the clock E is not outputted to the external terminal T₃, the noise does not enter the input signal of the adjacent terminal, which is adjacent to the external terminal T₃, through the coupling capacity between the external terminal T₃ and the adjacent terminal.

The single-chip microcomputer having the construction described above has two kinds of operation modes, that is, the single-chip mode and the external expansion mode. In this embodiment, however, the external expansion mode further includes two modes, that is, a multiplex mode of the address and data and their non-multiplex mode.

When the mode selector circuit 9 judges that

the operation mode is set to the single-chip mode in accordance with the state of the external terminals $T_{10} - T_{12}$, the function of each input/output port 6a - 6d is determined by the control signal from the mode selector circuit 9, and the signals on the internal address bus 7a and the internal data bus 7b are not outputted outside the microcomputer. Therefore, the single-chip microcomputer constitutes a microcomputer system by its internal circuit alone. At this time, LED, a motor driver, various sensors, a keyboard scanner and other devices are connected to the external terminals of the chip. The microprocessor unit 1 inside the single-chip microcomputer executes predetermined data processing in accordance with the program inside ROM 2 on the basis of the signals inputted thereto from the keyboard, the sensors or the like, and generates and outputs the control signals for the various devices such as LED, the motor, and the like, that are connected thereto.

In contrast, when the mode selector circuit 9 judges that the operation mode is set to the external expansion mode in accordance with the state of the external terminals $T_{10} - T_{12}$. The function of each input/output port 6a - 6d is changed by the control signal from the mode selector circuit 9, and the address signals and data signals on the address and data buses 7a and 7b can now be outputted to the external bus, and the signals on the external bus can be taken into the internal data bus 7b. In the external expansion mode, peripheral devices such as ROMs, RAMs or PIAs (peripheral interface adaptors) are connected to the address bus AB and the external data bus DB, and these peripheral devices and the single-chip microcomputer together constitute a microcomputer system.

In the embodiment described above, the clock E is supplied to, or cut off from, the output buffer 13 through the control gate 12 in accordance with the operation mode depending upon whether the output designation flag in the clock controlling register 15, which is disposed inside the single-chip microcomputer as shown in Fig. 1, is "1" or "0". However, in the single-chip microcomputer having the mode selector circuit 9 such as shown in Fig. 1, the signal representing whether the present state is the single-chip mode or the external expansion mode exists inside the mode selector circuit 9. Therefore, it is possible not to supply the clock E, which is generated from the clock generation circuit 11, to the output buffer 13 when the microcomputer is in the single-chip mode by extending a signal representing whether or not the operation mode is the single-chip mode from inside the mode selector circuit 9 and applying this signal to one of the input terminal of the control gate 12, instead of disposing the clock control register 15. According to this arrangement, the output buffer 13

is not driven in the single-chip mode, and the external sync signal is not outputted to the external terminal T_3 so that the same effect as described above can be obtained.

The embodiment shown in Fig. 1 uses the AND gate as the control gate 12 and closes this control gate 12 in the single-chip mode in order not to supply the clock E from the clock generation circuit 11 to the output buffer 13. However, it is also possible to employ a circuit construction wherein the output buffer 13 is of a push-pull type and the control gate 12 is a logic circuit which forms a control signal that brings the output buffer 13 into tristate on the basis of the signal from the output designation flag.

Though the embodiment described above represents the application of the present invention to a single-chip microcomputer having both the single-chip mode and the external expansion mode, the present invention is not particularly limited to such a single-chip microcomputer. For instance, single-chip microcomputers not having the external expansion mode such as Hitach Model HD6805 have an external terminal called an "NUM pin" which is not used for external connection but is used while being kept fixed to the ground potential. This NUM pin outputs to the outside a sync signal necessary for testing when connected to a V_{cc} level at the time of testing. In this case, too, the sync signal is applied up to the final output stage which is connected to the NUM pin in the prior art single-chip microcomputers. Accordingly, the present invention can provide the same effect as described above when applied to the output circuit corresponding to such an NUM pin.

As described above, the present invention provides the following effects.

(1) In single-chip microcomputers having an external sync signal, the present invention supplies the external sync signal generated by the internal clock generation circuit of the microcomputer to the output buffer through the control gate, and inputs a suitable control signal to the control terminal of the control gate in order to inhibit the supply of the external sync signal to the output buffer in the single-chip mode. Since the output of the external sync signal to the output pin is inhibited in the single-chip mode, noise does not enter the signal of the adjacent pin due to the coupling capacity between the external terminals (pins) and hence, the erroneous operation of the circuit can be prevented.

(2) In single-chip microcomputers having an external sync signal, the present invention supplies the external sync signal generated by the internal clock generation circuit of the microcomputer to the output buffer through the control gate, and inputs a suitable control signal to the

control terminal of the control gate in order to inhibit the supply of the external sync signal to the output buffer in the single-chip mode. Since the output buffer itself does not operate in the single-chip mode, the leakage of the radio wave from the output pin resulting from the harmonic waves at the time of rise of the sync signal can be eliminated, radio wave interference can be therefore removed and a consumed current in the buffer for clock output that has been extremely great in the prior art microcomputers can be eliminated with the result being in the drastic reduction of the consumed current of the chip as a whole.

Although the present invention has thus been described definitely with reference to its preferred embodiment, the invention is not particularly limited thereto but can of course be changed or modified in various ways. For example, in accordance with the embodiment described above, the external terminal T_3 becomes an empty pin which is not at all used in the single-chip mode, and input and output of other signals can be made by use of this pin.

Claims

1. A data processor formed on one semiconductor chip and being capable of operating in a single-chip mode or in an external expansion mode, comprising a central processing unit (1), a first external terminal (T_3) for delivering a sync signal when said data processor is in said external expansion mode, a second terminal adjacent to said first terminal (T_3), and a sync signal generation circuit to generate said sync signal,
 - characterized by
 - control means (9 or 15) for generating a gate control input signal (C) having a first state when the data processor is to be operated in the single-chip mode, and a second state when the data processor is to be operated in the external expansion mode, and
 - gate means (12), being coupled between said first terminal (T_3) and said sync signal generation circuit (10, 11), for inhibiting the supply of said sync signal (E) at said first terminal (T_3) in response to reception of the gate control input signal (C) having the first state and enabling the supply of said sync signal (E) at said first terminal (T_3) in response to reception of the gate control input signal having the second state.
2. Data processor according to claim 1, wherein said control means (9 or 15) includes a register (15) into which data can be written by said central processing unit (1), and the operation of said gate means (12) is controlled in accordance with the data in said register (15).
3. Data processor according to claim 1 or 2, comprising a bus (7b), said second external terminal being coupled to said bus (7b), and to which a signal from the outside of said data processor is fed.
4. Data processor according to claim 1, which further includes an output buffer circuit (13) connected between said gate means (12) and said first external terminal (T_3), wherein the supply of said sync signal (E) to said output buffer circuit (13) can be inhibited by said control means (9 or 15).
5. Data processor according to claim 1, wherein said control means (9 or 15) includes a mode selector circuit (9) for providing said control signal (C) to said gate means (12).
6. Data processor according to any one of the preceding claims, comprising a read only memory (2), and wherein the central processing unit (1) is coupled to said read only memory (2) via a bus (7b) and executes a predetermined data processing in accordance with a program stored in said read only memory (2).
7. Data processor according to claim 6, wherein operation timing of the central processing unit (1) is controlled by a clock signal ($\phi 1$, $\phi 2$) supplied thereto.
8. Data processor according to claim 7, wherein, in the external expansion mode, the central processing unit (1) has access to an address space provided by the read only memory (2), a random access memory (3) and a memory device externally coupled thereto, wherein the external memory device is coupled to the first external terminal (T_3) to receive the sync signal (E) therefrom, and is coupled to the second external terminal so that exchange of data between the central processing unit (1) and the external memory device is synchronously controlled in accordance with the sync signal (E).
9. Data processor according to claim 5, comprising third external terminals (T_{10} - T_{12}) coupled to the mode selector circuit to which data for determining an operation mode of the data processor is to be fed.
10. Data processor according to any one of the preceding claims, wherein the sync signal generator circuit (10, 11) includes an oscillation

control terminal of the control gate in order to inhibit the supply of the external sync signal to the output buffer in the single-chip mode. Since the output buffer itself does not operate in the single-chip mode, the leakage of the radio wave from the output pin resulting from the harmonic waves at the time of rise of the sync signal can be eliminated, radio wave interference can be therefore removed and a consumed current in the buffer for clock output that has been extremely great in the prior art microcomputers can be eliminated with the result being in the drastic reduction of the consumed current of the chip as a whole.

Although the present invention has thus been described definitely with reference to its preferred embodiment, the invention is not particularly limited thereto but can of course be changed or modified in various ways. For example, in accordance with the embodiment described above, the external terminal T_3 becomes an empty pin which is not at all used in the single-chip mode, and input and output of other signals can be made by use of this pin.

Claims

1. A data processor formed on one semiconductor chip and being capable of operating in a single-chip mode or in an external expansion mode, comprising a central processing unit (1), a first external terminal (T_3) for delivering a sync signal when said data processor is in said external expansion mode, a second terminal adjacent to said first terminal (T_3), and a sync signal generation circuit to generate said sync signal, characterized by control means (9 or 15) for generating a gate control input signal (C) having a first state when the data processor is to be operated in the single-chip mode, and a second state when the data processor is to be operated in the external expansion mode, and gate means (12), being coupled between said first terminal (T_3) and said sync signal generation circuit (10, 11), for inhibiting the supply of said sync signal (E) at said first terminal (T_3) in response to reception of the gate control input signal (C) having the first state and enabling the supply of said sync signal (E) at said first terminal (T_3) in response to reception of the gate control input signal having the second state.
2. Data processor according to claim 1, wherein said control means (9 or 15) includes a register (15) into which data can be written by said central processing unit (1), and the operation of said gate means (12) is controlled in accordance with the data in said register (15).
3. Data processor according to claim 1 or 2, comprising a bus (7b), said second external terminal being coupled to said bus (7b), and to which a signal from the outside of said data processor is fed.
4. Data processor according to claim 1, which further includes an output buffer circuit (13) connected between said gate means (12) and said first external terminal (T_3), wherein the supply of said sync signal (E) to said output buffer circuit (13) can be inhibited by said control means (9 or 15).
5. Data processor according to claim 1, wherein said control means (9 or 15) includes a mode selector circuit (9) for providing said control signal (C) to said gate means (12).
6. Data processor according to any one of the preceding claims, comprising a read only memory (2), and wherein the central processing unit (1) is coupled to said read only memory (2) via a bus (7b) and executes a predetermined data processing in accordance with a program stored in said read only memory (2).
7. Data processor according to claim 6, wherein operation timing of the central processing unit (1) is controlled by a clock signal ($\phi 1$, $\phi 2$) supplied thereto.
8. Data processor according to claim 7, wherein, in the external expansion mode, the central processing unit (1) has access to an address space provided by the read only memory (2), a random access memory (3) and a memory device externally coupled thereto, wherein the external memory device is coupled to the first external terminal (T_3) to receive the sync signal (E) therefrom, and is coupled to the second external terminal so that exchange of data between the central processing unit (1) and the external memory device is synchronously controlled in accordance with the sync signal (E).
9. Data processor according to claim 5, comprising third external terminals (T_{10} - T_{12}) coupled to the mode selector circuit to which data for determining an operation mode of the data processor is to be fed.
10. Data processor according to any one of the preceding claims, wherein the sync signal generator circuit (10, 11) includes an oscillation



circuit (10) and a clock generator (11) for receiving an output of the oscillation circuit (10) and for generating the clock signal ($\phi 1$, $\phi 2$) and the sync signal (E) by dividing a frequency of the output of the oscillation circuit (10).

Revendications

1. Processeur de données formé sur une micro-plaquette à semiconducteurs et apte à fonctionner dans un mode monopuce ou dans un mode d'expansion externe, comprenant une unité centrale de traitement (1), une première borne externe (T_3) servant à délivrer un signal de synchronisation lorsque ledit processeur de données est dans ledit mode d'expansion externe, une seconde borne adjacente à ladite première borne (T_3), et un circuit de production du signal de synchronisation servant à produire ledit signal de synchronisation, caractérisé par des moyens de commande (9 ou 15) servant à produire un signal d'entrée de commande de porte (C) possédant un premier état lorsque le processeur de données doit fonctionner dans le mode monopuce, et un second état lorsque le processeur de données doit fonctionner dans le mode d'expansion externe, et des moyens formant porte (12) branchés entre ladite première borne (T_3) et ledit circuit (10,11) de production du signal de synchronisation, pour bloquer l'envoi dudit signal de synchronisation (E) à ladite première borne (T_3) en réponse à la réception du signal d'entrée de commande de porte (C) possédant le premier état, et autorisant la délivrance dudit signal de synchronisation (E) sur ladite première borne (T_3) en réponse à la réception du signal d'entrée de commande de porte possédant le second état.
2. Processeur de données selon la revendication 1, dans lequel lesdits moyens de commande (9 ou 15) comprennent un registre (15), dans lequel des données peuvent être enregistrées par ladite unité centrale de traitement (1), et le fonctionnement desdits moyens formant porte (12) est commandé en fonction des données situées dans ledit registre (15).
3. Processeur de données selon la revendication 1 ou 2, comprenant un bus (7b) auquel est accouplée ladite seconde borne externe et auquel un signal est envoyé à partir de l'extérieur dudit processeur de données.
4. Processeur de données selon la revendication 1, qui comporte en outre un circuit formant tampon de sortie (13) branché entre lesdits moyens formant porte (12) et ladite première borne externe (T_3), la délivrance dudit signal de synchronisation (E) audit circuit formant tampon de sortie (13) pouvant être bloquée par lesdits moyens de commande (9 ou 15).
5. Processeur de données selon la revendication 1, dans lequel lesdits moyens de commande (9 ou 15) comprennent un circuit sélecteur de mode (9) servant à délivrer ledit signal de commande (C) auxdits moyens formant porte (12).
6. Processeur de données selon l'une quelconque des revendications précédentes, comprenant une mémoire morte (2) et dans lequel l'unité centrale de traitement (1) est accouplée à ladite mémoire morte (2) par l'intermédiaire d'un bus (7b) et exécute un traitement prédéterminé des données en fonction d'un programme mémorisé dans ladite mémoire morte (2).
7. Processeur de données selon la revendication 6, dans lequel la synchronisation du fonctionnement de l'unité centrale de traitement (1) est commandée par un signal d'horloge ($\phi 1, \phi 2$) envoyé à cette unité.
8. Processeur de données selon la revendication 7, dans lequel, dans le mode d'expansion externe, l'unité centrale de traitement (1) a accès à un espace adresses fourni par la mémoire morte (2), une mémoire à accès direct (3) et un dispositif de mémoire accouplé de façon externe à cette mémoire, le dispositif de mémoire externe étant accouplé à la première borne (T_3) pour recevoir, à partir de cette dernière, le signal de synchronisation (E), et étant accouplé à la seconde borne externe de manière que l'échange des données entre l'unité centrale de traitement (1) et le dispositif de mémoire externe est commandé d'une manière synchrone en fonction du signal de synchronisation (E).
9. Processeur de données selon la revendication 5, comprenant des troisièmes bornes externes ($T_{10}-T_{12}$) accouplées au circuit sélecteur de mode, auquel des données permettant de déterminer un mode de fonctionnement du processeur de données doivent être envoyées.
10. Processeur de données selon l'une quelconque des revendications précédentes, dans le-



quel le circuit (10,11) formant générateur du signal de synchronisation comprend un circuit oscillant (10) et un générateur d'impulsions d'horloge (11), apte à recevoir un signal de sortie du circuit oscillant (10) et à produire le signal d'horloge ($\phi 1, \phi 2$) et le signal de synchronisation (E) par division d'une fréquence du signal de sortie du circuit oscillant (10).

Patentansprüche

1. Datenprozessor, der auf einem Halbleiterchip ausgebildet und in einem Einzelchip-Modus oder in einem externen Erweiterungsmodus betreibbar ist, umfassend eine zentrale Verarbeitungseinheit (1), einen ersten externen Anschluß (T_3) zur Abgabe eines Synchronsignals, wenn sich der Datenprozessor in dem externen Erweiterungsmodus befindet, einen dem ersten Anschluß (T_3) benachbarten zweiten Anschluß, und eine Synchronsignal-Generatorstufe zur Erzeugung des Synchronsignals,

gekennzeichnet durch

eine Steuereinrichtung (9 oder 15) zur Erzeugung eines Gattersteuer-Eingangssignals (C) mit einem ersten Zustand, wenn der Datenprozessor in dem Einzelchip-Modus arbeiten soll, und einem zweiten Zustand, wenn der Datenprozessor in dem externen Erweiterungsmodus arbeiten soll, und

eine zwischen den ersten Anschluß (T_3) und die Synchronsignal-Generatorstufe (10, 11) eingeschaltete Gatterstufe (12), die bei Empfang des Gattersteuer-Eingangssignals (C) mit dem ersten Zustand die Zuführung des Synchronsignals (E) an den ersten Anschluß (T_3) sperrt und bei Empfang des Gattersteuer-Eingangssignals mit dem zweiten Zustand die Zuführung des Synchronsignals (E) an den ersten Anschluß (T_3) freigibt.

2. Datenprozessor nach Anspruch 1, wobei die Steuereinrichtung (9 oder 15) ein Register (15) aufweist, in das Daten von der zentralen Verarbeitungseinheit (1) eingeschrieben werden können, und wobei die Arbeitsweise der Gatterstufe (12) entsprechend den Daten in dem Register (15) gesteuert wird.
3. Datenprozessor nach Anspruch 1 oder 2, umfassend eine Sammelleitung (7b), mit dem der zweite externe Anschluß verbunden ist und der ein Signal von außerhalb des Datenprozessors zugeführt wird.
4. Datenprozessor nach Anspruch 1, ferner umfassend einen zwischen die Gatterstufe (12) und den ersten externen Anschluß (T_3) einge-

schaltete Ausgangspufferstufe (13), wobei die Zuführung des Synchronsignals (E) an die Ausgangspufferstufe (13) von der Steuereinrichtung (9 oder 15) gesperrt werden kann.

5. Datenprozessor nach Anspruch 1, wobei die Steuereinrichtung (9 oder 15) eine Modus-Auswahlstufe (9) zur Zuführung des Steuersignals (C) an die Gatterstufe (12) umfaßt.

6. Datenprozessor nach einem der vorhergehenden Ansprüche, umfassend einen Festspeicher (2), wobei die zentrale Verarbeitungseinheit (1) über eine Sammelleitung (7b) an den Festspeicher (2) angeschlossen ist und entsprechend einem in dem Festspeicher (2) gespeicherten Programm eine vorbestimmte Datenverarbeitung ausführt.

7. Datenprozessor nach Anspruch 6, wobei der zeitliche Ablauf der Arbeitsweise der zentralen Verarbeitungseinheit (1) durch ein ihr zugeführtes Taktsignal ($\phi 1, \phi 2$) gesteuert wird.

8. Datenprozessor nach Anspruch 7, wobei in dem externen Erweiterungsmodus die zentrale Verarbeitungseinheit (1) Zugriff zu einem in dem Festspeicher (2) vorhandenen Adressenfeld, einem Random-Access-Speicher (3) und einer extern angeschlossenen Speichereinrichtung hat, und wobei die externe Speichereinrichtung mit dem ersten externen Anschluß (T_3) verbunden ist, um das Synchronsignal (E) von diesem zu erhalten, und mit dem zweiten externen Anschluß verbunden ist, so daß ein Datenaustausch zwischen der zentralen Verarbeitungseinheit (1) und der externen Speichereinrichtung entsprechend dem Synchronsignal (E) synchron gesteuert wird.

9. Datenprozessor nach Anspruch 5, umfassend mit der Modus-Auswahlstufe verbundene dritte externe Anschlüsse (T_{10}, T_{12}), denen Daten zur Bestimmung des Arbeitsmodus des Datenprozessors zugeführt werden.

10. Datenprozessor nach einem der vorhergehenden Ansprüche, wobei die Synchronsignal-Generatorstufe (10, 11) eine Oszillatorstufe (10) und einen Taktgenerator (11) zur Aufnahme eines Ausgangssignals der Oszillatorstufe (10) und Erzeugung des Taktsignals ($\phi 1, \phi 2$) sowie des Synchronsignals (E) durch Teilen einer Frequenz des Ausgangssignals der Oszillatorstufe (10) umfaßt.

