SYSTEM WITH MESHED POWER AND SIGNAL BUSES ON CELL ARRAY

Abstract of the Disclosure

A method and apparatus for providing a meshed power and signal bus system on an array type integrated circuit that minimizes the size of the circuit. In a departure from the art, through-holes for the mesh system are placed in the cell array, as well as the peripheral circuits. The power and signal buses of the mesh system run in both vertical and horizontal directions across the array such that all the vertical buses lie in one metal layer, and all the horizontal buses lie in another metal layer. The buses of one layer are connected to the appropriate bus(es) of the other layer using through-holes located in the array. Once connected, the buses extend to the appropriate sense amplifier drivers. The method and apparatus are facilitated by an improved subdecoder circuit implementing a hierarchical word line structure.

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