METHOD OF SEMICONDUCTOR MANUFACTURE

This invention relates generally to methods of making semiconductors. More specifically, the present invention relates to methods applicable when changing the effective position of ("re-routing") bond pads.

After an integrated circuit (IC) has been made, it is necessary to package it in a way that will allow it to be connected to a circuit board. This involves providing input/output terminals so that the semiconductor may communicate with other segments of the electronic/electrical system. This is usually accomplished by providing bond pads on the IC which can have wires attached to them by solder. In order to achieve greater accessibility and flexibility, it is often necessary to change the position of the bond pads already present on an IC.

Presently, such re-routing may be carried out in accordance with the method schematically illustrated in Figure 1 of the accompanying drawings. This method comprises placing a patterned metal layer 1 onto a passive layer 2 on a semiconductor chip 3 such that the metal layer comes into contact with the exposed bond pad 4 (see Figure 1a.) Another layer of passive material 5 is then laid over the metal layer. A portion of the second layer of passive material 5 is then etched so that a part of the metal layer at a position different to the original bond pad position is exposed (see Figure 1b). This effectively changes the position of the bond pad to a new position.

The problem with this prior method is that the process used for laying the metal layer is an expensive and lengthy process known as physical vapour deposition (PVD). This process involves the spraying of minute metal particles onto the surface of the passive layer until a complete coating of a very thin layer of metal is achieved. This process is also known as "sputtering". The equipment required for this method is very expensive and the process takes a long time to carry out (an average of an hour or so for some machines).

According to a first aspect of the present invention there is provided a method of applying a metal layer to a semiconductor element, said method comprising:

providing a semi-conductor element having at least one bond pad on an outer

surface thereof;

thermo-compressing a metal foil onto said semiconductor element so as to be substantially parallel to said at least one bond pad;

wherein a layer of dielectric material is provided between said metal foil and said semiconductor element.

Accordingly, the present invention provides a method for re-routing bond pads which avoids the sputtering process altogether. Therefore, the method of the present invention is less expensive and is able to be carried out in a shorter time than conventional methods.

The layer of dielectric material may be initially provided adjacent to the bond pad on the semiconductor element so that the metal foil may be thermo-compressed thereon. Alternatively, the layer of dielectric material could initially be provided adjacent to the metal foil as an adhesive layer avoiding the need to place a layer of dielectric material on the bond pad initially. As a further alternative, two layers of dielectric material could be used, one adjacent to the bond pad and one adjacent to the metal foil as an adhesive layer.

According to a second aspect of the present invention there is provided a method of creating an interconnection between a first conductive substrate and a second conductive substrate, said second substrate being parallel to, and spaced apart from, said first substrate, said substrates being positioned so that at least part of said first substrate is visible when viewed from the side of said second substrate in a direction perpendicular to the plane of both substrates, said method comprising:

protecting areas of non-interconnection of said second substrate with a resistant coating;

submerging said substrates partially or wholly into an electroless nickel plating bath so that nickel is deposited adjacent to said first substrate until a satisfactory interconnect is obtained between said first and second substrates.

Preferably, the bond pad is cleaned in an alkaline cleaning step before being submerged into the electroless nickel plating bath. The bond pad may also be activated prior to submergence by being immersed in a zincation fluid.

After nickel plating, a passive layer may preferably be provided adjacent to

the nickel layer which can then be etched to reveal a portion of the second substrate. Then, an under-bump metallisation (UBM) layer may be applied to the revealed portion so that a bump can be placed thereon for connection to other electrical/electronic items.

According to a third aspect of the present invention there is provided a method of re-routing at least one bond pad provided on a semiconductor, said method comprising:

providing a layer of dielectric material either adjacent to said semiconductor or adjacent to a metal layer to be applied to said semiconductor;

thermo-compressing said metal layer onto said semiconductor so as to sandwich said layer of dielectric material;

applying a layer of photo resist over said metal layer;

carrying out photo lithographic and etching steps on said layer of photo resist so as to reveal at least a portion of said at least one bond pad;

applying a layer of photo resist to a side of said semiconductor opposite to the side upon which said bond pad is located;

cleaning said portion of said bond pad with an alkaline solution to remove any oxides from said portion of said bond pad;

immersing said structure partially or wholly in a zincation fluid to activate the bond pad;

immersing said structure partially or wholly in an electroless nickel plating bath so that nickel is deposited on said bond pad in an amount sufficient to connect said bond pad to said metal layer;

providing a layer of passive material adjacent to the resulting sandwich structure so as to cover said nickel plating; and

etching said passive layer to reveal at least a portion of said metal layer.

Each of the first, second and third aspects of the invention are applicable to all known wafer substrates including those made of gallium arsenide or silicon. The various dielectric layers in the methods of the present invention may be polyimide or thermoplastic resins.

Typically, the metal foil layer used has a thickness less than 18 microns or

more preferably ranges from 3 to 5 microns.

The thermo-compression step of the first and third aspects of the invention is preferably carried out at a pressure in the range of 340 to 420 kPa and at a temperature in the range of 200 to 350°C when the dielectric material is polyimide and in the range of 150 to 200°C when the dielectric material is a thermoplastic resin.

In the second and third aspects of the invention mentioned above, it is preferable that the deposited nickel forms a layer greater than 3 microns thick or more preferably in the range of 8 to 15 microns thick. In order to deposit such layers, it is preferred to use a sodium hypophosphite based bath at a temperature in the range of 70 to 90°C for a duration in the range of 20 to 30 minutes as the electroless nickel plating bath.

The present invention will be further described by way of non-limitative example only, with reference to the accompanying drawings, in which:

Figure 1 illustrates schematically in cross-sectional side-on view a known prior art method of re-routing a bond pad;

Figure 2 illustrates schematically in cross-sectional side-on view a method of applying a metal layer according to a first embodiment of the first aspect of the present invention;

Figure 3 illustrates schematically in cross-sectional side-on view a method of applying a metal layer according to a second embodiment of the first aspect of the present invention;

Figure 4 illustrates schematically in cross-sectional side-on view a method of applying a metal layer according to a third embodiment of the first aspect of the present invention;

Figure 5 illustrates schematically, in cross-sectional side-on view, a method of creating an interconnection between a first conductive substrate and a second conductive substrate in accordance with the second aspect of the present invention;

The method of applying a metal layer to a semiconductor element in accordance with the first aspect of the present invention will now be described with reference to Figures 2, 3 and 4.

In each of the three embodiments, the semiconductor element 20 contains a

single bond pad 21 on the right-hand side of the element which is desired to be re-routed to the left-hand side. The invention is not only applicable to elements having a single bond pad but may be applied to multi-pad elements. In such cases, a separate metal layer is needed for each re-routing process.

In the first embodiment of the invention, a layer of dielectric material 22 is deposited onto the IC surface over the semiconductor element 20 and bond pad 21. This layer is required in order to achieve good bonding for the metal layer that is to come. A thermo-compression technique is then used to attach the metal layer 23 to the layer of dielectric as shown in Figure 2b. The metal layer has a pressure exerted on it and is applied at a raised temperature so that it bonds well with the dielectric. The resulting structure is a thin metal layer 23 parallel to, and spaced apart from, the bond pad 21 (see Figure 2c).

Before thermo-compression, it is desirable to partially cure the layer of dielectric material 22 to achieve good bonding. After thermo-compression, the resulting structure is fully cured.

A second embodiment of the invention may be used as an alternative to the above process and is illustrated in Figure 3. As shown in Figure 3a, the metal layer 23 is precoated with a thin layer of organic compound 24 (which is chosen for its good adhesive properties) which is then pressed onto the element and bond pad directly. This results in the same structure as the previous embodiment since the bond pad ends up being separated from the metal layer by a thin layer of dielectric (see Figure 3b).

A further alternative is shown in Figure 4 as a third embodiment of this first aspect of the invention, a layer of dielectric is applied both to the element bond pad 21 as a passive layer 22 and to the back of the metal layer 23 as an adhesive layer 24. This results in a slightly thicker sandwich of dielectric but the overall structure is still the same.

In each embodiment, the parameters of the thermo-compression step are dictated largely by the particular material used for the dielectric. It is preferable that the temperature is greater than the glass transition temperature of the dielectric layer but less than the decomposition temperature of the dielectric layer. If a polyimide

based material is used for the dielectric passive layer, the temperature of thermo-compression should be between 200 and 350°C. A pressure of about 340 kPa to 420 kPa (50 to 60 psi) is also sufficient. If the passive layer is made of a thermoplastic resin, a temperature range of between 150 and 200°C is more appropriate. A pressure of 340 kPa to 420 kPa is also appropriate for thermoplastic-resin layers.

The metal layer in each embodiment typically comprises a metal foil of less than 18 microns in thickness. Preferably, the foil is less than 15 microns in thickness and more preferably still, is in the range of from 3 to 5 microns.

If a layer of adhesive dielectric is used, it has been found to be desirably in the range of from 5 to 8 microns in thickness.

As can be seen, this method of applying a metal layer has the advantage of totally avoiding the sputtering process. The above process of applying the metal layer by thermo-compression is generally much cheaper than the conventional sputtering process. Furthermore, the process of the present invention can be carried out much more quickly than conventional sputtering processes. The omission of this sputtering process (which can be a bottleneck in the IC packaging process as only a limited small number of ICs may be placed in the sputtering machine to undergo metallization at any time) therefore has a significant time advantage. Typically the thermo-compression process takes just a few minutes.

One disadvantage is that a dielectric intermediate layer is required to achieve good bonding so that the metal layer is not applied directly to the bond pad as in the prior art. To complete the re-routing process, therefore, it is necessary to interconnect the metal layer thus provided with the bond pad in some way. One method of doing this is described below.

The interconnection between the bond pad 21 and the metal layer 23 must have low electrical parasitics to reduce or prevent any signal loss. Also, the interconnect must be reliable in different environments.

Figure 5 shows an embodiment according to the second aspect of the invention in which an interconnection between the bond pad 21 and metal layer 23 (already provided parallel to one another) is made.

The process firstly comprises laying a passive layer of photo-resist 25 over

the metal layer 23. This protects the metal layer during the succeeding steps. Next, various etching and lithography steps (see Figure 5b) are carried out to etch through the photo-resist 25, metal layer 23 and dielectric layer 24 to reveal at least a portion of the original bond pad 21. Such chemical etching and lithography steps are well known in the art. After this, the surface of the bond pad 21 is cleaned in an alkaline solution to remove any oxide. Next, a layer of photo-resist 26 is applied to the backside of the semiconductor wafer to protect it (see Figure 5a). Thus, all of the surfaces of the wafer are now isolated except for the bond pad surface. Next, the entire structure is immersed in fluid to active the bond pads and make them receptive to the next stage, which is nickel plating. This immersion step is called "zincation". For this zincation step, the fluid used is based on a zinc salt and is preferably between 30 and 70°C. The zincation step usually takes around 10 to 15 minutes. The wafer may be wholly or partially immersed; it is only necessary that the bond pad itself receives the zincation treatment. After this, the interconnection is made using a nickel plating method. This is shown in Figure 5e. The nickel plating is performed using a so-called "electroless" method. This means that no electric current is required to be fed through the bath in which the wafer is submerged in for nickel plating to occur. In this stage, the wafer is partially or wholly submerged in a nickel plating bath which deposits a layer of nickel plating 27 on the bond pads. This depositing occurs because the bond pads have been made receptive to receive the nickel by the zincation step. The amount of nickel deposited is dependent upon the duration and temperature at which the wafer is submerged in the bath. The nickel is allowed to build up in height so as to form an interconnect 27 between the metal layer 23 and bond pad 21 as shown in Figure 5e.

The nickel plating bath comprises a nickel based salt fluid. For this step, the temperature is preferably maintained between 70 and 90°C and a duration between about 20 to 30 minutes is generally sufficient to produce a nickel interconnect of appropriate thickness. Usually, 8 to 15 microns in thickness is sufficient to create a good electrical connection.

After the abovementioned steps, the photo-resist 26 on the backside of the wafer 20 may be removed using a standard chemical etching process and a passive

layer 28 may be applied to the top of the sandwich structure to cover the nickel plating (see Figure 5f). This passive layer is then be etched in a place different to the position of the original bond pad so as to effectively re-route the bond pad by revealing the metal layer. Following this, the normal under-bump metallization (UBM) 29 and bump 30 may be applied to the re-routed bond pad position (see Figure 5h). The underbump metallization is usually about 3 microns thick.

As with the first aspect of the invention, there is no requirement to use a sputtering process resulting in cheaper and faster operation. Further, the height of the nickel interconnect can be easily controlled using the abovementioned technique by varying the temperature and duration of submergence in the nickel plating bath appropriately.

The first and second aspects of the invention are ideally used in combination to provide a method of re-routing a bond pad on a semiconductor wafer. Although the total number of steps of this combined method is more than in a conventional prior art process involving a sputtering method, the advantages obtained in terms of time, expense and throughput outweigh the additional complexity.

The above methods are suitable for all semiconductor wafers known in the industry, including GaAs and silicon wafers.

CLAIMS

1. A method of applying a metal layer to a semiconductor element, said method comprising:

providing a semi-conductor element having at least one bond pad on an outer surface thereof;

thermo-compressing a metal foil onto said semiconductor element so as to be substantially parallel to said at least one bond pad;

wherein a layer of dielectric material is provided between said metal foil and said semiconductor element.

2. The method of claim 1 wherein said layer of dielectric material is provided adjacent to said bond pad and said metal foil is thermo-compressed adjacent to said layer of dielectric material.

3. The method of claim 1 or 2, wherein said metal foil is provided on one side with a layer of dielectric adhesive material before said thermo-compressing step.

4. A method of creating an interconnection between a first conductive substrate and a second conductive substrate, said second substrate being parallel to, and spaced apart from, said first substrate, said substrates being positioned so that at least part of said first substrate is visible when viewed from the side of said second substrate in a direction perpendicular to the plane of both substrates, said method comprising:

protecting areas of non-interconnection of said second substrate with a resistant coating;

submerging said substrates partially or wholly into an electroless nickel plating bath so that nickel is deposited adjacent to said first substrate until a satisfactory interconnect is obtained between said first and second substrates.

5. The method of claim 4 further comprising an alkaline cleaning step before said submerging step.

6. The method of claim 4 or 5 further comprising immersing said substrates partially or wholly in a zincation fluid before said submerging step.

7. The method of any one of claims 4 to 6, further comprising:

providing a passive layer adjacent to said nickel plating and resistant coating;

etching through said passive layer so as to reveal a portion of said second substrate.

8. The method of claim 7 further comprising:

providing an under bump metallization layer adjacent to the exposed portion of said second substrate; and

creating a bump on said under bump metallization layer.

9. A method of re-routing at least one bond pad provided on a semiconductor, said method comprising:

providing a layer of dielectric material either adjacent to said semiconductor or adjacent to a metal layer to be applied to said semiconductor;

thermo-compressing said metal layer onto said semiconductor so as to sandwich said layer of dielectric material;

applying a layer of photo resist over said metal layer;

carrying out photo lithographic and etching steps on said layer of photo resist so as to reveal at least a portion of said at least one bond pad;

applying a layer of photo resist to a side of said semiconductor opposite to the side upon which said bond pad is located;

cleaning said portion of said bond pad with an alkaline solution to remove any oxides from said portion of said bond pad;

immersing said structure partially or wholly in a zincation fluid to activate the bond pad;

immersing said structure partially or wholly in an electroless nickel plating bath so that nickel is deposited on said bond pad in an amount sufficient to connect said bond pad to said metal layer;

providing a layer of passive material adjacent to the resulting sandwich structure so as to cover said nickel plating; and

etching said passive layer to reveal at least a portion of said metal layer.

10. The method of any preceding claim wherein said semiconductor is a GaAs or silicon wafer substrate.

11. The method of any one of claims 1 to 3 or 9 wherein said layer of dielectric material is made of a polyimide material.

12. The method of any preceding claim wherein said metal foil, said second substrate, or said metal layer are formed of a metal foil having a thickness less than 18 microns.

13. The method of any preceding claim wherein said metal foil, said second substrate, or said metal layer are formed of a metal foil having a thickness in the range of from 3 to 5 microns.

14. The method of any preceding claim wherein said at least one bond pad or said first substrate are aluminium based or copper based.

15. The method of any one of claims 4 to 9, wherein said deposited nickel forms a nickel plating layer greater than 3 microns thick.

16. The method of claim 15 wherein said nickel plating layer is in the range of from 8 to 15 microns thick.

17. The method of any one of claims 1 to 3 or 9, wherein said thermo-compression step is carried out at a temperature greater than the glass transition temperature of said layer of dielectric material but less than the decomposition temperature of said layer of dielectric material.

18. The method of claim 17, wherein said layer of dielectric material is polyimide and said thermo-compression step is carried out at a temperature in the range of from 200 to 350°C.

19. The method of claim 17 wherein said layer of dielectric material is a thermoplastic material and said thermo-compression step is carried out at a temperature in the range of from 150 to 200°C.

20. The method of any one of claims 1 to 3, 9 or 17 to 19, wherein said thermo-compression step is carried out at a pressure in the range of from 340KPa to 420KPa.

21. The method of claim 3 wherein said adhesive layer is an organic compound in the range of from 5 to 8 microns thickness.

22. The method of claim 6 or 9, wherein said substrates are immersed or said structure is immersed in a zincation fluid made of a zinc salt at a temperature in the range of from 30 to 70°C for a duration in the range of from 10 to 15 minutes.

23. The method of claim 4 or 9, wherein said step of submerging in an electroless nickel plating bath comprises submerging said substrates or structure in a sodium hypophosphite based bath at a temperature in the range of from 70 to 90°C for a duration in the range of from 20 to 30 minutes.

24. An integrated circuit board comprising at least one semiconductor chip produced using a method according to any preceding claim.

25. A method of making a semiconductor chip comprising the method of any one of claims 1 to 23.

26. A method of applying a metal layer to a semiconductor element substantially

as hereinbefore described with reference to Figures 2, 3 and 4 of the accompanying drawings.

27. A method of creating an interconnection between two conductive substrates substantially, as hereinbefore described with reference to Figure 5 of the accompanying drawings.

28. A method of rerouting at least one bond pad provided on a semiconductor substantially as hereinbefore described with reference to Figures 2 to 5 of the accompanying drawings.