Annealing process for annealing a structure

Background of the invention

The present invention relates to the field of annealing in oxidizing atmospheres used especially during the fabrication of multilayer semiconductor structures or substrates (also called multilayer semiconductor wafers) obtained by transferring at least one layer onto a support substrate, such as BSOI (bonded silicon-on-insulator) structures.

An example of a known process for fabricating a multilayer structure is described with reference to Figures 1A to 1F.

As shown in Figures 1A and 1B, a composite structure 100 is formed by assembling a first wafer 101 and a second wafer 102, for example made of silicon. The first and second wafers, 101 and 102, here have the same diameter. They could however have different diameters.

An additional oxide layer (not shown) may be formed on one or both wafers, 101 and 102, before placing them in contact – especially when fabricating an SOI (silicon-on-insulator) structure.

The first wafer 101 has a chamfered edge, namely an edge comprising a top chamfer 104 and a bottom chamfer 105.

The role of these chamfers is to make handling the wafers easier and to prevent edge flaking that could occur if these edges were sharp, such flakes being a source of particulate contamination on the surfaces of the wafers.

In the example described here, the wafer assembly is produced using the direct bonding (molecular adhesion) technique, well known to those skilled in the art.

Once the bonding step is completed, the composite structure 100 undergoes a stabilizing anneal the purpose of which is to strengthen the bond between the first wafer 101 and the second wafer 102 and to cover these two wafers with a protective oxide layer.

For this purpose, the stabilizing anneal is carried out in an oxidizing atmosphere so as to form an oxide layer 110 on the entire exposed surface of the composite structure 100 (Figure 1C). The oxide layer 100 thus forms a protective layer that protects the composite structure from chemical etches, especially during the subsequent processing operation.

The structure 100 is then trimmed, which consists in principally eliminating an annular portion of the layer 106 comprising the chamfer 105 (Figures 1D and 1E).

Such trimming is necessary because the presence of the chamfer 105 prevents a good contact between the first and the second wafers at their periphery. There is therefore a peripheral region where the transferred layer is weakly bonded, or not at all bonded, to the second wafer. This peripheral region of the transferred layer must be removed because it is liable to break in an uncontrolled way and to contaminate the structure with undesirable fragments or particles.

Preferably trimming called hybrid trimming is used which consists in carrying out a first trimming step by an entirely mechanical action or by entirely mechanical machining (Figure 1D), followed by a second, at least partially non-mechanical, trimming step for trimming the remaining thickness of the first wafer (Figure 1E). This second trimming step corresponds in general to chemical trimming that is selective with respect to the oxide layers formed on the wafer(s) 101 and/or 102. The hybrid trimming especially prevents peel-off both at the bonding interface between the transferred layer and the second wafer and in the transferred layer itself.

In the example envisaged here, the chemical trimming step consists in chemical etching, also called wet etching. The chemical etching solution is chosen depending on the material to be etched. In this example, either the etching solution TMAH or KOH, well known to those skilled in the art, is used, this solution in particular etching silicon.

The first wafer 101 may then be thinned so as to form a transferred layer 106 having a predetermined thickness e (Figure 1F). This thickness e may reach for example about 10 μm.

Oxidation of the composite structure 100 (Figure 1C) before the trimming operation prevents the second wafer 102 from being chemically etched by the TMAH solution during the chemical trimming step. The oxide layer 110 also protects the surface of the first wafer 101 from the trimming chemical etch, before it is thinned.

The Applicant has however observed the appearance of defects at the edges of the composite structures obtained after the chemical trimming step.

More specifically, the defects observed are nicks distributed over the edges (or edge face) of the second wafer of the composite structures.

These nicks are undesirable for the fabricator since they may, for example, be the source of flakes coming from the second wafer, these flakes being liable to contaminate the exposed surface of the first wafer. More generally, these defects attest to a non-optimized fabrication process and as a result the multilayer structures thus produced are less attractive. These defects may moreover cause various problems during supplementary technological steps on these defective composite structures (for example during the fabrication of microcomponents on the exposed surface of the first wafer).

It is therefore necessary to produce composite structures without such defects even when the process for fabricating these structures comprises one or more steps implementing chemical etches. Such chemical etches may occur especially, but not exclusively, during a trimming or thinning operation on the first wafer.

Document US2009/170287 (D1) relates to a process for fabricating an SOI substrate that uses a cleave technique to transfer a layer. Many processing steps (bonding, heat treatment, lift-off, etching, oxidation) are carried out between successive anneals so that, as a result, it is not the same structure that undergoes each anneal in D1. This document discloses localized oxidations at different moments in the fabrication process.

Objective and summary of the invention

For this purpose, the invention provides a process for annealing a structure comprising at least one wafer, the annealing process comprising a first step for annealing the structure in an oxidizing atmosphere so as to form an oxide layer on at least part of the exposed surface of the structure, the structure being in contact with a holder in a first position, characterized in that the process furthermore comprises:

- a step of shifting the structure on the holder into a second position in which the region or regions of contact between the structure and the holder during the first annealing step are exposed; and
- a second annealing step for annealing the oxidized structure in the second position in an oxidizing atmosphere.

The annealing process of the invention is in particular applicable to multilayer structures. As indicated above, the expression "multilayer structure" is understood to mean a structure produced by transferring at least a first wafer onto a second wafer (or support substrate), such as, for example, BSOI structures.

The annealing process of the invention is also applicable to a single wafer, the latter possibly being assembled with one or more other wafers later on.

The process according to the invention allows an oxide layer to be grown on the region or regions of the structure that are in contact with the holder during the first annealing step. In this way a uniform oxide layer is formed on the entire exposed surface of the substrate or substrates subjected to the annealing process according to the invention.

This oxide layer protects the structure from subsequent chemical etches that may be carried out on the structure.

For example, this oxide layer effectively protects the structure from chemical etches that may be implemented during a thinning or trimming operation on all or part of the structure.

The oxide layer thus formed also protects the structure from chemical etches implemented during an operation of chemically treating all or part of the structure.

Thus, the annealing process prevents the formation of nicks on the structure, especially on its edges, during a chemical etch.

The holder may for example be a plurality of holding elements allowing the structure to be held in position.

Moreover, the shifting step may comprise rotating the structure through a predetermined angle relative to the holder so that all the regions of the structure in contact with the support during the first annealing step are no longer in contact with the holder after the shifting step.

In this way it is possible to grow an oxide layer on all the regions of the structure that were in contact with the holder during the first annealing step. This oxide layer is advantageous in that it protects all the structure from chemical etches that may be subsequently implemented. It is thus possible to prevent the formation of nicks on the surface of the structure when a chemical etch is implemented later on.

The angle through which the structure is rotated during the shifting step may for example be between 40° and 90°.

The invention also relates to a first process for fabricating a heterostructure comprising a step of bonding a first wafer to a second wafer, characterized in that the process furthermore comprises annealing the heterostructure according to the annealing process defined in one of the abovementioned embodiments.

The first process for fabricating a heterostructure allows a heterostructure, comprising a first wafer and a second wafer, to be produced without nicks being formed on the second wafer during the chemical trimming step.

In particular, this process prevents the formation of nicks on the edges of the second wafer.

The anneal carried out on the heterostructure is preferably carried out in such a way that all the regions of the second wafer in contact with the holder during the first annealing step are no longer in contact with the holder after the shifting step. In this way, a protective oxide layer is formed over the entire exterior surface of the second wafer, this oxide layer protecting the second wafer from chemical etches that may be subsequently implemented.

Moreover at least one of the following steps may be carried out after the heterostructure has been annealed:

- a thinning step, for thinning said first wafer; and
- a chemical trimming step, for trimming said first wafer.

The expression "chemical trimming" is understood here to mean a trimming operation implementing at least one chemical etch.

The invention furthermore relates to a second process for fabricating a heterostructure comprising a step of bonding a first wafer to a second wafer, characterized in that the process furthermore comprises, before the bonding step, annealing the second wafer according to the annealing process defined in one of the abovementioned embodiments.

This process for fabricating a heterostructure allows an oxide layer to be formed on the surface of the second wafer, this layer effectively protecting the second wafer from chemical etches.

The second process may furthermore comprise, before the bonding step, a step of forming at least one microcomponent in the first wafer.

This process is advantageous because the first wafer does not undergo the first and second annealing steps. In this way, the components formed beforehand in the first wafer are not damaged during the first and second annealing steps.

The second process for fabricating a heterostructure may furthermore comprise an annealing step for stabilizing or strengthening the bonding interface of the heterostructure.

This annealing step for stabilizing or strengthening the bonding interface allows the bond between the first and second wafer to be strengthened.

Moreover, at least one of the following steps may be carried out after this anneal for stabilizing or strengthening the bonding interface:

- a thinning step, for thinning said first wafer; and
- a chemical trimming step, for trimming said first wafer.

The oxide layer formed on the second wafer thus serves as protection from chemical etches implemented especially during subsequent thinning and/or chemical trimming steps.

Brief description of the drawings

Other features and advantages of the present invention will become clear from the description given below with reference to the appended drawings that illustrate an exemplary embodiment. In the figures:

- Figures 1A to 1F are schematic views of a stabilizing annealing process known from the prior art;
- Figures 2A to 2C illustrate schematically the mechanism forming the nicks on the edges of a heterostructure during its fabrication process;
- Figures 3A to 3D show schematically a first process for fabricating a heterostructure according to the invention ;
- Figure 4 shows, in the form of a flow chart, the steps of the first process for fabricating a heterostructure illustrated in Figures 3A to 3D ;

- Figures 5A to 5E show schematically a second process for fabricating a heterostructure according to the invention; and
- Figure 6 shows, in the form of a flow chart, the steps of the second process for fabricating a heterostructure illustrated in Figures 5A to 5C.

Detailed description of one embodiment

The present invention is generally applicable to an anneal carried out in several steps on a structure comprising at least one wafer.

The wafer or wafers making up the structure generally has/have a circular outline and may have various diameters, especially diameters of 100 mm, 200 mm and 300 mm. However, the wafers may also be of any shape - rectangular for example.

A composite structure, or heterostructure, is fabricated by bonding a first wafer to a second wafer that acts as the support substrate for the first wafer.

As indicated above, the Applicant noticed the appearance of nicks on the edges of composite structures that had undergone a chemical etch, such as that during a trimming or a thinning operation implementing a chemical phase, when the structure had previously undergone a standard stabilizing anneal in an oxidizing atmosphere. These nicks were especially observed on the edges of the second wafer of the composite structure.

An in-depth study of these nicks allowed the mechanism forming these defects to be demonstrated and a process for preventing their formation to be developed.

The mechanism that causes these defects will now be described with reference to Figures 2A to 2C.

Figure 2A shows an exemplary composite structure similar to that described in Figure 1B, namely a composite structure 200 formed by assembling a first wafer 201 and a second wafer 202.

Preferably at least one of the two wafers 201 and 202 has been oxidized before bonding. This oxidation makes it possible in particular for there to be an oxide layer intermediate between the two wafers once the bonding is completed. In the example described here, the first wafer 201 is oxidized before bonding so as to form an oxide layer (not shown in the figures) over the entire surface of the first wafer.

In the example described here, the two wafers are made of silicon and the wafers are assembled using the technique of direct bonding, well known to those skilled in the art. Other bonding techniques can however be used, such as for example anodic, metallic or adhesive bonding.

As a reminder, the principle of direct bonding is based on direct contact between two surfaces - that is to say with no specific material (adhesive, wax, braze, etc.) being used. To carry out such an operation, it is necessary for the bonding surfaces to be sufficiently smooth, particle- and contamination-free, and for said surfaces to be placed so close that contact is initiated – typically a distance of less than a few nanometres is required. In this case, the attractive forces between the two surfaces are strong enough that direct bonding occurs, i.e. bonding induced by the Van der Waals forces between the atoms or molecules of the two surfaces to be bonded.

Moreover, the first wafer 201 has a chamfered edge, namely an edge comprising a top chamfer 204 and a bottom chamfer 205. In Figure 2A the wafers have rounded chamfers. However, the wafers may have various forms of chamfer or edge rounding, such as a bevel.

Figure 2B shows schematically the composite structure 200 seen from the side of the first wafer 201. The reference position "A" shown at the edge of the first wafer 201 corresponds for example to a flat or a notch.

The composite structure 200 is placed on a holder 212 (sometimes called a boat) so as to continue with a standard anneal in an oxidizing atmosphere. The anneal here is a stabilizing anneal that has the objective of strengthening the bond between the first wafer 201 and the second wafer 202 and of forming a protective oxide layer.

In this example, the holder 212 comprises four holding elements 212A, 212B, 212C and 212D configured to hold the composite structure 200 in position. The holding elements are in contact with the edges (or edge-face) of the composite structure 200 and more particularly in contact with the edges (or edge-face) of the second wafer 202. The edge portions of the second wafer 202 in contact with the holding elements are referenced by the contact regions 213A, 213B, 213C and 213D, respectively (and denoted collectively as contact regions 213).

The composite structure 200 and its holder 212 are placed in an oven or any other piece of equipment designed to carry out an anneal (not shown in the figures). A stabilizing anneal is carried out on the composite structure 200 at a temperature T1 of between, for example, 900°C and 1200°C, typically at 1100°C, for two hours.

The anneal forms an oxide layer on the exposed surface of the first wafer 201 and of the second wafer 202.

Next, a hybrid trimming step is carried out on the first wafer 201 as described with reference to figures 1D and 1E. In the example described here, the hybrid trimming comprises a first partial, mechanical trimming step using a grinding wheel or a blade followed by a selective chemical etching step for etching the first wafer using a TMAH etching solution.

This trimming operation allows the excess part at the edge of the first wafer 201 to be removed without damaging the second wafer 202. It is possible to preserve the second wafer 202 because the oxide layer (not shown) intermediate between the two wafers acts as a stop layer for the chemical etching. The chemical etching is thus stopped at the periphery of the first wafer 201 on the oxide layer located at the bonding interface between the two wafers.

Once the trimming is completed, the first wafer 201 may be thinned so as to form a transferred layer 206 having a predetermined thickness e, for example of about 10 μm.

Thinning is carried out using a grinding wheel or any other tool capable of mechanically wearing away (or grinding) the material of the first wafer.

Figure 2C shows schematically the structure 200 once the stabilizing anneal, the hybrid trimming and the thinning have been carried out.

The applicant noticed the appearance of nicks 214A, 214B, 214C and 214D (collectively reference 214) on the edge of the second wafer 202 after the TMAH chemical etch. The distribution of these defects along the edge of the second wafer 202 corresponds to the positions of the abovementioned contact regions 213.

In fact, during the stabilizing anneal of the composite structure 200 an oxide layer (SiO_2 in the present example) forms on all the exposed

surface of the composite structure 200, except in the contact regions 213. This is because, during the stabilizing anneal, the holding elements 212A to 212D locally mask the edge of the second wafer 202 so that the contact regions are not covered by an oxide layer.

Added to this masking effect may be another effect, namely the deterioration of the oxide possibly present on the structure at the contact points (lift-off, scratching during removal or other movements of the wafer, etc.). The holding elements 212 may in fact locally damage the preliminary oxide layer formed on the first wafer 201 (or optionally on the second wafer 202) before bonding and/or the oxide layer that forms near the contact points 213 during the stabilizing anneal.

As the contact regions 213 of the second wafer 201 have no protective oxide layer, these regions are directly subjected to the chemical etching action of the TMAH solution during the thinning and/or chemical trimming step. The chemical etching of the contact regions 213 then generates the nicks 214. The nicks 214A, 214B, 214C and 214D have thus been observed on the second wafer 202 in the positions of the contact regions 213A, 213B, 213C and 213D, respectively. The larger the regions not protected by the oxide are, the greater the etching effect of the TMAH solution.

These surface defects generated on the edge face of the second wafer 202 are prejudicial for the reasons already mentioned above.

For this purpose, the present invention proposes to carry out an anneal in several steps, shifting the structure on the support between two consecutive annealing steps so as to prevent the appearance of these nicks especially on the edge face (or edges) of the second wafer.

One particular implementation of the annealing process and a first process for fabricating a heterostructure according to the invention will now be described with reference to Figure 3A to 3D and 4.

As illustrated in Figure 3A, the first wafer 301, having a top chamfer 304 and a bottom chamfer 305, is firstly bonded to a second wafer 302 that also has chamfered edges, so as to form a composite structure 300 (step E1).

In the example described here, the first and second wafers 301 and 302 are made of silicon. The wafers may however be made of other materials.

The first wafer 301 and/or the second wafer 302 may furthermore, and preferably, be covered, before bonding, with an oxide layer (not shown in the figures), in the context, for example, of the fabrication of BSOI multilayer structures.

In the example described here, the wafers are assembled using direct bonding. However, as indicated above, other types of bonding may also be envisaged.

Figure 3B shows schematically the composite structure 300 seen from one side of the first wafer 301. The reference position "B" shown at the edge of the first wafer 301 corresponds for example to a flat or a notch.

The composite structure 300 is placed on the holder 312. In this first position, the four holding elements 312A, 312B, 312C and 312D of the holder 312 are thus in contact with the contact regions 313A, 313B, 313C and 313D, respectively (collectively denoted as contact regions 313), of the second wafer 302. In this example, the contact regions 313 are distributed along the edge of the second wafer 302.

However, it is possible to envisage the contact regions being located on the backside of the second wafer 302, for example.

The composite structure 300 and its holder 312 are then placed in an oven or any other piece of equipment (not shown in the figures) allowing a first anneal to be carried out on the composite structure 300 in an oxidizing (dry or wet) atmosphere (step E2).

In this example, the first anneal is carried out at a temperature T2 of between 1000°C and 1200°C. This first anneal serves as stabilizing anneal for the composite structure 300 since it allows the bond between the first wafer 301 and the second wafer 302 to be strengthened.

This first anneal furthermore allows an oxide layer 310 to grow on the exterior surface of the composite structure 300 and in particular on the exterior surface of the second wafer 302. The expression "exterior surface of the second wafer" is here understood to mean the entire surface of the second wafer apart from the bonding interface.

The principal objective of this oxide layer is to protect the exterior surface of the second wafer 302 from subsequent chemical etches, especially during thinning and/or chemical trimming operations on the first wafer 301.

In the case of a process for fabricating a BSOI multilayer structure, the oxide layer 310 thus formed may reach a thickness for example of about 1 μm.

Once the first annealing step E2 is completed, the composite structure 300 is removed from the oven. An oxide layer 310 is then present over the entire exterior surface of the composite structure 300, apart from the contact regions 314 distributed along the edge of the second wafer 302.

It should be noted that edge regions of the first wafer may also be in contact with the holder during the anneal. In this case, these regions also have no protective oxide layer after the first annealing step E2.

As illustrated in figure 3C, the composite structure 300 on the holder is then shifted by rotating it through a predetermined angle θ_1 with respect to the holder 312 (step E3). This rotation may be carried out manually or by using a suitable positioning device (an aligner for example). The composite structure 300 is thus positioned on its holders 312 in a second position angularly offset by an angle θ_1 with respect to the first position (Figure 3B).

Once the rotation has been carried out, the contact regions 312 of the second wafer 302 are no longer in contact with the holding elements 312.

The angle of rotation θ_1 is therefore chosen depending on the geometry of the holder 312 used and, more particularly, depending on the placement of the holding elements 312A to 312D along the edge of the second wafer 302.

In one particular implementation of the invention, the angle of rotation θ_1 is between 40° and 90°.

In the example described here in Figure 3C, the composite structure 300 is turned through an angle of rotation θ_1 of about 40°.

The composite structure 300 and its holder 312 are then put back in an oven (or any other suitable piece of equipment) so as to continue with a second annealing step in an oxidizing (dry or wet) atmosphere (step E4).

This second anneal is carried out at a temperature T3 of between 900°C and 1200°C, for example.

This second annealing step E4 allows an oxide layer to grow on the former (unoxidized) contact regions 314 of the second wafer 302. Such an oxidation is possible because the holding elements of the holder 312 no longer protect the contact regions 314 from the oxidizing atmosphere.

As necessary, this second annealing step also allows the surface of the regions of the first wafer 301 that were in contact with the support 312 during the first annealing step E2 to be oxidized.

It should be noted that it is not necessary to grow an oxide layer as thick as that grown during the first stabilizing annealing step. The second annealing step E4 may be configured so as to form a layer a few hundreds of nanometres thick on the former contact regions 314.

In the context of a process for fabricating a BSOI multilayer structure for example, the second annealing step E4 may be carried out at a temperature T3 = 950°C so as to form an oxide layer about 500 nm thick on the former contact regions 314.

After the second annealing step E4, an oxide layer is then present on the entire exterior surface of the composite structure 300 and in particular on the entire exterior surface of the second wafer 302 (including the edge of the second wafer 302)

In the example described here, the process then continues with the hybrid trimming (step E5) and then with the thinning (step E6) of the first wafer (Figure 3D).

The hybrid trimming operation (step E5) comprises a mechanical first trimming step followed by a chemical trimming step, as explained with reference to figures 1D and 1E.

More particularly, the mechanical trimming step allows the top chamfered edge 304 to be removed from the first wafer 301. Once the mechanical trimming is completed, the annular portion remaining on the periphery of the first wafer 201 is no longer protected by the oxide. It is then possible to continue with the chemical trimming of this remaining annular portion using a chemical etching solution, this step allowing the bottom chamfered edge 305 to be removed from the first wafer 301. In the example described here, a TMAH solution is used to etch the silicon of the first wafer. Other chemical etching solutions may however be envisaged, these being chosen especially depending on the composition of

the first wafer to trimmed. In certain cases, a KOH solution, well known to those skilled in the art, is used.

The oxide layer 310 effectively protects the entire second wafer 302 from the chemical etch implemented during the chemical trimming step and from chemical etches that may be implemented in other technological steps during the fabrication of the composite structure (especially during the fabrication of microcomponents on the exposed surface of the first thinned wafer).

Once the trimming operation has been carried out, the first wafer 301 is thinned in an analogous way to the composite structure 200 (step E6). Thus a transferred layer 306 having a predetermined thickness is formed on the second wafer 302, this thickness possibly reaching about 10 μm for example (Figure 3D). This thickness is measured between the top side and the bottom side of the first wafer, away from the chamfered edge.

Another example of an annealing process and a second process for fabricating a heterostructure according to the invention will now be described with reference to Figures 5A to 5E and 6.

Figure 5A shows a first wafer 501 and a second wafer 502. The first wafer 501 is different from the first wafer 301 described in Figure 3A in that it furthermore comprises microcomponents 503 on one of its sides. In addition, the first wafer 501 is preferably an SOI wafer comprising a buried insulating layer (not shown in the figures) corresponding, for example, to a buried layer of silicon oxide or silicon nitride or, alternatively, to a multilayer stack of these materials.

The second wafer comprises a reference position "C" on the edge of one of its sides.

The expression "microcomponents" is understood here to mean any elements made using materials different from that of the first wafer. These microcomponents correspond especially to elements forming all or part of an electronic component or a plurality of electronic microcomponents. They may for example be active or passive components, simple contacts or interconnects or even simple cavities.

The first wafer may especially comprise microcomponents in the case of 3D-integration that requires the transfer of one or more layers of microcomponents onto a final support substrate, or even in the case of

transferring circuits, as for example in the fabrication of backside-illuminated imagers. Of course, when such microcomponents are present they must be able to withstand the oxidation heat treatment according to the invention. This is the case for example for cavities.

In this second embodiment, the anneal according to the process of the invention is carried out only on the second wafer 502.

Steps E11, E12 and E13 differ therefore from steps E2, E3 and E4, respectively, in that only the second wafer 502 undergoes a first anneal followed by a rotation and a second anneal.

More precisely, the second wafer 502 is placed on a holder (Figure 5B) and a first annealing step E11 in an oxidizing atmosphere is carried out on the second wafer 502, in an analogous way to step E2 described above. This first anneal is carried out at a temperature T4.

As illustrated in Figure 5C, the second wafer 502 is then rotated through an angle θ_2 with respect to its holder (step E12), in an analogous way to step E3 described above.

Once the rotation has been carried out, a second annealing step E13 is carried out on the second wafer 502 in an oxidizing atmosphere, in an analogous way to step E4 described above. This second anneal is carried out at a temperature T5.

After steps E11 to E13, a protective oxide layer 510 is present over the entire surface of the second wafer 502. This oxide layer covers in particular the regions of the second wafer 502 that were in contact with the holder during the first annealing step E11 (figure 5D).

Next, the first wafer 501 is bonded to the second wafer 502 (step E14), so that the microcomponents 503 are located at the bonding interface between the two wafers (Figure 5E). The wafer 501 may have been provided with a smoothing layer (made of planarized SiO_2 for example) so as to supply a more suitable contact surface.

In the example described here, the assembly is carried out using direct bonding. As explained above, other assembly techniques may however be envisaged.

The second embodiment ensures the microcomponents 503 of the first wafer 501 do not undergo the first and second anneals of the process of the invention. This is because the high temperatures that are

involved during these anneals are liable to irreversibly damage the microcomponents 503.

In this second embodiment there is therefore no protective oxide layer on the exterior surface of the first wafer 501. The first embodiment also differs from the second embodiment in that an oxide layer is present at the bonding interface between the first wafer 501 and the second wafer 502.

Once the bonding is completed, the composite structure 500 thus formed undergoes a consolidation anneal that has the objective of strengthening the bond between the first wafer 501 and the second wafer 502 (step E15). This anneal is carried out at a temperature T6 which is lower than the temperatures T4 and T5 during the first and second annealing steps E11 and E13. The temperature T6 is chosen in particular so as to not damage the microcomponents 503 of the first wafer 501. It may be an anneal between 400°C and 500°C for 30 minutes to 4 hours.

In the example described here, a thinning step (step E16) is then carried out comprising a first, mechanical (grinding) step followed by a chemical treatment that is selective with respect to the buried insulating layer of the wafer 501. An optional trimming step (E17) for trimming the first wafer 501 may then be carried out.

The oxide layer 510 allows the entire surface of the second wafer 502 to be effectively protected from chemical etches especially implemented during thinning, and optionally trimming, steps.

Moreover, in certain cases it may be necessary to carry out more than one step of shifting (rotating) the composite structure so as to allow all the regions of the second wafer and/or of the structure that were in contact with the holder during the first anneal to be oxidized. This may be the case, for example, when the contact regions represent a substantial portion of the edge of the second wafer and/or structure.

According to another implementation of the annealing process of the invention, a first annealing step, conforming to step E2 (or E11), is carried out straight away.

Next, N rotation steps (N being an integer greater than or equal to 2), each rotation step being followed by an annealing step analogous to the second annealing step E4 (or E13) described above. Each second

annealing step is configured to grow an oxide layer on at least some of the contact regions that are still unoxidized.

It is also conceivable for the shifting step of the annealing process of the invention to comprise shifting the structure relative to the holder in other ways, such as a translational movement for example, the latter possibly being combined with a rotational movement.

CLAIMS

1. Process for annealing a structure comprising at least one wafer, said annealing process comprising a first step for annealing said structure in an oxidizing atmosphere so as to form an oxide layer on at least part of the exposed surface of said structure, said structure being in contact with a holder in a first position, characterized in that said process furthermore comprises:

- a step of shifting said oxidized structure on the holder into a second position in which the region or regions of contact between the structure and the holder in said first position are exposed; and
- a second annealing step for annealing the oxidized structure in said second position in an oxidizing atmosphere.

2. Annealing process according to Claim 1, in which the shifting step comprises rotating the structure through a predetermined angle relative to said holder.

3. Annealing process according to Claim 2, in which said angle through which the structure is rotated during the shifting step is between 40° and 90°.

4. Process for fabricating a heterostructure comprising a step of bonding a first wafer to a second wafer, characterized in that said process furthermore comprises annealing said heterostructure according to the annealing process defined in any one of Claims 1 to 3.

5. Process for fabricating a heterostructure according to Claim 4, in which at least one of the following steps is carried out after said anneal:

- a thinning step, for thinning said first wafer; and
- a chemical trimming step, for trimming said first wafer.

6. Process for fabricating a heterostructure comprising a step of bonding a first wafer to a second wafer, characterized in that the process furthermore comprises, before said bonding step, annealing said second

wafer according to the annealing process defined in any one of Claims 1 to 3.

7. Process for fabricating a heterostructure according to Claim 6, furthermore comprising, before said bonding step, a step of forming at least one microcomponent in the first wafer.

8. Process for fabricating a heterostructure according to either of Claims 6 and 7, furthermore comprising an annealing step for stabilizing said heterostructure.

9. Process for fabricating a heterostructure according to Claim 8, in which at least one of the following steps is carried out after said stabilizing anneal:

- a thinning step, for thinning said first wafer; and
- a chemical trimming step, for trimming said first wafer.