

Description

BACKGROUND OF THE INVENTION

It is known in the art of digital circuitry to perform integration by using a delay element and an adder circuit. The signal to be integrated is applied to one input (addend) of the adder circuit. The output of the adder circuit is coupled to the input of the delay element, the output of which is coupled to the second input (augend) of the adder circuit. The integrated signal may be taken from either the output of the adder circuit or the output of the delay element. See for example the article by H. Urkowitz, "Analysis and Synthesis of Delay Line Periodic Filters," IRE Trans. on Circuit Theory, June 1957, pp 41-53.

Frequently it is desired to both scale and truncate the values provided by the integrator. Truncation is performed in order to reduce the number of sample bits processed, in order to reduce the size of the processing circuitry or minimize the processing time. It has been found that undesirable effects may occur if the truncation is performed in the integrator loop, that is between the delay element and the adder. These effects are manifested as inaccuracies in the processed signals, undesirable excess signal build up for certain signals and possible oscillations or limit cycles. It is an object of the present invention to provide a bit-serial integrator circuit which provides both scaling and truncation; provides integration with full bit accuracy, and requires a minimum of hardware.

SUMMARY OF THE INVENTION

The present invention according to claim 1 is directed to a bit-serial integration circuit including a signal combining means serially coupled with an R-stage shift register. The output of the R-stage shift register is coupled through an N-stage shift register to a first connection of the combining means and the signal to be integrated is coupled to a second input connection of the combining means. A gated clock source providing at least R+N pulses per sample period is coupled to the shift-registers to transfer sample bits serially therethrough. Truncated, scaled and integrated R-bit samples are available at the output connection of the R-stage shift register.

Brief Description of the Drawings

Figure 1 is a block diagram of a bit-serial integration circuit embodying the present invention.

Figure 2 is a waveform diagram useful in describing the invention.

Figure 3 is a block diagram of circuitry for eliminating the DC component of a bit-serial signal including the integration circuit of Figure 1.

Detailed Description

The invention will be described in the environment of a bit-serial gated clock system. The samples to be processed are R-bit, two's complement bit-serial samples. Referring to Figure 2, samples occur synchronously at a rate defined by the sample clock designated SC. The sample bits occur synchronously with the burst of clock pulses of the clock signal designated CLOCK R with the least significant bit (LSB) occurring first in time and the most significant or sign bit (MSB) occurring last. The period of the burst of clock pulses of CLOCK R is less than the sample period. The pulses of the clocking signal CLOCK R are developed from a system clock designated CLOCK which is a continuous waveform.

Referring to Figure 1, the integration circuit includes an adder 12 having a first input terminal 10 at which samples to be integrated are applied. The output of the adder 12 is coupled to a sign-extend-shift-register (SXS) 14 including an R-stage serial shift register 16 and a transparent latch (TL) 18. The transparent latch 18 is controlled by a bilevel control signal XND and passes sample bits unaltered for signal XND in a first state and latches the bit occurring concurrently with a transition of the signal XND going from the first state to a second state and holds and outputs that bit for the duration that signal XND is in the second state. The output of the transparent latch is a scaled output of the integrated signal. The output of the serial register 16 is coupled to an N-stage serial shift register 22, the output of which is coupled to a second input of adder 12. Shift registers 22 and 16 are clocked with bursts of (R+N) clock pulses per sample period by clock signal CLOCK (R+N) whose relationship to CLOCK (R) is shown in Figure 2.

The control signal XND (illustrated in Figure 2) undergoes a transition from the first to second state during the Rth clock pulse so that the Rth sample bit output by register 16 is latched and therefore replicated for the remainder of the duration of the current sample period.

The clock signals are generated by, for example, an oscillator 23 which develops the system clock, CLOCK, and a clock generator 24. The clock generator 24 responsive to the system clock develops the signals CLOCK (R), CLOCK (R+N), XND and if required signal SC. These signals are developed in clock generator 24 by conventional means, the details of which are not part of this invention, which circuitry one skilled in the art of signal processing will readily be capable of designing knowing the timing relationships illustrated in Figure 2.

Consider a sequence of R-bit, two's complement, bit-serial samples being applied to input connection 10 with the Rth or sign bit of each sample replicated for the duration of the respective sample period after the occurrence of the R-1 value bits. The sign bit rep-

lication may be provided for example by applying the samples to connection 10 via a transparent latch controlled by the control signal XND. Assume also that the contents of registers 16 and 22 are initially zero valued and that adder 12 imposes no processing delay on the applied signal. During the sample period that the first sample is applied, since the contents of register 16 and 22 are zero valued, the first sample passes through adder 12 unchanged and, after the first R pulses of clock signal CLOCK (R+N), is resident in shift register 16. During this interval the output OUT is zero valued, that is the zero valued contents originally in register 16 are passed through the transparent latch 18. Latch 18 latches the Rth output bit and replicates it for the duration of the sample period thus precluding further bit values provided by register 16, during the sample period, from being placed on terminal OUT.

Register 16 is clocked for an additional N clock periods providing the N LSB's of the sample to the N-stage shift register 22. At the beginning of the next sample period, the first sample is thus available at the second input of adder 12 and properly justified for addition to the next applied sample. That is the LSB and subsequent bits of the first sample resident in register 22 will occur coincidentally with the LSB and corresponding bits of the subsequent (second) sample applied to connection 10.

At the end of the first sample period (and every subsequent sample period) only the R MSB's of the sum samples are resident in register 16 since register 16 is an R-stage register and it is clocked with R+N pulses. (Note that even though the input samples are R-bits wide, the sum samples can expand to R+N bits wide.) During each subsequent sample period the R MSB's of the sums are provided as the output signal OUT via the transparent latch 18. The R MSB's of the sum samples are output coincident with the first R pulses of the burst of clock pulses. The output samples are representative of the sum samples provided by adder 12, truncated and shifted to N lesser significant bit positions. The shifting of the sum samples to N lesser significant bit positions is equivalent to scaling the sum samples by a factor of 2^{-N} .

The samples fed back to the adder 12 via register 22, however, are not truncated nor are they scaled. Thus the integration is performed with full precision.

Designating the values of the input samples as A, the sum samples as B, and the samples fed back via register 22 as C, the transfer function of the circuit is derived as follows. The sample C is equal to the sample B delayed by one sample period and using conventional Z-transform notation

$$C = BZ^{-1} \quad (1)$$

Sum samples B are equal to

$$B = A + C \quad (2)$$

or

$$B = A + BZ^{-1} \quad (3)$$

collecting terms and rearranging equation (3)

$$B/A = 1/(1 - Z^{-1}) \quad (4)$$

Equation (4) describes the integration function in Z-transform notation.

Designating the output samples OUT as D

$$D = 2^{-N} BZ^{-1} \quad (5)$$

and substituting (4) in (5) the transfer function D/A is given by

$$D/A = 2^{-N} Z^{-1}/(1 - Z^{-1}) \quad (6)$$

indicating that the output equals the integration of the input signal delayed one sample period and scaled by 2^{-N} .

In the arrangement of Figure 1, the sums provided by adder 12 may expand to bit widths of R+N since there are a total series combination of R+N shift register stages. Further if it is desired to feed back to adder 12, sum samples scaled by 2^{-X} , then the number of stages of register 22 may be reduced by X and a transparent latch interposed between register 22 and adder 12 which latch being conditioned to latch and replicate the sample bit occurring at the (R+N-X)th clock pulse.

In the Figure 1 arrangement, it was assumed that adder 12 imposed no processing delays. If, however, adder 12 imposes Y bit periods of processing delay, then the samples B will be multiplied by 2^Y and the transfer function B/A will be altered.

This factor may be partially compensated by reducing the number of stages in register 22 by Y stages. In this instance the transfer functions B/A and D/A are given by

$$B/A = 2^Y/(1 - Z^{-1}) \quad (7)$$

and

$$D/A = 2^{-(N-Y)} Z^{-1}/(1 - Z^{-1}) \quad (8)$$

Alternatively if the adder imposes Y bit-periods of processing delay, the transfer functions of equations (4) and (6) can be maintained intact by increasing the number of pulses in each burst of clock pulses by Y with no other changes made to the circuit elements 16 and 22. In this instance, the clock signals applied to registers 16 and 22 will contain R+N+Y pulses in each burst.

Refer next to Figure 3. The elements in Figure 3 designated with the same numbers as elements in Figure 1 are presumed identical. The circuitry in Figure 3 may be employed to remove a DC component from a bit-serial signal such as a bit-serial audio signal. Presume for example that the signal applied to terminal 32 is an unsigned straight binary signal from an analog-to-digital convertor and all values are positive. The conversion process inherently imposes a DC reference on the digitized signal. The audio signal from, for example, a broadcast source is nominally an AC signal. The DC component, if not removed, will in general, require that the processing circuitry be capable of processing a signal of greater dynamic range than that required by the AC audio signal. Thus to minimize the overall signal processing hardware it is de-

sirable to remove the DC component.

The Figure 3 circuit includes a bit-serial two's complement subtractor circuit 30 and an integrator circuit as described with reference to Figure 1. The input signal (AIN) is coupled to the minuend input of the subtractor 30 and the integrator terminal OUT is coupled to the subtrahend input of the subtractor 30. Note in fact, that the subtractor 30 and adder 12 may in fact be interchanged if the signal AC_{OUT} is coupled to the subtrahend input of the subtractor interchanged with adder 12.

The signal AC_{OUT} is equal to the difference of the signal AIN minus the output OUT from the integrator. The signal OUT from the integrator is, from equation (6),

$$OUT = AC_{OUT}Z^{-N} / (1 - Z^{-1}) \quad (9)$$

Therefore,

$$AC_{OUT} = AIN - AC_{OUT}Z^{-N} / (1 - Z^{-1}) \quad (10)$$

Collecting terms and rearranging the transfer function AC_{OUT}/AIN of the figure 3 circuit can be shown to be

$$AC_{OUT}/AIN = (Z - 1) / (Z - 1 + Z^{-N}) \quad (11)$$

For sample periods that are small relative to the signal of interest, this transfer function contains a zero at zero Hz and a pole at approximately $2^{-N}f_s/2\pi$ Hz, where f_s is the sample frequency. The audio bandwidth is 20Hz-20kHz. Assume a sample rate of 300kHz to satisfy the criteria that the sample period be small relative to the period of the maximum audio-frequency. In order not to lose any of the audio signal spectrum the pole must be at a frequency less than 20Hz or

$$2^{-N}f_s/2\pi < 20. \quad (12)$$

This condition is satisfied for N less than 11. For N equal to 12 the 3dB point is at 11.6 Hz and for N equal to 13 the 3dB point is reduced to 5.8Hz. Thus the AC audio signal will pass substantially with no amplitude loss and the DC component will be completely eliminated.

Now assume that the subtractor 30 and adder 12 each impose a one-bit period delay on the signal samples. Relative to the sample datum established in a gated clock system, a one bit period delay effectuates a multiplication by a factor of two. The output from subtractor 30 becomes

$$AC_{OUT} = 2(AIN - OUT) \quad (13)$$

The signal OUT, in accordance with equation (8) becomes

$$OUT = AC_{OUT}Z^{-N} / (1 - Z^{-1}) \quad (14)$$

Substituting (14) in (13), collecting terms and transposing, the transfer function can be shown to be

$$AC_{OUT}/AIN = 2(Z - 1) / (Z - 1 + 2 \cdot Z^{-(N-2)}) \quad (15)$$

Again there is a zero at zero Hertz, however, in this instance the pole is at $2^{-(N-2)}f_s/2\pi$ Hz and the amplitude is increased by a factor of two. To establish the pole at the same frequency as the previous example, N must be increased by two.

In the claims that follow, the phrase "burst of

clock pulses" is recited. The "burst of clock pulses" may occupy an entire sample period or it may occupy less than an entire sample period depending on the particular circuit elements selected i.e. the number of register stages and the sample period. If the burst occupies the entire sample period, the clock signal will occur as a continuous string of pulses, that is, successive bursts will be immediately adjacent one another without apparent separation. The term "burst of clock pulses" as used in the claims is intended to include this contingency.

Claims

1. A bit-serial integrator circuit for integrating a bit-serial signal comprising:

a signal input terminal (IN) for applying a bit-serial signal;

combining means (12) for combining bit-serial signals, having a first input terminal coupled to said signal input terminal, a second input terminal and an output terminal;

a first serial shift register (16) having R stages, R an integer, an input terminal coupled to the output terminal of said combining means (12), an output terminal and a clock input terminal; and characterized by

a second serial shift register (22) having N stages, N being an integer, an input terminal coupled to the output terminal of said first serial shift register (16), an output terminal coupled to the second input terminal of said combining means, and a clock input terminal;

means (23,24) for applying a burst of clock pulses to the clock input terminals of said first (16) and second (22) serial shift registers, the pulses in said burst being synchronous with occurring bits of said bit-serial signal, and the number of pulses in said burst being at least R+N per sample period; and

transparent latch means (18) coupled to the output terminal of said first serial shift register (16) for passing sample bits during a first predetermined portion of said burst and latching and outputting a predetermined sample bit for the duration of each sample period following said predetermined portion.

2. The bit-serial integrator set forth in Claim 1 characterized in that said means (23,24) for applying a burst of clock pulses provides a burst of pulses equal in number to an integer number of bit-delay periods between an input terminal of said combining means (12) and the output terminal of said second serial shift register (22).

3. The bit-serial integrator set forth in Claim 2 char-

acterized in that said combining means (12) has a processing delay of one sample bit period between its input and output terminals and said means for applying a burst of clock pulses provides a burst of pulses equal in number to $R+N+1$.

4. The bit-serial integrator set forth in Claim 3 further characterized by:

a further bit-serial combining means (30) having a first input terminal coupled to the output terminal of said bit-serial transparent latch means (18), an output terminal coupled to the first input terminal of said combining means (12) and at which a processed signal is available, and having a second input terminal; and

means (AIN) for applying a bit-serial signal to the second input terminal of said further bit-serial combining means (30).

Patentansprüche

1. Bitserieller Integrator zur Integration eines bitseriellen Signals mit

- einem Signaleingang (IN) zur Zuführung eines bitseriellen Signals,
- einer Kombinationsschaltung (12) für bitserielle Signale mit einem mit dem Signaleingang gekoppelten ersten Eingang, einem zweiten Eingang und einem Ausgang,
- einem ersten seriellen Schieberegister (16) mit R-Stufen, wobei R eine ganze Zahl ist, das mit seinem Eingang an den Ausgang der Kombinationsschaltung (12) angeschlossen ist und einen Ausgang sowie einen Takteingang hat,

gekennzeichnet durch

- ein zweites seriellcs Schieberegister (22) mit N-Stufen, wobei N eine ganze Zahl ist, das mit einem Eingang an den Ausgang des ersten seriellen Schieberegisters (16) angeschlossen ist und mit seinem Ausgang an den zweiten Eingang der Kombinationsschaltung angeschlossen ist und einen Takteingang hat,
- eine Einrichtung (23,24) zur Zuführung einer Taktimpulsgruppe zu den Takteingängen des ersten und des zweiten seriellen Schieberegisters (16,22), wobei die Impulse der Gruppe synchron mit dem Auftreten der Bits in dem bitseriellen Signal sind und die Anzahl der Impulse der Gruppe mindestens $R+N$ pro Abtastperiode beträgt, und
- eine transparente Verriegelungsschaltung (18), die mit dem Ausgang des ersten seriellen Schieberegisters (16) gekoppelt ist, um die Abtastbits während eines ersten vorbestimmten Teils der Gruppe passieren

zu lassen und ein vorbestimmtes Abtastbit während der diesem vorbestimmten Teil folgenden Dauer jeder Abtastperiode zu verriegeln und auszugeben.

2. Bitserieller Integrator nach Anspruch 1, dadurch gekennzeichnet, daß die Einrichtung (23,24) zur Zuführung einer Taktimpulsgruppe eine Gruppe von Impulsen liefert, deren Anzahl gleich einer ganzzahligen Zahl von Bit-Verzögerungsperioden zwischen einem Eingang der Kombinationsschaltung (12) und dem Ausgang des zweiten seriellen Schieberegisters (22) ist.

3. Bitserieller Integrator nach Anspruch 2, dadurch gekennzeichnet, daß die Kombinationsschaltung (12) zwischen ihrem Eingang und ihrem Ausgang eine Verarbeitungsverzögerung von einer Abtastbitperiode aufweist und daß die Einrichtung zur Zuführung einer Taktimpulsgruppe eine Gruppe von Impulsen liefert, deren Anzahl gleich $R+N+1$ ist.

4. Bitserieller Integrator nach Anspruch 3, dadurch gekennzeichnet, daß eine weitere bitserielle Kombinationsschaltung (30) mit einem ersten Eingang an den Ausgang der bitseriellen transparenten Verriegelungsschaltung (18) angeschlossen ist und mit einem Ausgang an den ersten Eingang der Kombinationsschaltung (12) angeschlossen ist und an diesem ein verarbeitetes Signal liefert, und mit einem zweiten Eingang an eine Einrichtung (AIN) zur Zuführung eines bitseriellen Signals angeschlossen ist.

Revendications

1. Circuit intégrateur en série par bit pour intégrer un signal en série par bit comprenant :

- une borne d'entrée de signal (IN) pour appliquer un signal en série par bit;
- des moyens de combinaison (12) pour combiner des signaux en série par bit, ayant une première borne d'entrée couplée à ladite borne d'entrée de signal, une seconde borne d'entrée et une borne de sortie ;
- un premier registre à décalage série (16) ayant R étages, R étant un nombre entier, une borne d'entrée couplée à la borne de sortie desdits moyens de combinaison (12), une borne de sortie et une borne d'entrée d'horloge et caractérisé par :
- un second registre à décalage série (22), ayant N étages, N étant un nombre entier, une borne d'entrée couplée à la borne de sortie dudit premier registre à décalage série (16), une borne de sortie couplée à ladi-

- te seconde borne d'entrée desdits moyens de combinaison et une borne d'entrée d'horloge;
- des moyens (23,24) pour appliquer une rafale d'impulsions d'horloge aux bornes d'entrée d'horloge desdits premier (16) et second (22) registres à décalage série, les impulsions de ladite rafale étant synchrones aux bits survenant dudit signal en série par bit, et le nombre d'impulsions dans ladite rafale étant au moins $R + N$ par période d'échantillon ; et, 5 10
 - des moyens de bascule transparents (18) couplés à la borne de sortie dudit premier registre à décalage série (16) pour laisser passer des bits échantillons pendant une première portion prédéterminée de ladite rafale et verrouiller et extraire un bit échantillon prédéterminé pendant la durée de chaque période échantillon suivant ladite portion prédéterminée. 15 20
2. Intégrateur en série par bit selon la revendication 1, caractérisé en ce que lesdits moyens (23,24) pour appliquer une rafale d'impulsions d'horloge fournissent une rafale d'impulsions dont le nombre est égal à un nombre entier de périodes de retard de bit entre une borne d'entrée desdits moyens de combinaison (12) et la borne de sortie dudit second registre à décalage série (22). 25 30
3. Intégrateur en série par bit selon la revendication 2 caractérisé en ce que lesdits moyens de combinaison (12) comportent un retard de traitement d'une période de bit échantillon entre ses bornes d'entrée et de sortie et lesdits moyens pour appliquer une rafale d'impulsions d'horloge fournissent une rafale d'impulsions dont le nombre est égal à $R + N + 1$. 35 40
4. Intégrateur en série par bit selon la revendication 3 caractérisé en outre par : 40
- des moyens supplémentaires de combinaison bit-série (30) ayant une première borne de sortie couplée à la borne de sortie desdits moyens de bascule transparents en série par bit (18), une borne de sortie couplée à ladite première borne d'entrée desdits moyens de combinaison (12) et à laquelle un signal traité est disponible et comportant une seconde borne d'entrée et, 45 50
 - des moyens (AIN) pour appliquer un signal en série par bit à ladite seconde borne d'entrée desdits moyens supplémentaires de combinaison en série par bit (30). 55