



- (51) International Patent Classification:
H01L 27/115 (2006.01) *H01L 21/8247* (2006.01)
- (21) International Application Number:
PCT/US2012/040891
- (22) International Filing Date:
5 June 2012 (05.06.2012)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
13/153,707 6 June 2011 (06.06.2011) US
- (71) Applicant (for all designated States except US): **MICRON TECHNOLOGY INC.** [US/US]; 8000 S. Federal Way, Mail Stop 525, Boise, ID 83716 (US).
- (72) Inventors: **BANNA, Srinivasa, R.**; 3924 Emerald Isle Lane, San Jose, CA 95135 (US). **VAN BUSKIRK, Michael, A.**; 18653 Vessing Road, Saratoga, CA 95070 (US). **THURGATE, Timothy**; 1363 Arleen Avenue, Sunnyvale, CA (US).
- (74) Agents: **ANDERSON, Thomas, E.** et al.; Wilmer Cutler Pickering Hale And Dorr LLP, 1875 Pennsylvania Avenue, NW, Washington, DC 20006 (US).
- (81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
- (84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM,

[Continued on next page]

(54) Title: TECHNIQUES FOR PROVIDING A SEMICONDUCTOR MEMORY DEVICE

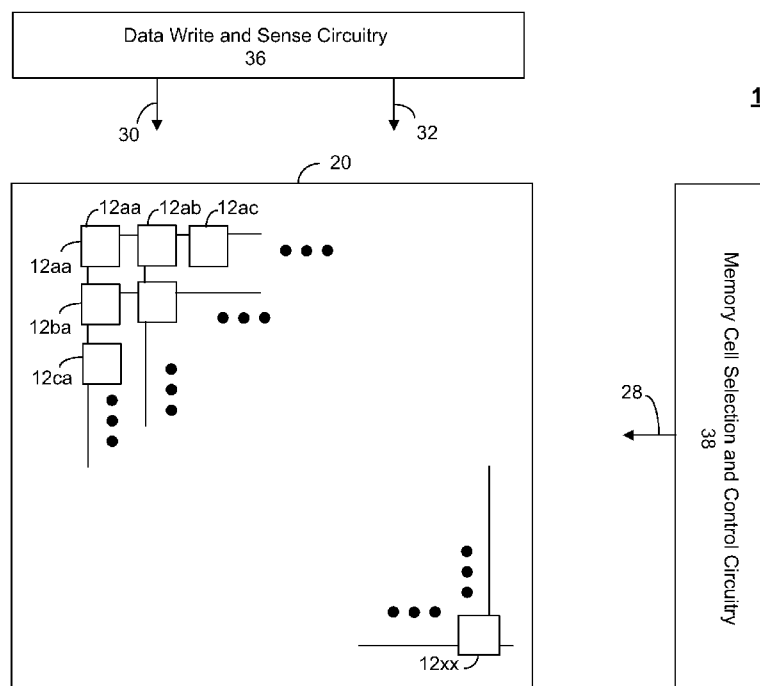


FIGURE 1

(57) Abstract: Techniques for providing a semiconductor memory device are disclosed. In one particular embodiment, the techniques may be realized as a semiconductor memory device including a plurality of memory cells arranged in an array of rows and columns. Each memory cell may include a first region coupled to a source line, a second region coupled to a bit line, and a body region capacitively coupled to at least one word line via a tunneling insulating layer and disposed between the first region and the second region.



TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, **Published:**
ML, MR, NE, SN, TD, TG).

— *without international search report and to be republished
upon receipt of that report (Rule 48.2(g))*