"Interface circuit of the slave type working with a serial bus".

Description

The invention relates to a slave-type interface circuit intended for the switching of a plurality of channels and comprising logic inputs capable of receiving data and clock signals supplied by a serial bus, a register for receiving the signals received from the bus by the logic inputs, and a memory for the data received by the register.

A circuit of this kind is known from European patent 51332 in the name of N.V. PHILIPS' GLOEILAMPENFABRIEKEN, published on 11th April 1984, in the form of a station which is addressable notably as a master or a slave, and which is employed in a two-wire, serial-type bus system.

In a certain number of applications, particularly for television, one or more interface circuits are generally used between the receiver and a television-equipment connector. The circuits generally used for this application perform switching operations in conventional fashion and cannot be controlled from a bus.

The invention aims to provide an interface circuit which can be controlled from a serial bus, particularly of the previously mentioned type, but which is designed so as to perform only the functions of a slave-type interface in a configuration in which writing into the memory takes place after recognition of an address.

To achieve this, the invention is characterized in that there is provided a decoder which controls the switching of the channels on the basis of logic signals stored in the memory, and also a plurality of addressing inputs, each of which can be set to a logic level so as to generate an indicated address, in that the register is a shift register receiving in series at an input located at an upstream end series logic information supplied by the bus in the form of cycles, each of which presents at least one sequence and is clocked by a clock signal supplied by the bus whereto the circuit is normally connected, and producing at an output located at a downstream end an end-of-sequence acceptance signal which is applied to the input of a first control flip-flop which is synchronized by said clock signal and whose output synchronizes a

second control flip-flop, referred to as a pointer, whose inverted output is retrocoupled to its input, in that the presence of a logic level "1" at the output of the first flip-flop and at the inverted output of the pointer enables initialisation of the register, for example by setting its first flip-flop to the "1" state and resetting its other flip-flops to zero, in that there is provided a logic comparator which identifies, in a given part of an address sequence, series logic information supplied by the bus if said address sequence, corresponds to said indicated address, and which produces an identification logic signal, in that there is provided a circuit for storing said identification signal, and in that there is provided a gate controlling the loading in the memory of the data from the register when the output of the first control flip-flop and of the pointer are in the logic state "1", when a said stored identification signal is present and also a said end-of-sequence acknowledge signal, thus corresponding to the end of a data sequence succeeding said address sequence.

In one embodiment the register is initialised between the address sequence and the data sequence by setting the first flip-flop of a register to the "1" state and resetting its other flip-flops to zero when the output of the first control flip-flop is in the "1" state and the output of the pointer is in the zero state.

The circuit in accordance with the invention can be deactivated by means of a series of logic gates inhibiting the transmission of the logic signals available at the output of the first decoder to the cannels to be switched in the presence of a logic signal which is referred to as the interface-circuit off signal.

Validation of this off signal can be realised with the aid of an authorisation gate receiving at one input said "off" signal and at the other input an output from a first flip-flop of the memory loaded at the time of said loading by the first flip-flop of the register.

This circuit can be initialised by means of a pulse generator which, when voltage is applied to the circuit, produces a pulse causing the initialisation of the memory and the register.

In an attractive version the bus supplies, in accordance with the procedure described in the cited European patent, start and stop information relating to a cycle of information supplied by the bus

with the aid of logic relations between the information and clock signals.

The circuit then incorporates a third and a fourth control flip-flop which, when the interface circuit is in its first state, receive the clock signal at their input and are timed one by the information signal and the other by its inverse so that the output of the third flip-flop is set to the state "1" by a first type of coincidence between the clock and information signals, corresponding to the start of a said cycle, and the fourth flip-flop is set to the "1" state by a second type of coincidence between the clock and information signals, corresponding to the end of a cycle, the third flip-flop being reset to zero by the inverse of the clock signal and the fourth flip-flop by the output from the third, the output of the fourth flip-flop being designed so as to produce, when it is in its logic "1" state, an initialisation of the register by setting its first flip-flop to the "1" state and resetting its other flip-flops to zero.

The fourth flip-flop can be advantageously set to the logic "1" state, when, after an address sequence, no identification whatsoever has been stored. To do so, the circuit is arranged so that the fourth flip-flop has its output set to the logic "1" state when the stored identification signal is in the logic "0" state and when the first flip-flop has its output in the logic "1" state; this consequently produces initialisation of the register.

The fourth flip-flop can likewise have its output set to the logic "1" state in various configurations, particularly in the presence of a pulse produced by the pulse generator or when the outputs of the first and the second flip-flop and the clock signal together are at the logic "1" level (detection of end of cycle).

The register may be advantageously initialised when the fourth flip-flop, and possibly the third flip-flop, has its output in the state "1". This initialisation occurs when the fourth flip-flop detects an inactive state of the circuit or when the third flip-flop indicates, in the course of a cycle, the undue reception of a coincidence corresponding to the start of a cycle.

For the purpose of communicating with the bus with a view to the acceptance of a data sequence following an address sequence, the circuit preferably comprises an acceptance flip-flop synchronized by the

clock signal, and receiving at its input the logic product of the acceptance signal and the stored identification signal, and producing an authorisation signal at its output to the bus. This acceptance flip-flop may also be reset to zero by said pulse. Said pulse can also reset flip-flop to zero and set the fourth control flip-flop to the state "1".

In one embodiment the circuit for storing the identification signal comprises two inverting AND-gates, the output of one of which is looped to one of the inputs of the other and vice versa, the other input of the first of the two inverting AND-gates receiving the inverse of the identification signal, be it only if the pointer has its output in the logic state "0" and if the clock signal is in the logic state "1", the other input of the second of the two inverting AND-gates receiving the logic product of the inverses of the outputs of the third and the fourth flip-flop so as to maintain the storage of the identification signal during each cycle.

The invention will be more readily understood if the following description, given by way of a non-exhaustive example, is read in conjunction with the Figures:

Figure 1, shows an overall diagram of a device in accordance with the invention;

Figure 2, shows an embodiment of the memory of Figure 1 and its functional link with controlled switches;

Figure 3, shows an embodiment of the bus logic, the register and the address-identification circuit of Figure 1; and

Figures 4a and b, show a cycle supplied by the bus and a time diagram of the principle signals of Figure 3, respectively.

As shown in Figure 1, the interface circuit comprises addressing inputs S_0, S_1, S_2, each of which can be connected by wiring either to a given potential, for example the power-supply voltage of the circuit, or to ground so as to generate an indicated address A_0, A_1 and A_2, each bit of which is coded either "0" or "1". Such an address may also be generated from a multistate logic circuit and a decoder.

An address-sequence identification circuit AIC receives signals leaving the register REG and also the signals A_0, A_1, A_2 corresponding to the indicated address. It performs a logic comparison between all these signals in order, on the one hand, to identify whether

the indicated address A_0, A_1, A_2 corresponds to the address transmitted by the bus and, on the other hand, to recognise an always identical flag, transmitted in the address sequence of a cycle, the purpose being the detection of any transmission errors in the signals. The address-sequence identification circuit AIC produces at its output an identification logic signal DVA which is received by the bus logic BUSL.

The bus logic BUSL also receives the logic information signal SDA and the clock signal SCL, notably in order to recognise the start and the end of each cycle. It further receives an end-of-sequence acceptance signal ACN which is produced by the register REG when all bits of a sequence have been received by the register REG. An information cycle transmitted via the bus is typically composed of an address sequence preceding a data sequence.

The bus logic BUSL then controls the circuit on the basis of three logic signals:

a) a reset to zero signal RST1 from the register REG which is produced at the start of each sequence and also in the case that the address is not recognised or absent;

b) an authorisation signal ACK transmitted towards the bus (input L_1) and confirming the acceptance by the bus logic BUSL of a sequence and authorising the transmission of the next sequence by the bus;

c) a signal LDA instructing the loading of the data in the register REG into the memory M. The memory M controls a series of switches COM via a switching decoder COM.

When the interface circuit is connected to the supply voltage source, the power-supply voltage V is advantageously applied to a pulse generator PG which produces an initialisation pulse PON for the bus logic BUSL, the register REG, and the memory M. In the remainder of the description all D-type flip-flops have been chosen of the type which is loaded on a negative-going edge applied to their clock input CK. It will be evident that flip-flops which are loaded on a positive-going edge could also have been used.

As Figure 2 shows, the memory M comprises eight D-type flip-flops M_0 to M_7 and the switching decoder CDEC is composed of a decoder CDEC 1 processing the information from memories M_1 and M_2 and a direct control for the other memories M_3 to M_7. The switching

block COM consists of nine controlled switches I_1 to I_9.

More specifically, each of the flip-flops M_0 to M_7 receives at its input D an output, QR_0 to QR_7, respectively, of the register REG, the latter being formed, for example, as will be seen in Figure 3, by a shift register comprising flip-flops R_0 to R_7 receiving the logic information SDA in series. Each of the flip-flops M_0 to M_7 receives at its clock input CK the inverse $\overline{LDA}$ of the signal for loading the data into the memory. When LDA changes to the state "1", authorising the loading, $\overline{LDA}$ changes to zero, producing a negative-going edge which activates the inputs CK of the flip-flops M_0 to M_7. Additionally, the flip-flops M_0 to M_7 receive at their reset to zero input R the pulse PON produced when the circuit is connected to the supply voltage.

The nine controlled switches I_1 to I_9 receive the output from nine AND-gates 101 to 109, one input of which receives the output from an inverting AND-gate 90. The other input of the AND-gates 101 to 104 receives an output from the decoder CDEC 1, and that of the AND-gates 105 to 109 receives the outputs M_3 (Q) to M_7 (Q), respectively, from the memory flip-flops M_3 to M_7.

When the output of the inverting AND-gate 90 is in the state "1" (normal case, OFF = 0), the gates 101 to 109 enable the control of the switches I_1 to I_9 by the data stored in the memory in M_1 to M_7, the logic signals QM_1 and QM_2 at the output of the memory flip-flops M_1 and M_2, applied to the inputs of the decoder CDEC 1, controlling the switches I_1 to I_4, in accordance with four possible configurations, for example, the closing of one of them at a time.

As will be explained in the course of the description, the flip-flop M_0 is reserved for the storage of a state for enabling an "OFF" command. The inverted output $M_0(P)$ from the memory M_0 is applied to an input of the inverting AND-gate 90 whose other input receives said command OFF. The inverted output PM_0 from the memory flip-flop M_0 enables, when it is at the level "1", the transmission of the command OFF via the gate 90. The output of the gates 101 to 109 is then at "0" and de-activates the switches I_1 to I_9.

As Figure 3 shows, the register REG is a shift register consisting of nine D-type flip-flops R_0 to R_8. The output Q of

registers R_0 to R_7 is connected to the input D of the next register, which is respectively R_1 to R_8. Each of the flip-flops R_0 to R_8 is synchronized at its input CK by the inverse $\overline{SCL}$ of the clock signal SCL so as to operate on the positive-going edges of the clock signal SCL. The flip-flop R_0 is set to the state "1" (input 5) and the flip-flops R_1 to R_8 are reset to zero by an initialisation signal RST1 available at the output of an inverting AND-gate 63. Before each cycle the signal RST1 effects an initialisation. Therefore, $R_0(Q) = 1$. This corresponds time-wise to the start bit STA of the type of cycle shown in Figure 4a. The shift register, synchronized by $\overline{SCL}$, receives all bits of the address sequence A. This sequence is correctly positioned in the shift register when the logic "1" inserted in R_0 at the time of initialisation enters R_8. Thus, the bit A_6 is stored in R_7 and so on to A_0 which is stored in R_1. The bit W is always equal to zero. The bits A_2, A_1 and A_0 in the sequence will be compared with the corresponding bits of the same name in the indicated address by means of three exclusive-NOR gates 10, 11 and 12. The gate 10 receives A_0 and $Q(R_1)$ at its inputs, the gate 11 receiving A_1 and $Q(R_2)$, and the gate 12 receiving A_2 and $Q(R_3)$. If the address A_0, A_1, A_2 transmitted in the address sequence A is identical to the indicated address, each of the gates 10, 11 and 12 produces a logic "1" at its output. For the embodiment of Figure 3, it has also been assumed that the bits A_6, A_5, A_4 and A_3 form an identification flag which always has a fixed value according to the sequence 1001. Consequently, the complete identification of an address sequence is performed by a multiple AND-gate producing at its output an identification signal DVA and receiving at its inputs the outputs $Q(R_7)$ and $Q(R_4)$ and the inverted outputs $P(R_6)$ and $P(R_5)$ and also the outputs from the gates 10, 11 and 12. The gates 10, 11, 12 and 15 form the address-sequence identification circuit AIC. On the other hand, the output $Q(R_8)$ produces an end-of-sequence acceptance logic signal ACN. The bit W which follows A_0 in the address sequence is by convention a zero; it indicates a write mode. It can be identified by also applying $P(R_0)$ to the input of the gate 15.

The lower part of Figure 4, enclosed by a dot-dash line, forms the bus logic BUSL.

It comprises a first D-type control flip-flop DC1 receiving at its input D the signal ACN available at the output Q of R_8, and at its synchronizing input CK the clock signal SCL, and a second control or pointer flip-flop PNT, also of the D-type, whose inverting output P is retrocoupled to the input D, its synchronizing input CK being connected to the output Q of the first flip-flop DC1. The pointer PNT serves to indicate whether an address sequence or a data sequence of a cycle is in progress.

A third control flip-flop STR and a fourth control flip-flop, STP, again of the D-type, serve to control the start and the end of a cycle. The bus indicates the start of a cycle (see Figure 5b) by a transition from the level "1" to the level "0" of the signal SDA when the clock signal SCL is at the level "1", and the end of a cycle by a transition from the level "0" to the level "1" of the signal SDA when the clock signal SCL is at the level "1". However, the information-carrying transitions of the signal SDA occur when the clock signal SDA is at the logic level "0". The fourth flip-flop STP serves to indicate whether the circuit is in an active or inactive state relative to the bus. In the latter case its output initialises the register R.

The third flip-flop STR receives the clock signal SCL at its input D and is synchronized at its synchronizing input CK by the signal SDA so as to detect the start of a cycle, whereas the fourth flip-flop STP receives the clock signal SCL at its input D and, at its synchronizing input CK, the inverted signal $\overline{SDA}$ formed from SDA by an inverter 28, so as to detect the end of a cycle. The output Q of the third flip-flop STR is applied to the reset to zero input R of the pointer PNT and of the fourth flip-flop STP. The third flip-flop STR is reset to zero by the inverse $\overline{SCL}$ of the clock signal SCL obtained by the inverter 60 whose output is connected to the input R of STR. The authorisation signal DVA produced at the output of the gate 15 is stored by a flip-flop with two interconnected inverting AND-gates 66 and 67, i.e. so that the output from the gates 66 and 67 is connected to a respective input of the gates 67 and 66. This storage process is enabled by an inverting AND-gate 65 and occurs when DVA = 1, SCL = 1 and PNT Q (output of the pointer) = 0. This last condition indicates that the address part of a cycle is in progress and avoids any accidental identification in a data sequence. The inverting AND-gate 65 thus

receives at its inputs the signals DVA and SCL and the inverted output P from the pointer PNT, and its output is connected to the other input of the inverting AND-gate 66. On the other hand, the other input of the inverting AND-gate 67 receives a signal STN available at the output of an AND-gate 70 whose inputs are connected to the inverting outputs P of the control flip-flops STR and STP, respectively. As long as STN = 1, the signal DVA being volatile, remains stored in the form of the signal ADC at the output of the gate 66. The return of STN to the state "0" means the erasure of this stored signal. The flip-flops R_0 to R_8 are initialized by the signal RST1 available at the output of an inverting AND-gate 63 which receives at one input the inverse P of the output of the fourth flip-flop STP (initialisation when STPQ = 1) or, as shown, preferably the output signal STN from the AND-gate 70. In the latter case, the initialisation occurs when STPQ or STRQ is equal to "1", which entails the initialisation of the register REG in the event of the occurrence of an undue coincidence corresponding to the start of a cycle while such a cycle is actually in progress. The inverting AND-gate 63 receives at its other input a signal RST2 available at the output of an inverting AND-gate 44. The latter receives at its three inputs the clock signal SCL, the output of the first control flip-flop DC1, and the inverted output P from the pointer PNT, respectively.

The flip-flops R_0 and R_8 are initalised when the flip-flop STP stores an inactive state of the circuit (STPQ = 1), or between an address sequence and a data sequence (RST2), and also at the start of a cycle.

A D-type flip-flop R_9 generates at its output P an inverted authorisation logic signal $\overline{ACK}$, which means that the acceptance corresponds to a logic "0". The flip-flop R_9 is synchronized at its loading-authorisation input CK by the clock signal SCL and receives at its input D the output from an AND-gate 16, one input of which receives the end-of-sequence acceptance signal ACN, while its other input receives the stored identification signal ADC.

The loading of the storage flip-flops M_0 and M_7 is realised with an inverted loading signal $\overline{LDA}$ applied to their loading-authorisation inputs CK. Said loading is effected by the change of ~~$\overline{LDA}$~~ from the state "1" to the state "0". The signal $\overline{LDA}$ is obtained at the output of an inverting AND-gate 33

whose inputs receive the end-of-sequence acceptance signal ACN, the stored identification signal ADC, and the outputs Q from the first flip-flop DC1 and from the pointer PNT. The loading is thus authorised when an end of a data sequence has been detected while, previously an address sequence corresponding to that indicated by the circuit has been identified.

The fourth flip-flop STP is set to the state "1" by the output from an inverting AND-gate 71 which comprises four inputs. Its first input receives the inverted output P from STP (self-maintenance of the state "1" of STP) and its second input receives the inverse PON of the pulse PON produced when voltage is first applied (setting STP to the state "1" when voltage is first applied).

Its third input receives the output from an inverting AND-gate 69 whose inputs are SCL, the output Q from DC1, and the output Q from the pointer PNT (setting STP to the state "1" at the end of the cycle, even in the event of failure of the bus). Its fourth input receives the output from an inverting AND-gate 68 whose inputs are the output Q from DC 1 and the inverse $\overline{ADC}$ of ADC which is available at the output of the inverting AND-gate 67 (setting STP to the state "1" if, at the end of an address sequence, no identification signal whatsoever has been produced and stored).

It will be noted, finally, that the pulse PON produced when the circuit is connected to voltage also resets (input R) the first control flip-flop DC1 and the flip-flop R_9 to zero.

The operation of the circuit in the event of an information cycle provided by the bus and corresponding to the indicated address A_0, A_1, A_2 at the inputs S_0, S_1 and S_2 of the circuit will now be described with reference to Figures 4a and 4b.

The starting condition STA correspoinds to a negative-going edge of SDA with SCL = 1. This is detected by STR whose output STRQ changes to the state "1" upon said negative-going edge of SDA, this change to the state "1" also having the effect to resetting the output STPQ of STP and of PNT to zero and of making ADC = 0, because STN = 0 and DVA = 0. At that instant the output P of STP changes to the state "1" (STPQ = 0) and RST1 to the state "0". Thanks to the previous initialisation, the flip-flop R_0 is at that instant in the state "1", and the flip-flops R_1 to R_8 are in the state "0". The output Q from

STR is reset to zero by the negative-going edge of the starting clock pulse SCL. The bus transmits the address sequence A until R_8 receives, via shifting the logic "1" stored in R_0 upon initialisation, resulting in ACN = 1 on the positive-going edge of the 8th clock pulse. The bit A_6 is then located in R_7 and so on until A_0 is located in R_1, and W = 0 (by convention) in R_0. The address transmitted by the bus corresponding to that indicated by the circuit, the AND-gate 15 transmits a DVA = 1, which is authorised by the gate 65 because the output P from the pointer PNT is in the state "1" as from the 8th clock pulse SCL. ADC changes to the state "1". In response to the next clock pulse DVA again changes to "0", but ADC remains at the level "1" because the outputs from STR and STP are both at the level "1", hence STN = 1.

The simultaneous presence of ACN and ADC, detected by the gate 16, produces at the output P of R_9 the signal $\overline{ACK}$ at the negative-going edge of the 8th clock pulse, the latter being erased by the negative-going edge of the 9th clock pulse because the output of the gate 16 is zero at that instant: ACK is, therefore, a signal identical to ACN but delayed by half a clock pulse. It is, therefore, present when the clock is at its high level for the ninth pulse, hence in the space provided for that purpose between the address sequence A and the data sequence D. The way in which the bus system deals with this signal ACK is described in the cited European Patent.

The signal ACN also sets the flip-flop DC1 (DC1Q) to the state "1" at the negative-going edge of the eighth clock pulse. DC1Q changes back to zero at the negative-going edge of the 9th clock pulse because ACN has changed back to zero at the positive-going edge of this same clock pulse. This negative-going edge of DC1Q sets the output of the pointer PNT to the state "1" (PNT Q =1). The pointer PNT thus notes the fact that the data sequence D of the cycle is now about to be received.

For the duration of the ninth clock pulse SCL, SCL = 1, DC1Q = 1 and PNTQ = 0, hence RST1 = 1; this causes the initalisation of the register R, R_0 being in the state "1" and R_1 to R_8 in the state "0".

The arrival of the data sequence thus cocurs with ADC = 1 and PNT = 1.

As for the address sequence A, the logic "1" stored in

R_0 at the time of initialisation is transferred by shifting to the register R_8 so as to produce an ACN = 1 at the positive-going edge of the 8th clock pulse of the sequence D, ACN returning to 0 at the positive-going edge of the next clock pulse. The bit D_7 is then stored in R_7 and so on until D_0 which is stored in R_0. Thus, DC1Q = 1 at the negative-going edge of the eighth clock pulse of the sequence D, DC1Q returning to 0 at the negative-going edge of the next clock pulse.

Between the negative-going edge of the eighth clock pulse of the sequence D and the next positive-going edge, simultaneously DC1Q = PNTQ = ACN = ADC = 1, and hence LDA = 1 for the duration of half a clock pulse. The contents of R_0 to R_7 are transferred in parallel into the memory flip-flops M_0 to M_7. In particular, M_0 receives from R_0 the bit D_0, being a "0" in principle, making it possible to enable the command OFF at the input of the gate 90 (Figure 3).

The open or closed position of switches I_1 to I_9 is then changed in accordance with the new contents of the memories M_0 to M_7 if the control OFF is inactive or inhibited by the bit D_0.

As for the address sequence A, R_9 produces a signal ACK = 1 between the negative-going edge of the eighth clock pulse and that of the ninth clock pulse in the sequence D. The change to zero of DC1Q at the negative-going edge of the ninth clock pulse in the sequence D causes the resetting to zero of the pointer (PNTQ = 0). At the end of the cycle the bus transmits an "off" signal formed by a positive-going edge SDA on a clock signal SCL at the level "1", resulting in STPQ = 1, hence STN = 0, therefore ADC = 0, and RST = 1 (initialisation of the register R). An improved embodiment of the interface circuit in accordance with the invention caters for the case in which the bus might fail with regard to the production of such an "off" signal.

To that end, advantage is taken of the fact that, in the terminal phase of a cycle, a transitory and characteristic situation occurs in which DC1Q = PNTQ = 1. The gate 69 then sets the flip-flop STP to the state "1" (STPQ = 1) at the positive-going edge of the ninth clock pulse in the sequence D.

The "off" signal delivered by the bus consists of a positive-going edge on the signal SDA while SCL = 1 on the tenth clock pulse in the sequence D. It is detected by the flip-flop STP which changes to the state "1" (STPQ = 1) in the circuit versions not

incorporating a gate 69. This is represented by dashes in Figure 4b, and also applies to the signals ADC and RST1.

CLAIMS:

1. A slave-type interface circuit intended to operate with a serial bus for the purpose of switching a plurality of channels and comprising logic inputs capable of receiving information and clock signals supplied by said bus, a register (REG) for receiving the signals (SDA, SCL) received from the bus by the logic inputs (L_1, L_2), and a memory (M) for the data received by the register (REG), characterized in that it comprises a decoder (CDEC) which controls the switching of the channels on the basis of logic signals stored in the memory (M), and also a plurality of addressing inputs (S_0, S_1, S_2) each of which can be set to a logic level so as to generate an indicated address (A_0, A_1, A_2) in that the register is a shift register (R_0-R_7) receiving in series at an input located at an upstream end series logic information (SDA) supplied by the bus in the form of cycles, each of which presents at least one sequence and is clocked by a clock signal (SCL), and producing at an output (QR_8) located at a downstream end an end-of-sequence acceptance signal (ACN) which is applied to the input (D) of a first control flip-flop (DC_1) which is synchronized (CK) by said clock signal (SCL) and whose output (Q) synchronizes (CK) a second control flip-flop (PNT), referrred to as a pointer, whose inverted output (P) is retrocoupled to its input (D) in that the presence of a logic level "1" at the output (Q) of the first flip-flop (DC1) and at the output (P) of the pointer (PNT) enables initialisation of the register (REG), which corresponds to a return to the same initial state, that it comprises a logic comparator (10, 11, 12) identifying, in a given part of an address sequence, series logic information supplied by the bus if at least said address sequence corresponds to said indicated address, and producing an identification logic signal (DVA), in that it comprises a circuit (66, 67) for storing said identification signal (DVA), and in that it comprises an AND-gate (33) enabling the loading into the memory (M) of the data of the register (R) when the output (Q) of the first control flip-flop (DC_1) and the pointer (PNT) are in the logic state "1", when a said stored identification signal (ADC) is

present as well as a so-called end-of sequence acceptance signal (ACN) which, therefore, corresponds to the end of a data sequence following said address sequence.

2. An interface circuit as claimed in Claim 1, characterized in that the configuration is such as to initialise the register (REG) by setting a first flip-flop (R_n) to the state "1" and resetting its other flip-flops (R_1 ... R_8) to zero when the output of the first control flip-flop (DC_1) is in the state "1" and the output (Q) of the pointer (PNT) is in the state zero.

3. An interface circuit as claimed in either of the Claims 1 or 2, characterized in that it comprises a series of logic gates (101, 109) inhibiting the transmission of the logic signals available at the output of the first decoder (CDEC) towards the channels to be switched in the presence of a logic "off" signal (OFF) for the interface circuit.

4. An interface circuit as claimed in Claim 3, characterized in that it comprises an authorisation gate (90) receiving at one input the "off" signal (OFF) and at the other input an output (P) from a first flip-flop (M_0) of the memory (M) loaded during said loading by the first flip-flop (R_0) of the register (R) so as to enable or not, the "off" signal (OFF).

5. An interface circuit as claimed in any one of the preceding Claims, characterized in that it comprises a pulse generator (PG) which, when voltage is applied to the circuit, generates a pulse (PON) causing the initialisation of the memory (M) and of said register (REG).

6. An interface circuit as claimed in any one of the preceding Claims, characterized in that it comprises a third (STR) and a fourth (STP) control flip-flop which, when the interface circuit is in its first state, receive at their input (D) the clock signal (SCL) and are synchronized (CK) one by the information signal (SDA) and the other by the inverse ($\overline{SDA}$) thereof, so that the output (Q) of the third flip-flop (STR) is set to the state "1" by a first type of coincidence between the clock (SCL) and information (SDA) signals corresponding to the start of a said cycle, and the fourth flip-flop (STP) is set to the state "1" by a second type of coincidence between the clock (SCL) and information (SDA) signals corresponding to the end of a cycle, the third flip-flop (STR) being reset to zero by the inverse

($\overline{SCL}$) of the clock signal (SCL) and the fourth flip-flop (STP) by the output (Q) from the third flip-flop (STR), the output (Q) from the fourth flip-flop (STP) being arranged so as to set, when in the logic "1", the first flip-flop (R_0) of the register (R) to the state "1" and to reset its other flip-flops (R_1 ... R_8) to zero.

7. An interface circuit as claimed in Claim 6, characterized in that the fourth flip-flop (STP) has its output set to the logic state "1" when the stored identification signal (ADC) is in the logic state "0" and when the first flip-flop (DC_1) has its output in the logic state "1".

8. An interface circuit as claimed in either of the Claims 6 or 7, characterized in that the register (REG) is initialized when the fourth flip-flop (STP) has its output in the state "1".

9. An interface circuit as claimed in Claim 8, characterized in that the configuration is such as to produce an initialisation of the register (REG) when the third flip-flop (STR) has its output in the state "1".

10. An interface circuit as claimed in Claim 5, in combination with any one of the Claims 6 to 9, characterized in that the fourth flip-flop (STP) also has its output (Q) set to the logic state "1" by said pulse (PON), its output being, additionally, self-maintained when it is in the state "1".

11. An interface circuit as claimed in any one of the Claims 5 to 10, characterized in that the fourth flip-flop (STP) also has its output set to the logic state "1" when the output from the first (DC_1) and the second (PNT) flip-flop and the clock signal (SCL) are all at the logic level "1".

12. An interface circuit as claimed in any one of the preceding Claims, characterized in that it comprises an acceptance flip-flop (R_9) synchronized by the clock signal (SCL) and receiving at its input the logic product of the acceptance signal (ACN) and the stored identification signal (ADC), and producing at its output directed towards the bus an authorisation signal (ACK).

13. An interface circuit as claimed in the Claims 4 and 11 taken together, characterized in that the configuration is such that said pulse also produces the resetting to zero of the acceptance flip-flop (R_9).

14. An interface circuit as claimed in the Claims 4 and 5 taken together, characterized in that said pulse also produces the resetting to zero of the first control flip-flop (DC_1) and the setting to the state "1" of the fourth control flip-flop (STP).

15. An interface circuit as claimed in any one of the preceding Claims, characterized in that the circuit for storing the identification signal (DVA) comprises two inverting AND-gates (66, 67), the output of one of which is retrocoupled to one of the inputs of the other and vice versa, the other input of the first of the two inverting AND-gates (66) receiving the inverse ($\overline{DVA}$) of the identification signal (DVA), be it only if the pointer (PNT) has its output in the logic state "0" and if the clock signal is in the logic state "1", the other input of the second one of the two inverting AND-gates (67) receiving the logic product of the inverses (P) of the outputs (Q) of the third (STR) and the fourth (STP) flip-flop, so as to permit maintenance, during each cycle, of the storage (ADC) of the identification signal (DVA).