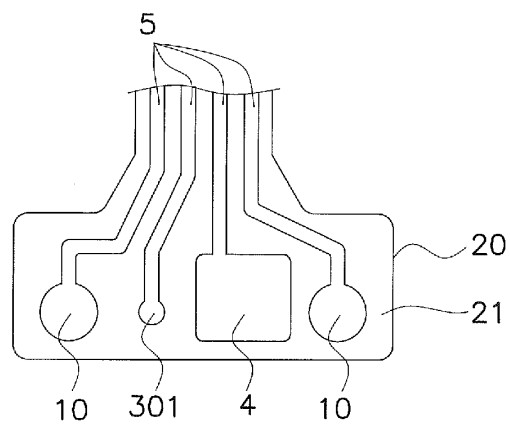
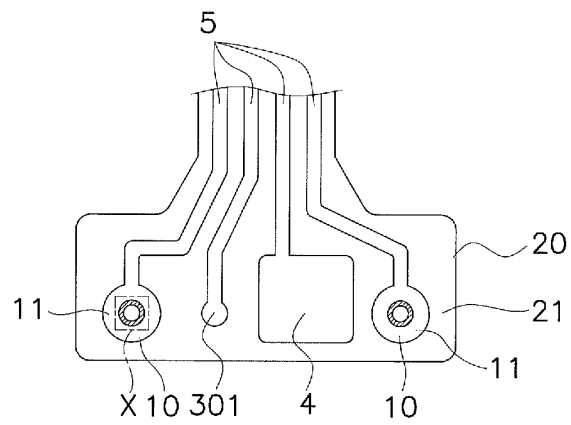


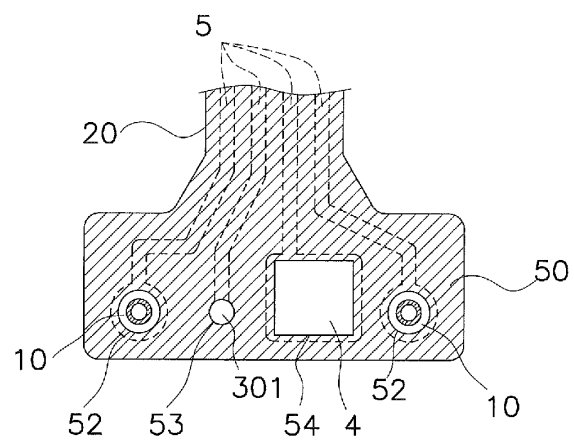
[図1]



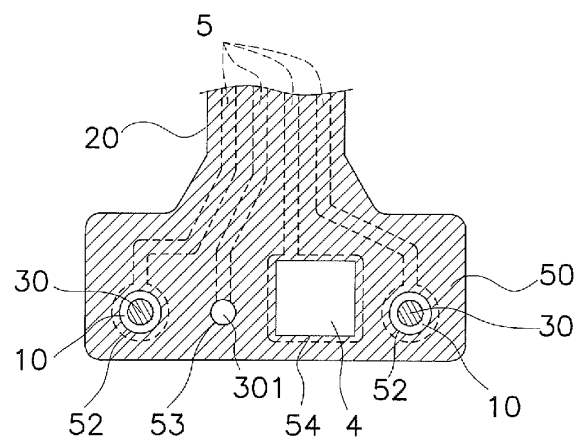
[図2]



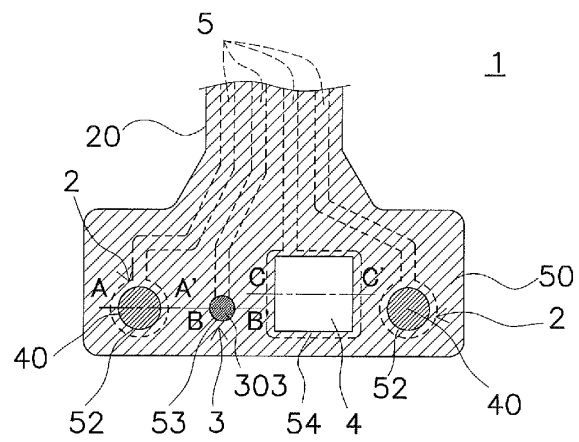
[図3]



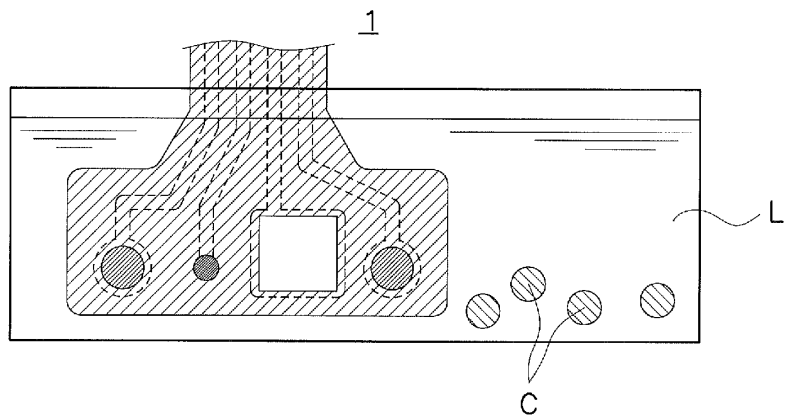
[図4]



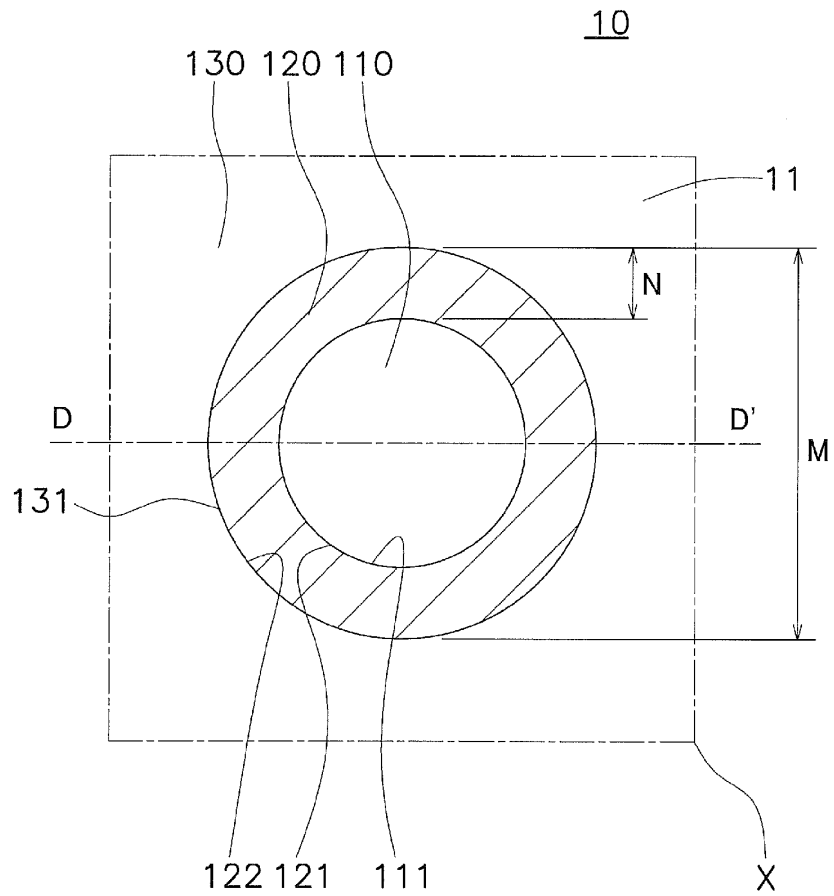
[図5]



[図6]

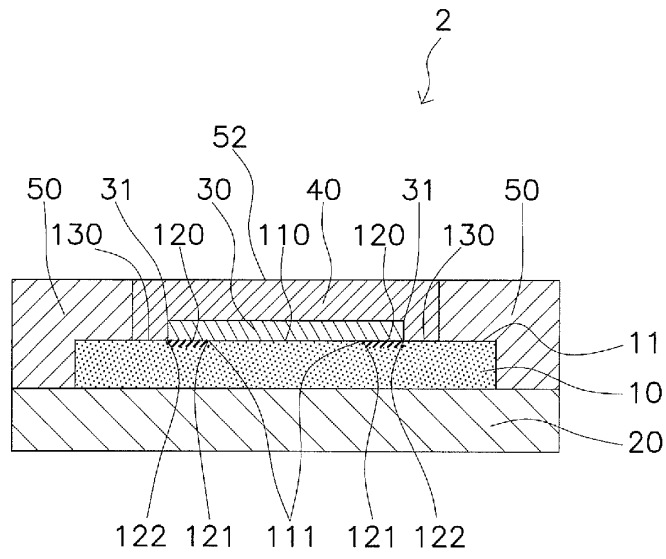


[図7]

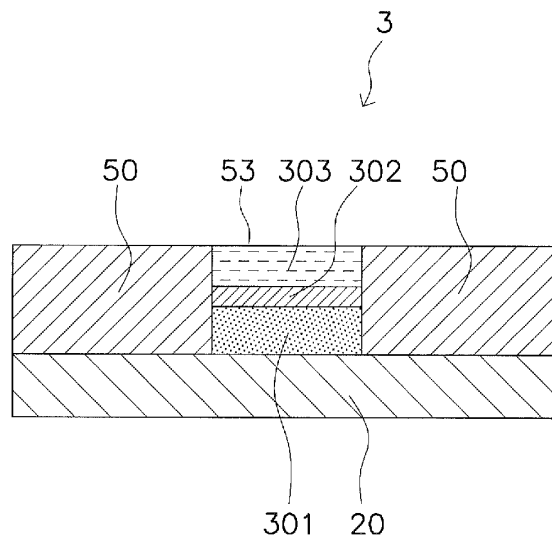




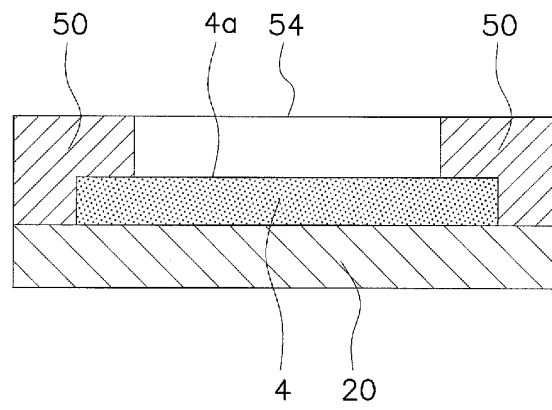
[図11]



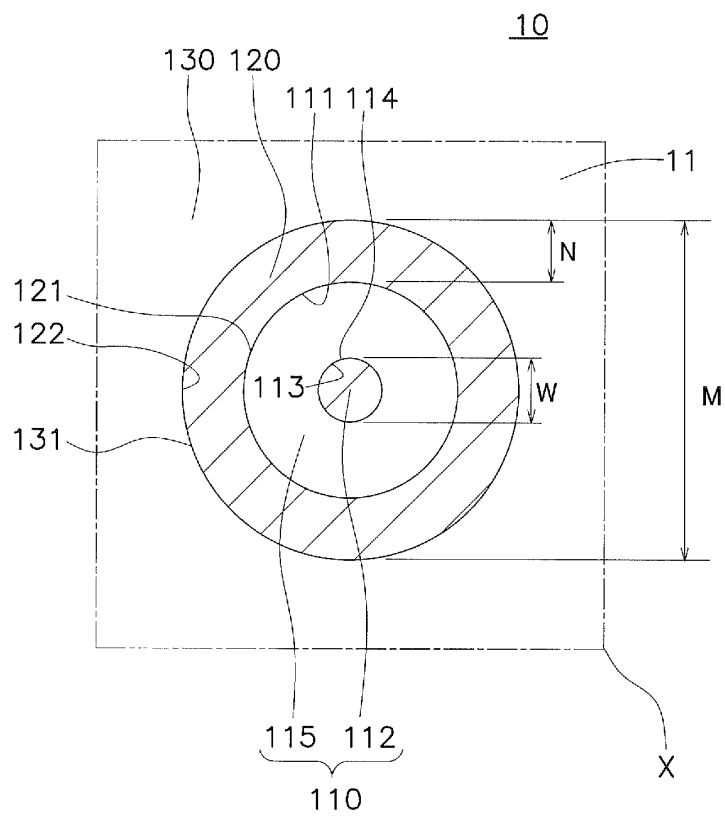
[図12]



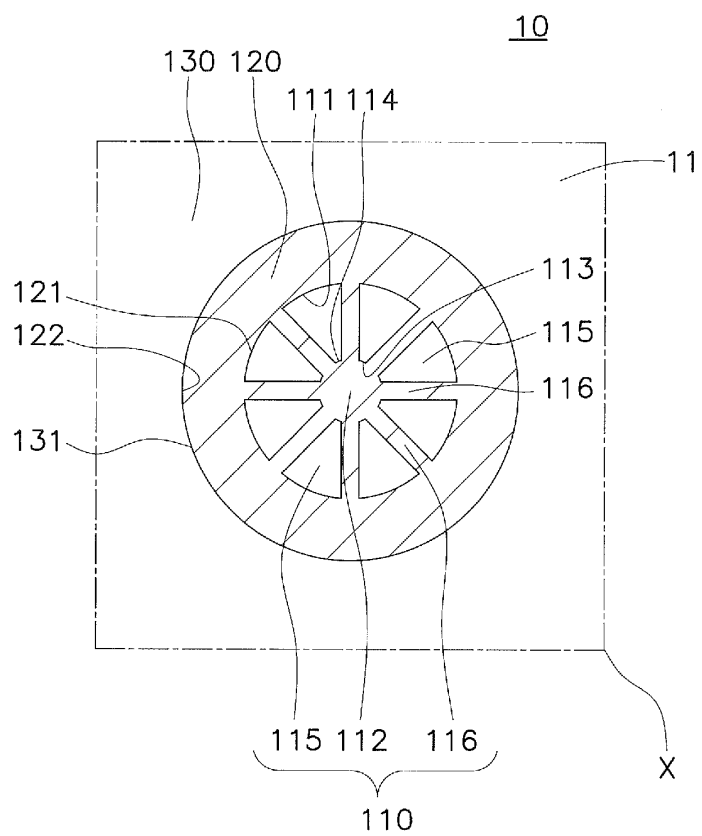
[図13]



[図14]

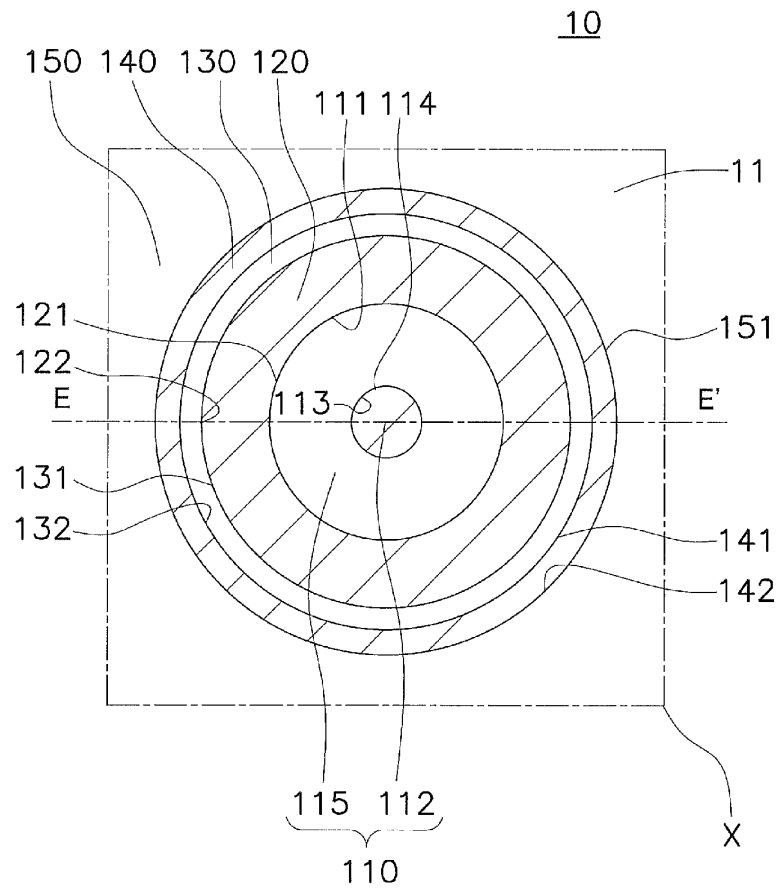


[図15]

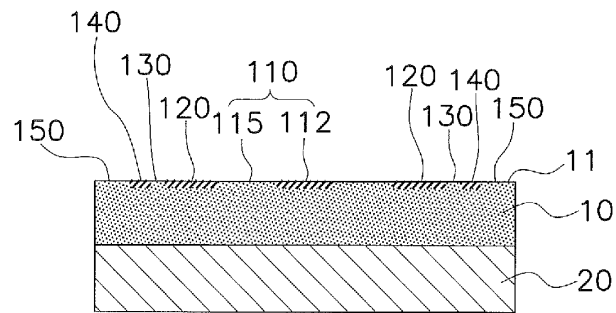




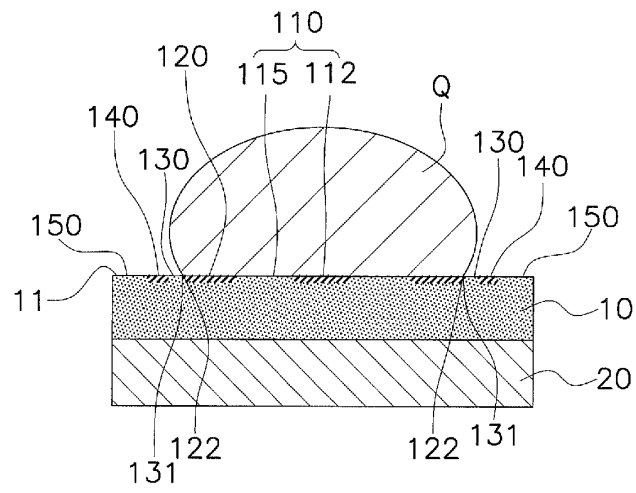
[図17]



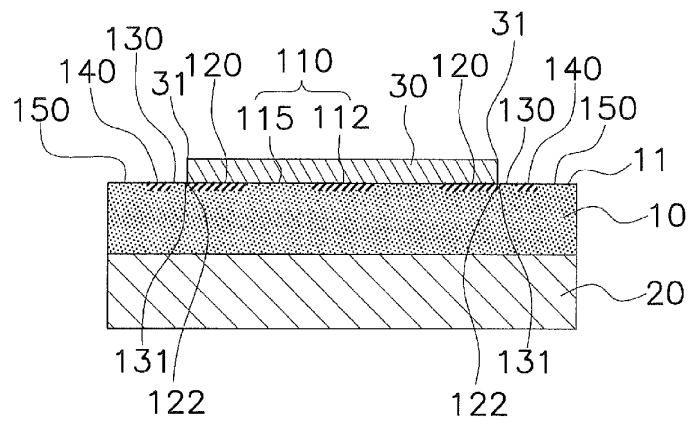
[図18]



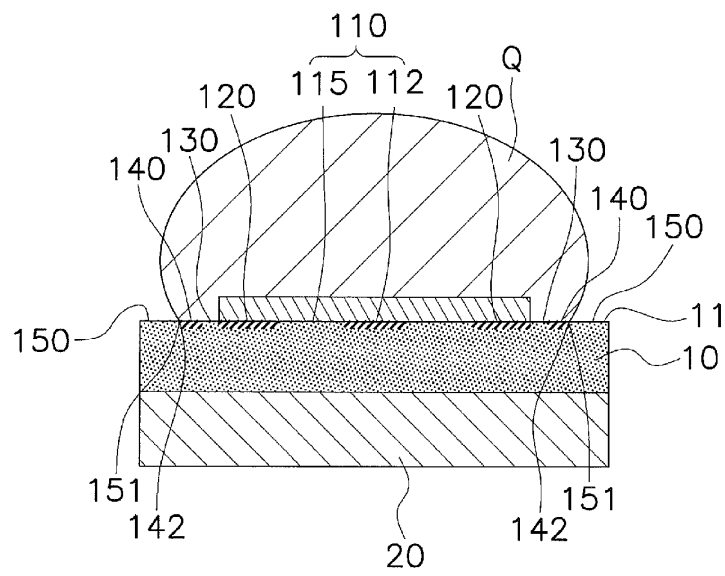
[図19]



[図20]

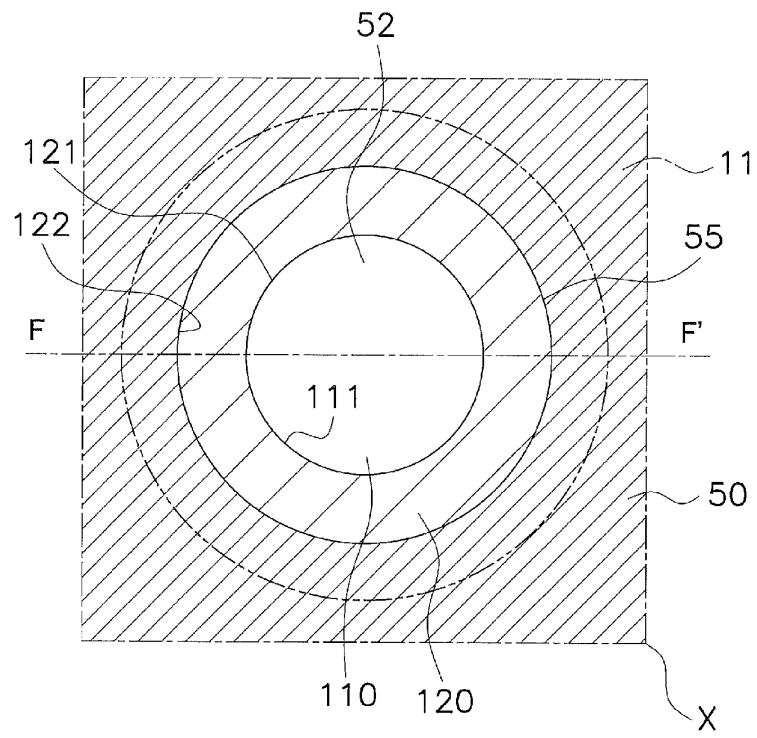


[図21]

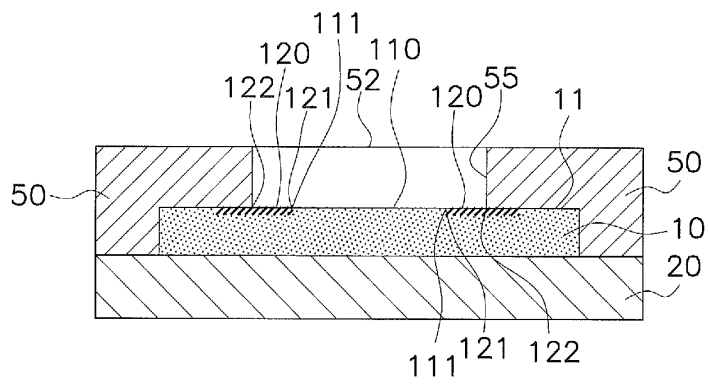




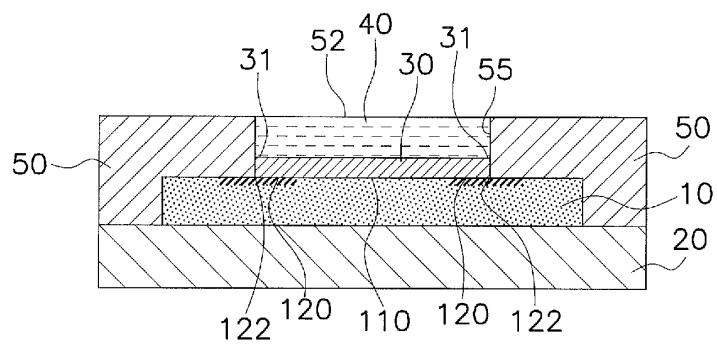
[図23]

10

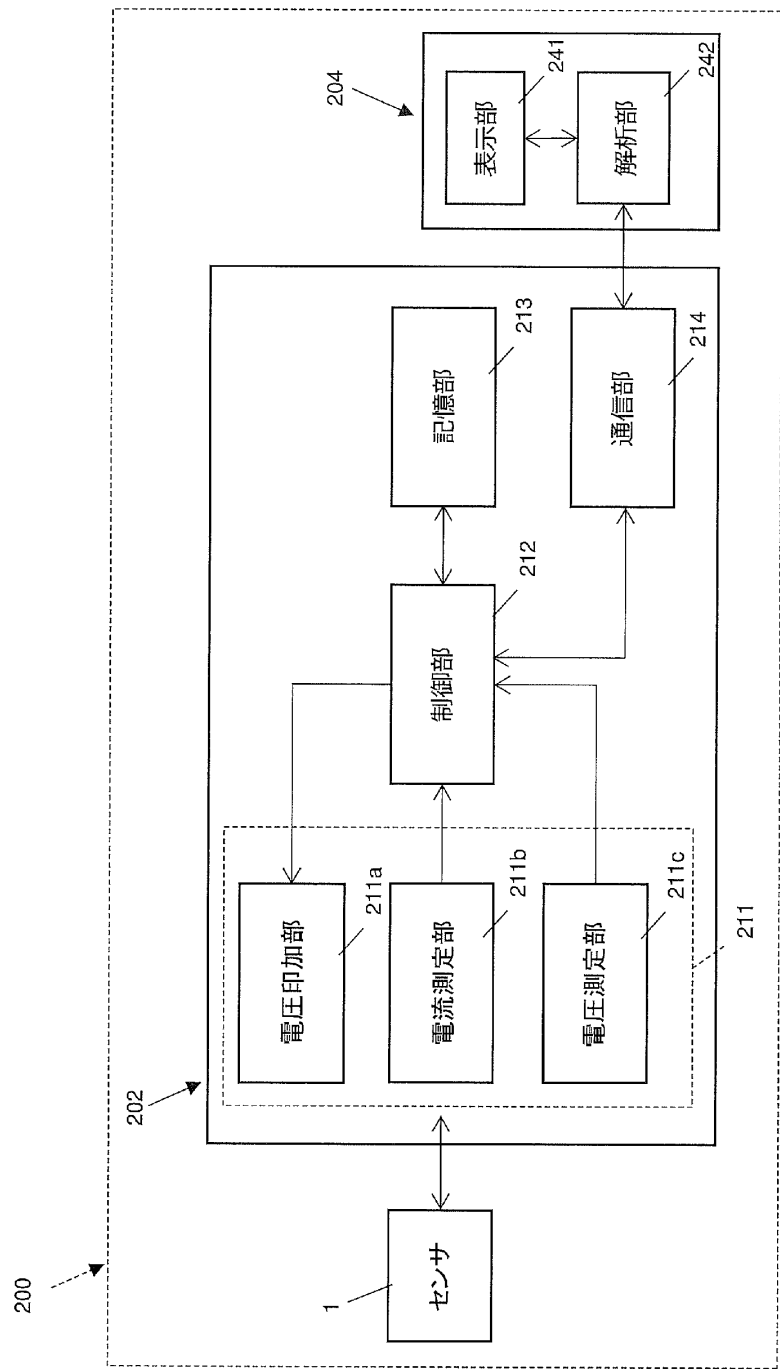
[図24]



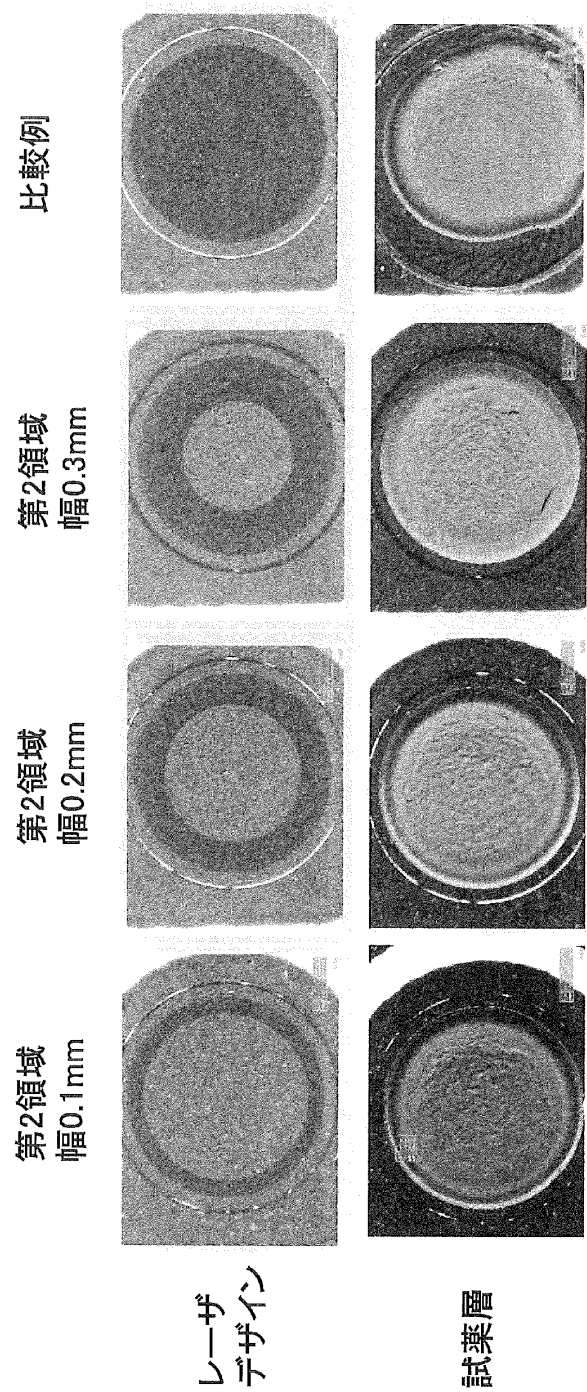
[図25]



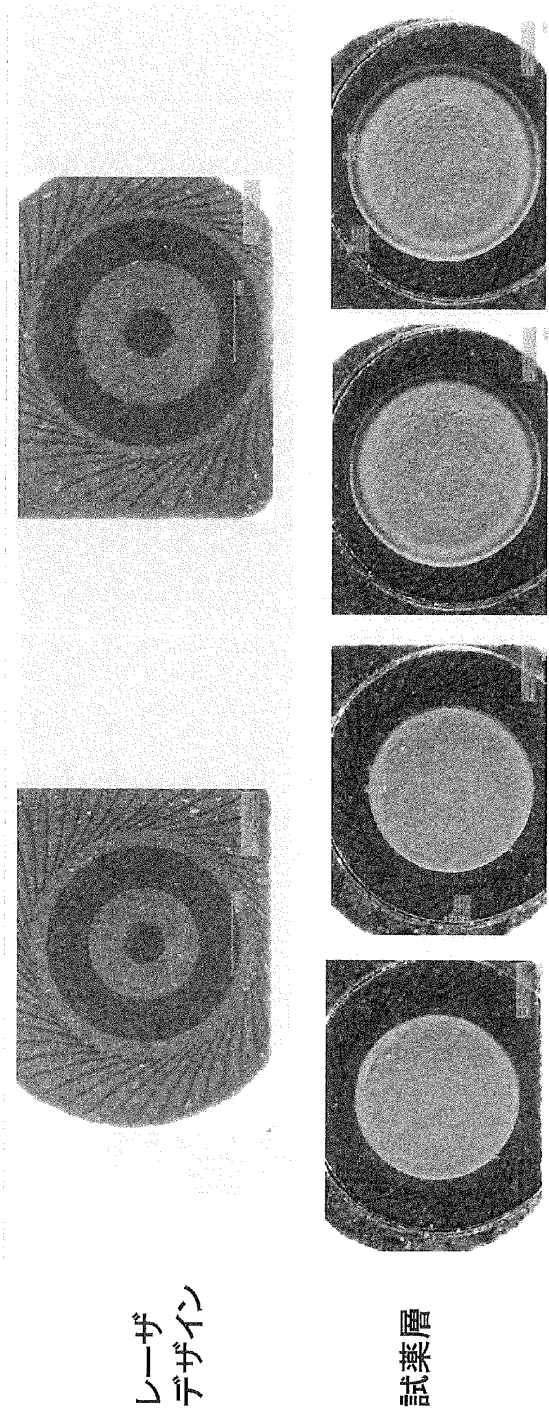
[図26]



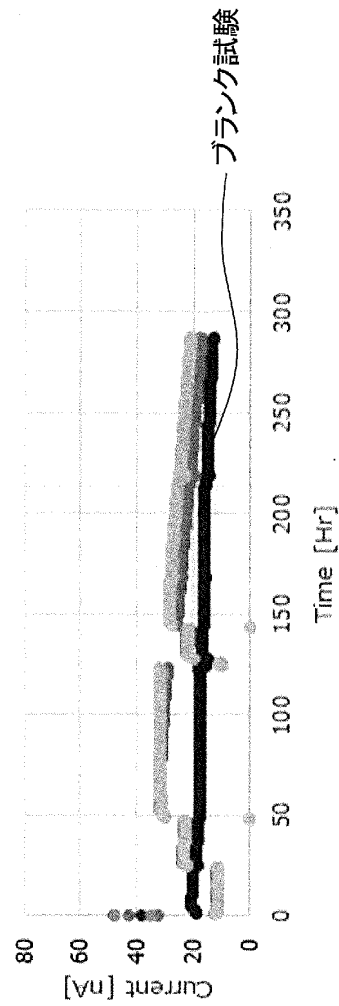
[図27]



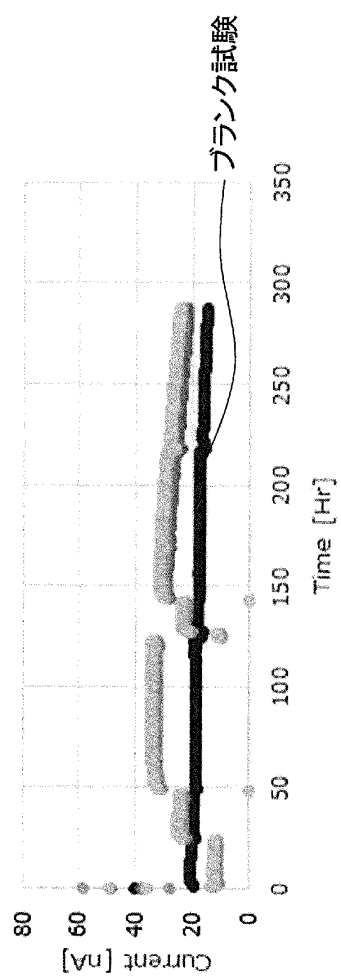
[図28]



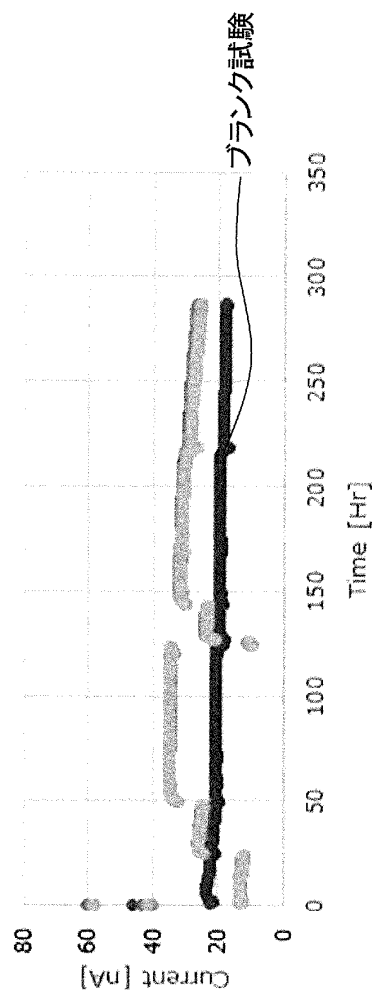
[図29A]



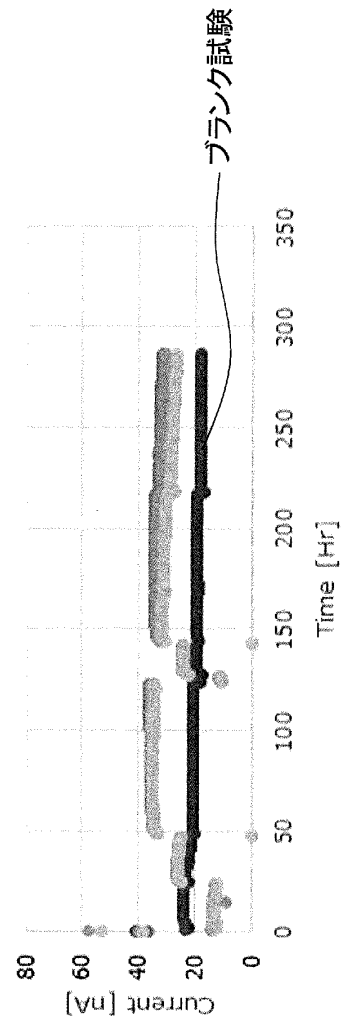
[図29B]



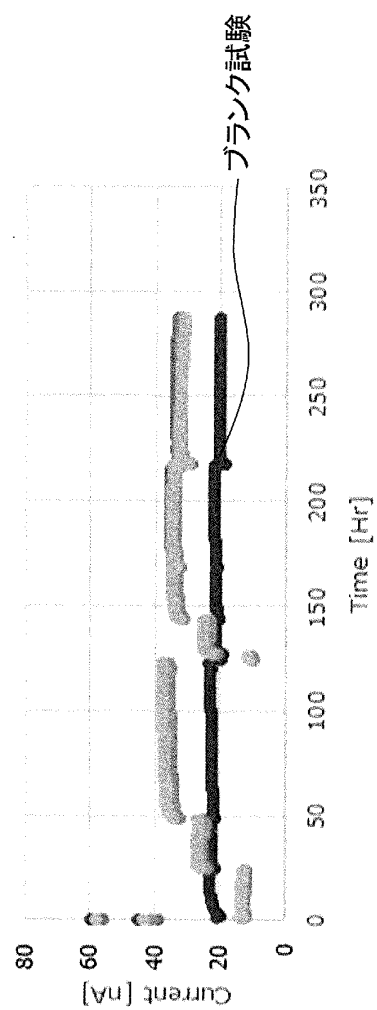
[図29C]



[図29D]

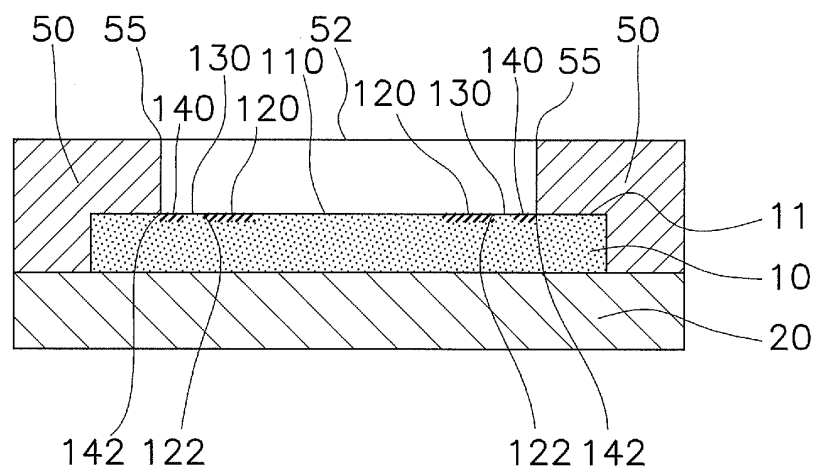


[図29E]





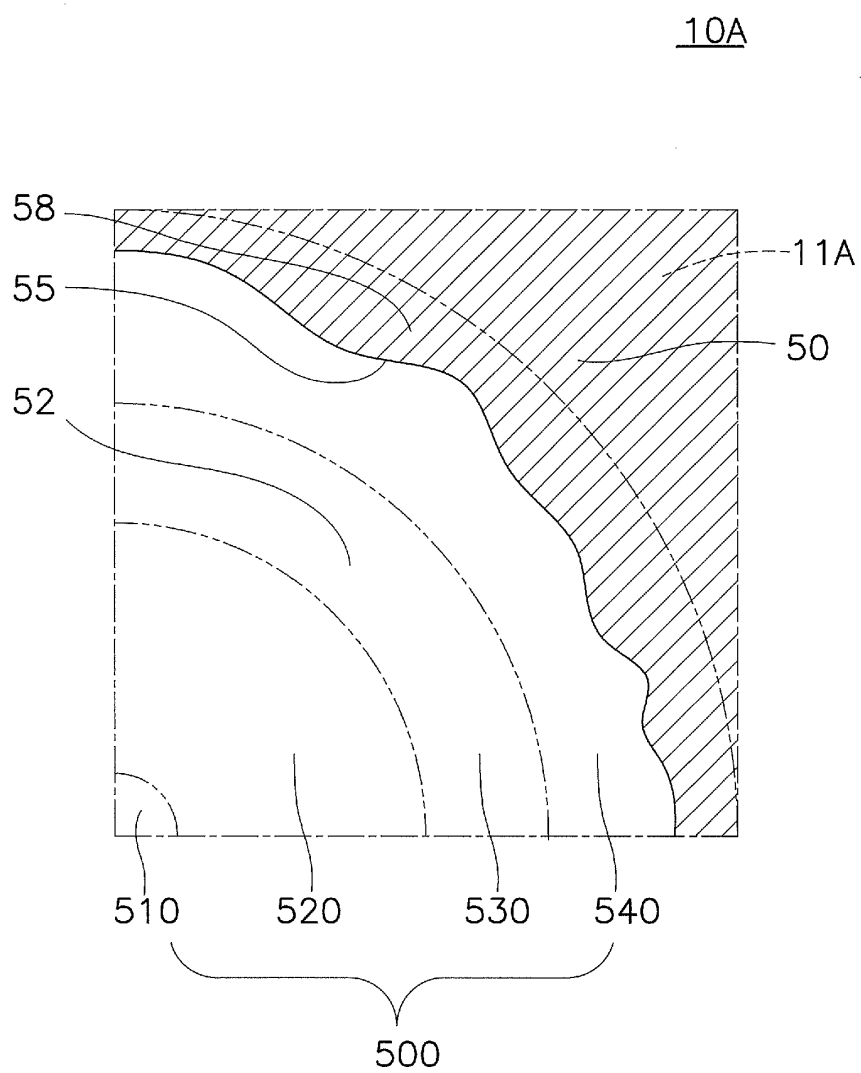
[図31]



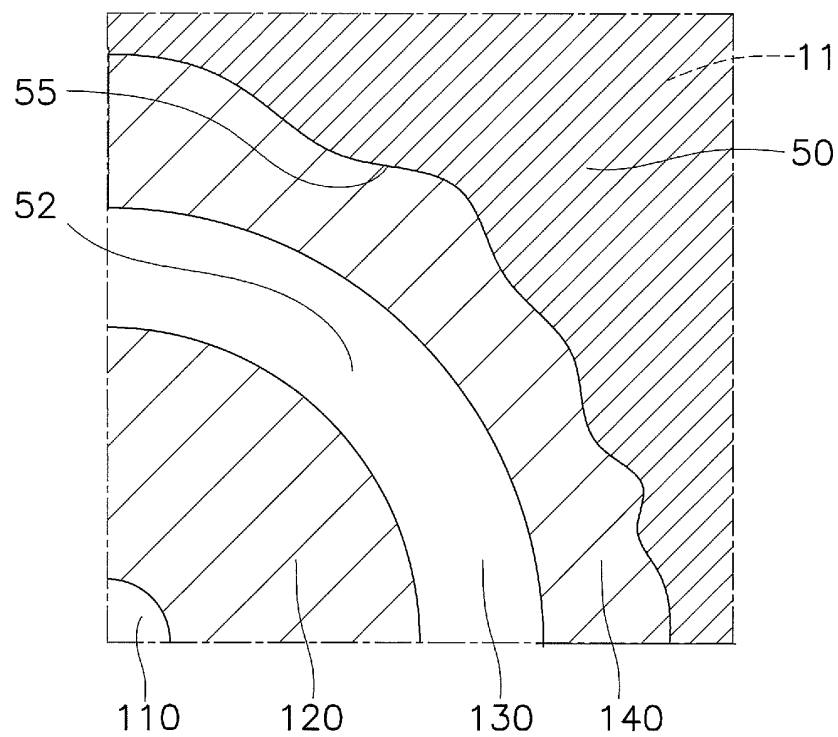
A cross-sectional view of a semiconductor device 2. The device consists of a substrate 20 with a top layer 10 and a bottom layer 11. A central region 120 is defined by a top layer 122 and a bottom layer 122. This central region is surrounded by a layer 140, which is further defined by a top layer 142 and a bottom layer 142. The device is labeled with various reference numerals: 2, 10, 11, 120, 122, 140, 142, 30, 31, 40, 50, and 52.

A cross-sectional view of a semiconductor device 500. The device includes a substrate 20, a first insulating layer 10A, and a second insulating layer 11A. A central region 500 is defined by a bracket and contains a patterned layer 510, a second insulating layer 520, a conductive layer 530, and a third insulating layer 540. The device is surrounded by a material 50, and a layer 55 is located between the substrate 20 and the central region 500.

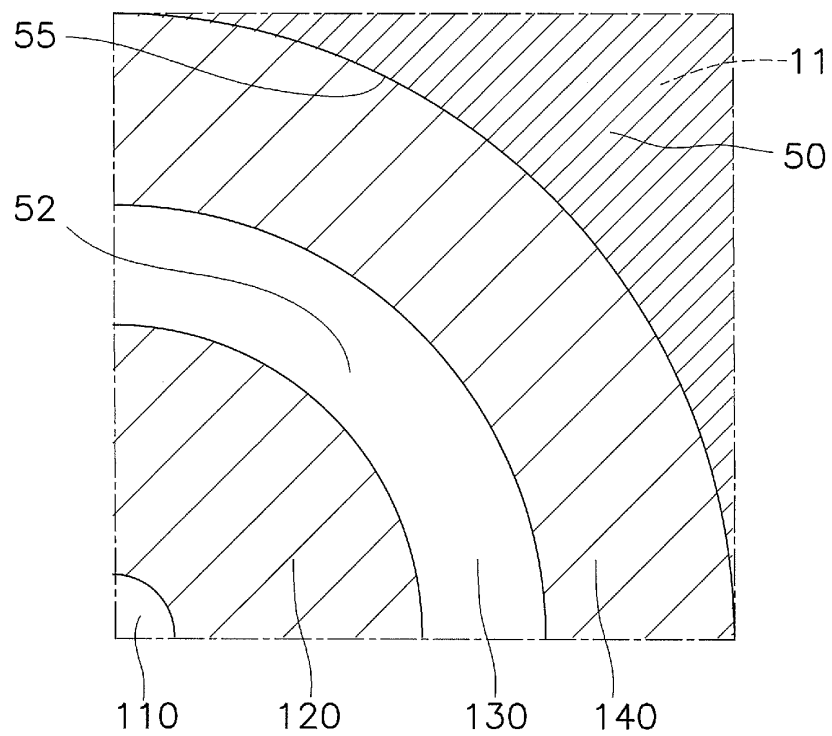
[図34]



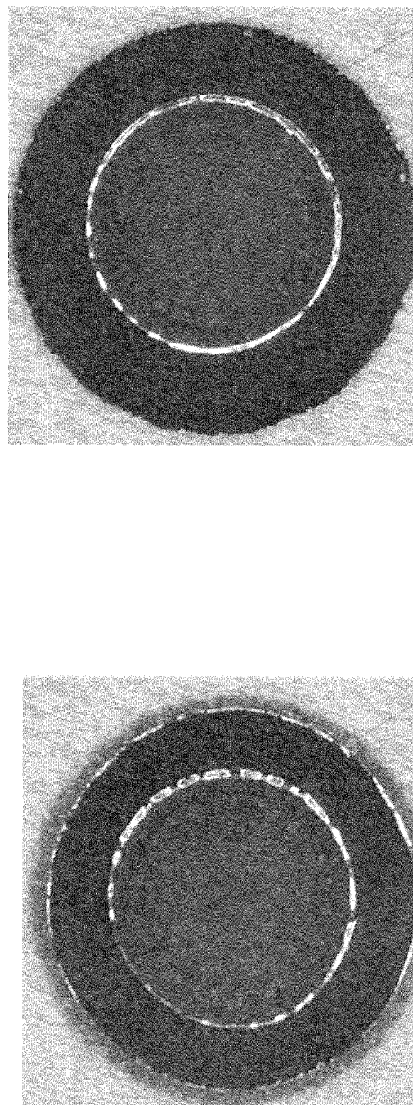
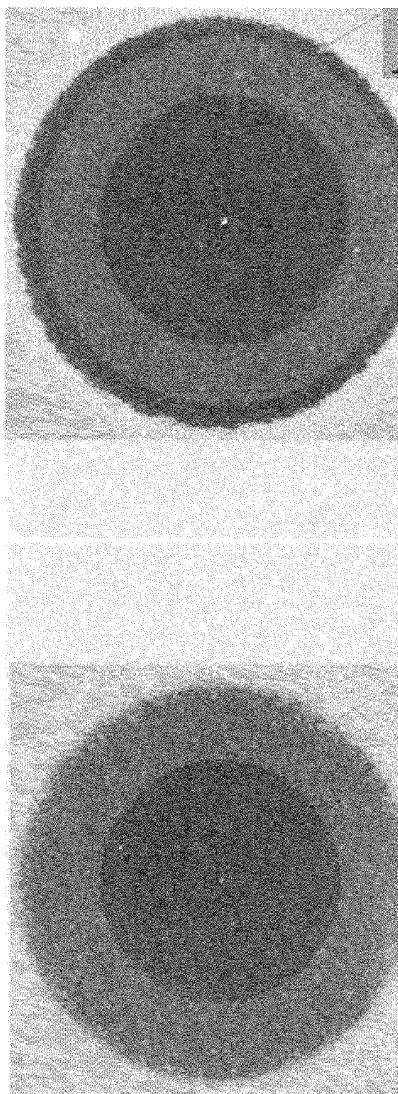
[図35]

10

[図36]

10

[図37]



[図38]

