

What is claimed is:

1. A semiconductor package comprising:
 - a package substrate;
 - a flip chip coupled to the package substrate;
 - an interposer stacked on the flip chip and including an interposer substrate, and a first terminal and a second terminal on an upper surface of the interposer substrate;
 - a bonding wire which connects the first terminal and the package substrate; and
 - a mold layer which covers the interposer, the flip chip and the bonding wire,wherein the mold layer has a signal hole therein which leads to and opens at the second terminal, and at least one dummy hole therein spaced apart from the signal hole and situated over the upper surface of the interposer,
 - wherein part of the mold layer extends over the upper surface of the interposer, and
 - each said at least one dummy hole extends completely through said part of the mold layer, and
 - a protective film on the upper surface of the interposer and exposed by each said at least one dummy hole.
2. The semiconductor package of claim 1, wherein the first and second terminals are disposed on a first region of the upper surface of the interposer, and the protective film is disposed on a second region of the upper surface of the interposer that is apart from the first region.
3. The semiconductor package of claim 1 or claim 2, wherein respective shapes of the signal hole and each said at least one dummy hole are the same.

4. The semiconductor package of any one of claims 1 to 3, wherein the at least one dummy hole comprises a plurality of dummy holes each situated over the upper surface of the interposer, and

the respective sizes of the signal hole and each of the dummy holes, as viewed in a plan view, are the same.

5. The semiconductor package of any one of claims 1 to 4, wherein respective depths of the signal hole and each said at least one dummy hole are the same.

6. The semiconductor package of any one of claims 1 to 5, wherein the signal hole is situated over a first region of the upper surface of the interposer,

the at least one dummy hole is situated over a second region of the upper surface of the interposer, and

the first region is located further towards the outer periphery of the upper surface of the interposer than the second region.

7. The semiconductor package of any one of claims 1 to 6, further comprising:
a micro bump which electrically connects the package substrate and the flip chip.

8. A semiconductor package comprising:
a lower package; and
an upper package stacked on the lower package,
wherein the lower package includes:
a package substrate,
a flip chip coupled to the package substrate,

an interposer stacked on the flip chip and including an interposer substrate, and a first terminal and a second terminal on an upper surface of the interposer substrate, and

a mold layer which covers the interposer and the flip chip,

the mold layer having a signal hole therein which leads to and is open at the second terminal, and at least one dummy hole therein spaced apart from the signal hole and situated over the upper surface of the interposer, and

wherein the at least one dummy hole is filled with a non-electrically conducting medium.

9. The semiconductor package of claim 8, wherein the lower package further includes a solder ball situated in the signal hole as disposed in contact with the second terminal,

wherein the upper package is in contact with the solder ball.

10. The semiconductor package of claim 8 or claim 9, wherein the upper package includes a first memory chip and a second memory chip stacked on the first memory chip.

11. The semiconductor package of any one of claims 8 to 10, wherein the lower package further includes a bonding wire which connects the package substrate and the first terminal.

12. The semiconductor package of any one of claims 8 to 11, wherein the at least one dummy hole comprises a plurality of dummy holes, and
an arrangement of the dummy holes is non-uniform.

13. The semiconductor package of any one of claims 8 to 12, wherein an air gap exists between the upper package and the lower package.

14. A semiconductor package comprising:

- a package substrate;
- a plurality of microbumps disposed on the package substrate;
- a flip chip stacked on the plurality of microbumps and electrically connected to the package substrate via the plurality of microbumps;
- an underfill film which surrounds the plurality of microbumps between the flip chip and the package substrate;
- an adhesive film on the flip chip;
- an interposer which is stacked on the adhesive film and includes an interposer substrate and a first terminal and a second terminal on an upper surface of the interposer substrate;
- a bonding wire which electrically connects the first terminal and the package substrate; and
- a mold layer which covers the interposer, the flip chip and the bonding wire,

wherein the mold layer has a signal hole therein which leads to and is open at the second terminal, and at least one dummy hole therein spaced apart from the signal hole and situated over the upper surface of the interposer; and

- a protective film on the upper surface of the interposer and exposed by each of the at least one dummy hole.

15. The semiconductor package of claim 14, wherein a dimension of the interposer in a horizontal direction parallel to the upper surface thereof is greater than a dimension of the flip chip in said horizontal direction.

16. The semiconductor package of claim 14 or claim 15, further comprising:
a solder ball disposed inside the signal hole.

17. The semiconductor package of claim 16, further comprising:
a memory package stacked on the solder ball.

18. The semiconductor package of any one of claims 14 to 17, wherein the at least one dummy hole comprises a plurality of dummy holes situated over the upper surface of the interposer.

19. The semiconductor package of any one of claims 14 to 18, wherein a thickness of the protective film and a thickness of the second terminal are the same.

20. The semiconductor package of any one of claims 14 to 19, wherein the first and second terminals are disposed on a first region of the upper surface of the interposer, and the protective film is disposed on a second region of the upper surface of the interposer that is apart from the first region and is not disposed on the first region.