## Description

This invention relates to an improvement on the method of manufacturing a lateral transistor. A lateral PNP transistor has been produced, for example, by the following steps. First, an N type silicon layer is deposited on a P type semiconductor substrate. The N type silicon layer is divided into a plurality of N type islands by a P type element-isolating region. A thick oxide layer is mounted on part of an element-isolating region and an island. A thin oxide layer is laid in that part of the island on which the silicon layer is exposed. An annular resist pattern is deposited on the thin oxide layer.

A P type impurity is ion implanted into an N type base region through the thin oxide layer. At this time, the resist pattern is used as a mark. The resist pattern is removed. The implanted ion is activated. As a result, an emitter region is formed on that part of the silicon layer which corresponds to the hollow portion of the annular resist pattern. At this time, an annular collector region is formed on that part of the silicon layer which is defined between the outer peripheral wall of the resist pattern and the inner peripheral wall of the thick oxide layer. As a result, an annular region lying between the emitter and collector regions is converted into a base region. A resist pattern is mounted on the thin oxide layer. The resist pattern has an opening formed in that part thereof which faces the part in which a bare leadout region is to be formed. An N type impurity is ion implanted into a silicon layer (base region) through a thin oxide layer with the resist pattern used as a mask. The resist pattern is removed. As a result, the implanted ion is activated to provide a base electrode leadout region.

A CVD-$SiO_2$ layer is deposited over the whole surface of the resultant structure. The CVD-$SiO_2$ layer and thin oxide layer are selectively etched. This etching process provides a base electrode leadout contact hole, an emitter electrode leadout contact hole, and a collector electrode leadout contact hole. An aluminium layer is deposited over the whole surface of the resultant structure. The aluminium layer is patterned, thereby providing a base electrode, an emitter electrode and a collector electrode. These electrodes are connected to the corresponding base electrode leadout region, emitter electrode leadout region, and collector electrode leadout region. Hitherto a lateral PNP transistor has generally been fabricated in the above-mentioned manner. One of such manufacturing methods is disclosed, for example, in Japanese patent publication Sho 41-5656 (priority claim NO 284611 filed in USA on May 31, 1963).

With the lateral type PNP transistor, the magnitude of collector electrode is proportional to the effective area of the emitter region. In other words, the magnitude of the collector current is proportional to the peripheral length of the emitter region. On the other hand, the base current flows toward the bottom of the emitter region. Therefore, the base current increases with a rise in the area of the emitter region. To elevate current gain (or amplitude), therefore, it is necessary not only to narrow the base width, but to reduce the real area of the emitter region and to enlarge a ratio between the effective area of the emitter region (or its peripheral length) and the real area of the emitter region.

In the above-mentioned lateral transistor-manufacturing method, the deposition of the emitter and collector regions, and the boring of the emitter electrode leadout contact hole are carried out by applying different resist patterns. In the manufacture of the subject lateral transistor, therefore, it is necessary to take into account the difficulties which might occur in matching the different resist patterns used in masks. Now let it be assumed that an annular resist pattern is formed having a small hollow area to provide a small emitter region. In this case, if a resist used for the selective etching of a layer (for example, CVD-$SiO_s$) fails to be masked with high precision, the resultant emitter electrode contact hole will spread over an area including the emitter and base regions. In such case, the emitter and base regions are short circuited by the emitter electrode. To suppress the occurrence of short circuiting between the emitter and base regions, it is necessary to expand the emitter region and provide a sufficient margin for masking. In the conventional method of manufacturing a lateral transistor, therefore, a limitation was imposed on the noticeable dimensional reduction of the area of the emitter region, thus presenting difficulties in dense integration of transistors and the manufacture of a transistor ensuring a high current gain.

The object of the present invention is to provide a method of manufacturing, for example, a lateral transistor whose emitter region can be noticeably reduced in size.

According to the invention, there is provided a method of manufacturing a lateral transistor which comprises the steps of: providing semiconductor body of first conductivity type; forming at least one annular pattern above the main surface of said semiconductor body; implanting an impurity of second conductivity type in said semiconductor body with said pattern used as a mask, thereby forming first layer of second conductivity type facing the inner peripheral wall of said annular pattern; depositing an insulation layer on said resultant structure; and boring a contact hole in said insulation layer, and characterized in that the step of providing said insulation layer is taken by retaining said annular pattern and depositing at least one insulation layer on the resultant structure, and the boring step has the step of boring a contact hole in

said insulation layer in the self-aligned fashion with respect to said annual pattern.

Therefore, it is unnecessary to provide a masking margin for the formation of the first region as well as the contact hole. Moreover neither the contact hole extends beyond the boundary of the first region, nor is the semiconductor layer found to be short circuited by each other. Therefore, it is possible to reduce the dimension of the first region, providing a highly integrated lateral transistor possessing a high current amplitude.

In one embodiment, the annular pattern is prepared from silicon nitride, but it can also be prepared from metal silicide, or from a polycide representing a composite body comprising metal silicide and polycrystalline silicon.

This invention can be more fully understood by way of example from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Figs. 1A to 1F are sectional views showing the sequential steps of manufacturing a lateral transistor embodying this invention.

Fig. 2 is a plan view of a lateral transistor manufactured by the method collectively illustrated by Figs. 1A to 1F;

Fig. 3 is a sectional view on line III-III of the transistor shown in Fig. 2; and

Figs. 4 and 5 are curve diagrams comparing the properties of a lateral transistor manufactured by the conventional method with the lateral transistor embodying this invention.

Description may now be made with reference to Figs. 1A to 1F, 2, and 3 illustrating the method of this invention for manufacturing a lateral PNP transistor. Figs. 1A to 1E are sectional views showing the sequential steps of manufacturing a PNP lateral transistor embodying this invention. Figs. 1F and 3 are sectional views of a finished PNP lateral transistor embodying the invention. Fig. 1F corresponds to sectional view on line I-I of Fig. 2. Fig. 3 corresponds to sectional view on line III-III of Fig. 2.

Description may now be made of the sequential steps of manufacturing the subject lateral transistor. First, there is a P type silicon substrate 21 having an impurity concentration of $10^{14}$ to $10^{16}/cm^3$. The main surface of silicon substrate 21 is selectively doped with an N type impurity (for example, antimony) by ion implantation or diffusion. N type silicon layer 23 is opitaxially grown on the main surface of silicon substrate 21. Silicon layer 23 is prepared with an impurity concentration of $10^{14}$ to $10^{16}/cm^3$ and with a thickness of about 1 to 20 microns. In this embodiment, the ion-implanted N type impurity is redistributed through substrate 21. At this time, the N type impurity is also carried into silicon layer 23 by auto doping. An N type embedded layer 25 is formed by the above-mentioned steps. When N type embedded layer 25 completes the function of reducing base resistance, the impurity concentration in layer 25 is at a level ranging between $10^{18}$ and $10^{20}/cm^3$. The structure illustrated in Fig. 1A results from the above-mentioned steps.

A P type impurity (for example, boron) is selectivery doped in N type silicon layer 23. The doped impurity is activated to provide $P^+$ type element-isolating region 27. This element-isolating region 27 causes island 29 electrically isolated from other elements, to be formed in N type silicon layer 23. Island 29 acts as the base region of the PNP transistor. Therefore, hereinafter island 29 is referred to as "base region 29." Selective oxidation is applied to the surface of the resultant structure, causing field oxide layer 31 having a thickness of 900 nm to be formed on a part of element isolating region 27 and base region 29. Field oxide layer 31 is formed on a region other than that on which emitter and collector regions and base electrode leadout layer are to be formed. The structure illustrated in Fig. 1B results from the aforementioned steps.

Oxide layer 33 is thermally deposited on the exposed portion of base region 29 (that portion of base region 29 which is not covered with field oxide layer 31). Oxide layer 33 is deposited with a thickness of, for example, 50 nm. A polycrystalline silicon layer is deposited over the whole surface of the resultant structure with a thickness of, for example, 350 nm. The polycrystalline layer is patterned to provide annular polycrystalline silicon pattern 35 in oxide layer 33. The structure of Fig. 1C results from the abovementioned steps.

A P type impurity, for example, boron is ion implanted into base region 29 through oxide layer 33 by applying a mask composed of field oxide layer 31, polycrystalline silicon pattern 35 and, if necessary, a resist layer. The ion implantation is carried out under the conditions prescribed, for example, as follows:

| | |
|---|---|
| Acceleration voltage | 35 kV |
| Dosage | $2 \times 10^{15}/cm^2$ |

The implanted P type ion is activated to form P type emitter region 37 and annular P type collector region 39 in base region 29. P type emitter region 37 is deposited in that portion of base region 29 which faces the hollow part of annular pattern 35. Further, annular P type collector region 39 is formed in that

portion of base region 29 which is interposed between the outer periphery of annular pattern 35 and the inner periphery of field oxide layer 31. Namely, emitter region 37 and collector region 39 are formed in a self-aligned fashion with respect to annular pattern 35. Oxide layer 33 deposited on that part on which the base electrode leadout region is to be formed is selectively etched to provide an opening. Further, a resist pattern (not shown) is formed. An N type impurity (for example, arsenic) is selectively ion implanted on base region 29. The aforementioned resist pattern is removed. The resultant structure is subjected to thermal oxidation at a temperature of 900°C. As a result, the implanted ion is activated, and base electrode leadout region 41 (Fig. 3) is formed in base region 29. Further, oxide layer 43 is deposited on annular polycrystalline silicon pattern 35 and the surface of base region 29. The structure of Fig. 1D results from the above-mentioned steps.

CVD-$SiO_2$ layer 45 is spread over the whole surface of the resultant structure. Silicon nitride layer (passivation layer) 47 is deposited on CVD-$SiO_2$ layer 45. The structure of Fig. 1E results from the aforementioned steps.

A resist pattern (not shown) is formed in such a manner that openings are provided on those portions in which contact holes are to be formed to lead out of the emitter electrode, base electrode, and collector electrode. As shown in Fig. 3, the silicon nitride layer 47, CVD-$SiO_2$ layers 45 and oxide layers 33, 43, deposited on base electrode leadout region 41, emitter region 37 and collector region 39, are selectively etched, thereby providing base electrode leadout contact hole 49, emitter electrode leadout contact hole 51, and collector electrode leadout contact hole 53 (Figs. 2 and 3). It is assumed that a resist mask for the formation of the emitter electrode leadout contact hole 51 is slightly displaced from the original position. Even with such an occasion, the annular silicon pattern 35 acts as an etching mask, thereby giving rise to a small possibility that contact hole 51 is so formed as to overlap base region 29. Namely, the contact hole 51 is formed in a self-aligned fashion with respect to the annular pattern 35. Emitter region 37, too, is formed in a self-aligning fashion with respect to said annular pattern 35. Consequently, contact hole 51 is also formed in a self-aligned fashion with respect to emitter region 37. As a result, emitter region 37 and base region 39 are little likely to be electrically connected together by means of the later described aluminium element. An aluminium layer is deposited over the whole surface of the resultant structure. The aluminium layer is patterned to provide base electrode 55, emitter electrode 57, and collector electrode 59. Base electrode 55, emitter electrode 57, and collector electrode 59 all prepared from aluminium are respectively connected to the corresponding base electrode leadout region 41, emitter region 37, and collector region 39 through contact holes 49, 51, and 53. A lateral PNP transistor whose section is shown in Fig. 1F, whose plan view is given in Fig. 2 and whose particular cross section on line III-III of Fig. 2 is indicated in Fig. 3 is manufactured by the aforementioned steps.

According to the present invention, emitter region 37 and collector region 39 are formed with annular polycrystalline silicon pattern 35 used as a mask. Later, emitter electrode contact hole 51 is formed with annular silicon pattern 35 retained. In this case, annular silicon pattern 35 acts as a second etching mask. Therefore, even if a resist mask for the formation of emitter electrode leadout contact hole 51 should happen to be displaced, the position of contact hole 51 is restricted by annular silicon pattern 35 (Fig. 1). Consequently, a contact hole is prevented from being so formed as to overlap emitter region 37 and base region 29. In other words, the contact hole is formed in a self-aligned fashion on emitter region 37. Should, therefore, the masking of a resist for the formation of a contact hole be displaced within the width of the annular pattern, no difficulties will arise. Consequently, no short circuiting will arise between the base and emitter regions when emitter electrode 57 is formed. Therefore, it is unnecessary to provide a masking margin when emitter region 39 and emitter contact hole 51 are formed, thereby reducing the area of emitter region 37 and ensuring the manufacture of a lateral transistor having a high current amplitude.

If polycrystalline silicon pattern 35 is retained and not electrically connected to any other terminal, polycrystalline silicon pattern 35 will act as a floating gate, tending to give rise to a malfunction of the transistor due to an injection of carriers from the substrate. With a lateral transistor embodying this invention, however, emitter electrode 57 is connected to polycrystalline silicon 35. Pattern 35 is connected to emitter region 37 having a slight voltage difference from base region 29. Therefore, pattern 35 is prevented from acting as a floating gate, thereby suppressing the deterioration of the characteristics of a transistor.

Further, there is the possibility that polycrystalline pattern 35 will act as a gate electrode; the emitter and collector act as a drain or source; and a leak current regions to flow. In such case, the occurrence of a leak current is generally suppressed by causing the emitter to be impressed with a high voltage and the collector to be impressed with a low voltage. Customarily, the adoption of the above-mentioned process ensures a suppression of any problem.

The foregoing embodiment involved the application of two layers, that is, CVD-$SiO_2$ layer 45 and silicon

nitride layer 47. However, it is possible in the case of either one. Further, CVD-$SiO_2$ layer 45 need not be exclusively used, but it is possible to apply plasma $SiO_2$ or any other insulation layer.

The foregoing description relates to the case where the present invention is applied to the manufacture of a PNP lateral transistor. However, the invention is also applicable to the manufacture of an NPN lateral transistor.

Figs. 4 and 5 give an experimental comparison between the properties of a lateral transistor manufactured by the present invention and those the conventional lateral transistor. Fig. 4 is a curve diagram indicating the relationship between the current amplitude $\beta$ and collector current [A] observed in the present invention and the conventional lateral transistor. Fig. 5 is a curve diagram showing the relationship between the cutoff frequency fT [Hz] of a transistor and collector current [A] observed in the present invention and conventional lateral transistor. Throughout Figs. 4 and 5, curve A represents the property of a lateral transistor manufactured by the method of the invention. Curve B denotes the property of a lateral transistor manufactured by the conventional process. Fig. 4 clearly indicates that the current amplitude of the lateral transistor of the present invention increased 2 to 3 times over that of the conventional type. Fig. 5 distinctly shows that the cutoff frequency of a lateral transistor produced by the present invention was about 10 times higher than that of the conventional lateral transistor. Further, the lateral transistor of the present invention has the merit that it occupies an area about 20 to 25 % reduced from that of the conventional lateral transistor.

## Claims

1. A method of manufacturing a lateral transistor which comprises the steps of:
providing a semiconductor body of first conductivity type;
forming at least one annular pattern above the main surface of said semiconductor body;
implanting an impurity of second conductivity type in said semiconductor body with said pattern used as a mask, thereby forming a first layer of second conductivity type facing the inner peripheral wall of said annular pattern;
depositing an insulation layer on said resultant structure; and
boring a contact hole in said insulation layer, and characterised in that the step of providing said insulation layer (45, 47) is taken by retaining said annular pattern (35) and depositing at least one insulation layer (45, 47) on the resultant structure, and the boring step has the step of boring a contact hole (51) in said insulation layer (45, 47) in the self-aligned fashion with respect to said annular pattern (35).

2. The method of manufacturing a transistor according to claim 1, characterized in that said ion-implanting step has the step of implanting an impurity of second conductivity type (P) in said semiconductor body (29) with said annular pattern (35) used as a mask, thereby forming said first layer (37) and a second layer (39) in the self-aligning fashion with respect to said annular pattern (35); and said boring step has the step of forming at least one hole (51), which reaches said first layer (37), formed in said insulation layer, in the self-aligning fashion with respect to said annular pattern (35), with said annular pattern (35) used as a mask.

3. The method of manufacturing a lateral transistor according to claim 1, characterized in that said step of forming the annular pattern comprises the steps of:
forming at least one insulation layer (31) having an opening on the main surface of the semiconductor body;
depositing a second insulation layer (33) thinner than said first insulation layer (31) on that portion of said semiconductor body (29) which faces said opening; and
forming annular pattern (35) on said second insulation layer (33) at a predetermined distance from said first insulation layer (31), and characterized in that said ion implantating step comprises the steps of forming said first layer (37) on that portion of said semiconductor body (29) which faces said hollow area of said annular pattern (35) and forming a second layer (39) in a position interposed between the outer peripheral wall of said annular pattern (35) and the inner peripheral wall of said first insulation layer (31), and which further comprises the step of etching said second insulation layer (33) and said insulation layer (45, 47) both facing the hollow area of said annular pattern (35) with said pattern (35) used as a mask.

4. The method of manufacturing a lateral transistor according to claim 1, which further comprises the step

nitride layer 47. However, it is possible in the case of either one. Further, CVD-$SiO_2$ layer 45 need not be exclusively used, but it is possible to apply plasma $SiO_2$ or any other insulation layer.

The foregoing description relates to the case where the present invention is applied to the manufacture of a PNP lateral transistor. However, the invention is also applicable to the manufacture of an NPN lateral transistor.

Figs. 4 and 5 give an experimental comparison between the properties of a lateral transistor manufactured by the present invention and those the conventional lateral transistor. Fig. 4 is a curve diagram indicating the relationship between the current amplitude $\beta$ and collector current [A] observed in the present invention and the conventional lateral transistor. Fig. 5 is a curve diagram showing the relationship between the cutoff frequency fT [Hz] of a transistor and collector current [A] observed in the present invention and conventional lateral transistor. Throughout Figs. 4 and 5, curve A represents the property of a lateral transistor manufactured by the method of the invention. Curve B denotes the property of a lateral transistor manufactured by the conventional process. Fig. 4 clearly indicates that the current amplitude of the lateral transistor of the present invention increased 2 to 3 times over that of the conventional type. Fig. 5 distinctly shows that the cutoff frequency of a lateral transistor produced by the present invention was about 10 times higher than that of the conventional lateral transistor. Further, the lateral transistor of the present invention has the merit that it occupies an area about 20 to 25 % reduced from that of the conventional lateral transistor.

## Claims

1. A method of manufacturing a lateral transistor which comprises the steps of:
providing a semiconductor body of first conductivity type;
forming at least one annular pattern above the main surface of said semiconductor body;
implanting an impurity of second conductivity type in said semiconductor body with said pattern used as a mask, thereby forming a first layer of second conductivity type facing the inner peripheral wall of said annular pattern;
depositing an insulation layer on said resultant structure; and
boring a contact hole in said insulation layer, and characterised in that the step of providing said insulation layer (45, 47) is taken by retaining said annular pattern (35) and depositing at least one insulation layer (45, 47) on the resultant structure, and the boring step has the step of boring a contact hole (51) in said insulation layer (45, 47) in the self-aligned fashion with respect to said annular pattern (35).

2. The method of manufacturing a transistor according to claim 1, characterized in that said ion-implanting step has the step of implanting an impurity of second conductivity type (P) in said semiconductor body (29) with said annular pattern (35) used as a mask, thereby forming said first layer (37) and a second layer (39) in the self-aligning fashion with respect to said annular pattern (35); and said boring step has the step of forming at least one hole (51), which reaches said first layer (37), formed in said insulation layer, in the self-aligning fashion with respect to said annular pattern (35), with said annular pattern (35) used as a mask.

3. The method of manufacturing a lateral transistor according to claim 1, characterized in that said step of forming the annular pattern comprises the steps of:
forming at least one insulation layer (31) having an opening on the main surface of the semiconductor body;
depositing a second insulation layer (33) thinner than said first insulation layer (31) on that portion of said semiconductor body (29) which faces said opening; and
forming annular pattern (35) on said second insulation layer (33) at a predetermined distance from said first insulation layer (31), and characterized in that said ion implantating step comprises the steps of forming said first layer (37) on that portion of said semiconductor body (29) which faces said hollow area of said annular pattern (35) and forming a second layer (39) in a position interposed between the outer peripheral wall of said annular pattern (35) and the inner peripheral wall of said first insulation layer (31), and which further comprises the step of etching said second insulation layer (33) and said insulation layer (45, 47) both facing the hollow area of said annular pattern (35) with said pattern (35) used as a mask.

4. The method of manufacturing a lateral transistor according to claim 1, which further comprises the step

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of forming an electrode terminal (57) which contacts said first layer (37) of second conductivity type through said hole (51).

5. The method of manufacturing a lateral transistor according to claim 1, characterized in that said annular pattern (35) is prepared from a material which can be etched at a slower rate per unit time than said insulation layer (45, 47).

6. The method of manufacturing a lateral transistor according to claim 5, characterized in that said annular pattern (35) is prepared from polycrystalline silicon.

7. The method of manufacturing a lateral transistor according to claim 5, characterized in that said annular pattern (35) is prepared from silicon nitride.

8. The method of manufacturing a lateral transistor according to claim 5, characterized in that said annular pattern (35) is prepared from metal silicide.

9. The method of manufacturing a lateral transistor according to claim 5, characterized in that said annular pattern (35) is prepared from a polycide representing a composite body comprising metal silicide and polycrystalline silicon.

**Revendications**

1. Procédé de fabrication d'un transistor latéral, comprenant les étapes de :
fourniture d'un corps semiconducteur d'un premier type de conductivité ;
formation d'au moins un motif annulaire au-dessus de la surface principale dudit corps semiconducteur ;
implantation d'une impureté d'un second type de conductivité dans ledit corps semiconducteur, ledit motif étant utilisé en tant que masque, d'où la formation d'une première couche du second type de conductivité qui fait face à la paroi périphérique interne dudit motif annulaire ;
dépôt d'une couche d'isolation sur ladite structure résultante ; et
perçage d'un trou de contact dans ladite couche d'isolation,
caractérisé en ce que l'étape de formation de ladite couche d'isolation (45, 47) est réalisée en conservant ledit motif annulaire (35) et en déposant au moins une couche d'isolation (45, 47) sur la structure résultante et en ce que l'étape de perçage comporte l'étape de perçage d'un trou de contact (51) dans ladite couche d'isolation (45, 47) d'une manière autoalignée par rapport audit motif annulaire (35).

2. Procédé de fabrication d'un transistor selon la revendication 1, caractérisé en ce que ladite étape d'implantation ionique comporte l'étape d'implantation d'une impureté d'un second type de conductivité (P) dans ledit corps semiconducteur (29), ledit motif annulaire (35) étant utilisé en tant que masque, d'où la formation de ladite première couche (37) et d'une seconde couche (39) d'une manière autoalignée par rapport audit motif annulaire (35) ; et ladite étape de perçage comporte l'étape de formation d'au moins un trou (51) qui atteint ladite première couche (37), ce trou étant formé dans ladite couche d'isolation d'une manière auto-alignée par rapport audit motif annulaire (35), ledit motif annulaire (35) étant utilisé en tant que masque.

3. Procédé de fabrication d'un transistor latéral selon la revendication 1, caractérisé en ce que ladite étape de formation du motif annulaire comprend les étapes de :
formation d'au moins une couche d'isolation (31) comportant une ouverture sur la surface principale du corps semiconducteur ;
dépôt d'une seconde couche d'isolation (33) plus mince que ladite première couche d'isolation (31) sur cette partie dudit corps semiconducteur (29) qui fait face à ladite ouverture ; et
formation d'un motif annulaire (35) sur ladite seconde couche d'isolation (33) à une distance prédéterminée de ladite première couche d'isolation (31),
caractérisé en ce que ladite étape d'implantation ionique comprend les étapes de formation de ladite première couche (37) sur cette partie dudit corps semiconducteur (29) qui fait face à ladite zone évidée dudit motif annulaire (35) et de formation d'une seconde couche (39) en une position interposée entre la paroi périphérique externe dudit motif annulaire (35) et la paroi périphérique interne de ladite

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première couche d'isolation (31), et en ce qu'elle comprend en outre l'étape de gravure de ladite seconde couche d'isolation (33) et de ladite couche d'isolation (45, 47) qui font toutes deux face à la zone évidée dudit motif annulaire (35) en utilisant ledit motif (35) en tant que masque.

4. Procédé de fabrication d'un transistor latéral selon la revendication 1, comprenant en outre l'étape de formation d'une borne d'électrode (57) qui est en contact avec ladite première couche (37) du second type de conductivité au travers dudit trou (51).

5. Procédé de fabrication d'un transistor latéral selon la revendication 1, caractérisé en ce que ledit motif annulaire (35) est préparé à partir d'un matériau qui peut être gravé selon un vitesse de gravure inférieure à celle de ladite couche d'isolation (45, 47).

6. Procédé de fabrication d'un transistor latéral selon la revendication 5, caractérisé en ce que ledit motif annulaire (35) est préparé à partir de silicium polycristallin.

7. Procédé de fabrication d'un transistor latéral selon la revendication 5, caractérisé en ce que ledit motif annulaire (35) est préparé à partir de nitrure de silicium.

8. Procédé de fabrication d'un transistor latéral selon la revendication 5, caractérisé en ce que ledit motif annulaire (35) est préparé à partir de siliciure de métal.

9. Procédé de fabrication d'un transistor latéral selon la revendication 5, caractérisé en ce que ledit motif annulaire (35) est préparé à partir d'un polycide qui représente un corps composite comprenant du siliciure de métal et du silicium polycristallin.

**Patentansprüche**

1. Herstellungsverfahren eines lateralen Transistors mit den folgenden Schritten:
Schaffen eines Halbleiterkörpers eines ersten Leitfähigkeitstyps;
Bilden von wenigstens einem ringförmigen Muster auf der Hauptoberfläche des Halbleiterkörpers;
Implantieren einer Verunreinigung eines zweiten Leitfähigkeitstyps in dem Halbleiterkörper unter Verwendung des Musters als eine Maske, wodurch eine erste Schicht vom zweiten Leitfähigkeitstyp gebildet wird, die der inneren Umfangswand des ringförmigen Musters zugekehrt ist;
Aufbringen einer Isolationsschicht auf der sich ergebenden Struktur;
und Bohren eines Kontaktloches in die Isolationsschicht,
dadurch **gekennzeichnet,** daß daß der Schritt des Schaffens der Isolationsschicht (45, 47) unter Beibehaltung des ringförmigen Musters (35) durchgeführt wird, und wenigstens eine Isolationsschicht (45, 47) auf der sich ergebenden Struktur aufgebracht wird, und der Bohr-Schritt den Schritt des Bohrens eines Kontaktloches (51) in der Isolationsschicht (45, 47) in einer selbstausrichtenden Art und Weise bezüglich des ringförmigen Musters (35) aufweist.

2. Herstellungsverfahren eines Transistors nach Anspruch 1,
dadurch **gekennzeichnet,** daß der Ionenimplantierungsschritt den Schritt des Implantierens einer Verunreinigung eines zweiten Leitfähigkeitstyps (P) in dem Halbleiterkörper (29) unter Verwendung des ringförmigen Musters (35) als Maske aufweist, wodurch die erste Schicht (37) und eine zweite Schich6 (39) in der selbstausrichtenden Art und Weise bezüglich des ringförmigen Musters (35) gebildet wird; und der Bohr-Schritt den Schritt des Bildens wenigstens eines Loches (51) aufweist, das die erste in der Isolationsschicht gebildete Schicht (37) in der selbstausrichtenden Art und Weise bezüglich des ringförmigen Musters (35) unter Verwendung des ringförmigen Musters (35) als Maske erreicht.

3. Herstellungsverfahren eines lateralen Transistors nach Anspruch 1,
dadurch **gekennzeichnet,** daß der Schritt des Bildens des ringförmigen Musters die folgenden Schritte umfaßt:
Bilden wenigstens einer Isolationsschicht (31) mit einer Öffnung auf der Hauptoberfläche des Halbleiterkörpers;
Aufbringen einer zweiten Isolationsschicht (33), die dünner ist als die erste Isolationsschicht (31) auf demjenigen Abschnitt des Halbleiterkörpers (29), der der Öffnung zugewandt ist; und
Bilden eines ringförmigen Musters (35) auf der zweiten Isolationsschicht (33) in einem vorgegebenen

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Abstand von der ersten Isolationsschicht (31), und dadurch gekennzeichnet, daß der Ionenimplantierungsschritt die Schritte des Bildens der ersten Schicht (37) auf demjenigen Abschnitt des Halbleiterkörpers (29), der der hohlen Fläche des ringförmigen Musters (35) zugewandt ist und des Bildens einer zweiten Schicht (39) an einer Position, die zwischen der äußeren Umfangswand des ringförmigen Musters (35) und der inneren Umfangswand der ersten Isolationsschicht (31) zwischenliegt, umfaßt, und außerdem den Schritt des Ätzens der zweiten Isolationsschicht (33) und der Isolationsschicht (45, 47) umfaßt, wobei beide der hohlen Fläche des ringförmigen Musters (35) unter Verwendung des Musters (35) als Maske zugewandt sind.

4. Herstellungsverfahren eines lateralen Transistors nach Anspruch 1, dadurch **gekennzeichnet,** daß es außerdem den Schritt des Bildens eines Elektrodenanschlusses (57) umfaßt, der die erste Schicht (37) des zweiten Leitfähigkeitstyps durch das Loch (51) kontaktiert.

5. Herstellungsverfahren eines lateralen Transistors nach Anspruch 1, dadurch **gekennzeichnet,** daß das ringförmige Muster (35) aus einem Material hergestellt ist, das mit einer langsameren Rate pro Einheitszeit als die Isolationsschicht (45, 47) geätzt werden kann.

6. Herstellungsverfahren eines lateralen Transistors nach Anspruch 5, dadurch **gekennzeichnet,** daß das ringförmige Muster (35) aus polykristallinem Silizium hergestellt wird.

7. Herstellungsverfahren eines lateralen Transistors nach Anspruch 5, dadurch **gekennzeichnet,** daß das ringförmige Muster (35) aus Siliziumnitrid hergestellt wird.

8. Herstellungsverfahren eines lateralen Transistors nach Anspruch 5, dadurch **gekennzeichnet,** daß das ringförmige Muster (35) aus Metallsilizid hergestellt wird.

9. Herstellungsverfahren eines lateralen Transistors nach Anspruch 5, dadurch **gekennzeichnet,** daß das ringförmige Muster (35) aus einem Polyzid hergestellt wird, das einen zusammengesetzten Körper umfassend Metallsilizid und polykristallines Silizium darstellt.