

[0005] For example, the insulation layers may be deposited to include silicon oxide or silicon nitride, and thus a silicon oxide layer and a silicon nitride layer may be formed.

[0006] When the insulation layers are etched to form patterns, a selective etching process with respect to a specific layer may be required. For example, a selective
5 etching process for the silicon nitride layer may be needed. In this case, an etchant composition for only etching the silicon nitride layer while sufficiently protecting the silicon oxide layer may be used.

[0007] Further, when the selective etching process is performed for a long period at a high temperature, a steady and stable protection of the silicon oxide layer is needed.

10 **[0008]** For example, Korean Registered Patent Publication No. 10-0823461 discloses a composition for etching both silicon oxide layer and silicon nitride layer, however, the selective etching process as described above may not be realized from the composition.

SUMMARY

15 **[0009]** According to an aspect of the present invention, there is provided an insulation layer etchant composition having improved etching selectivity and uniformity.

[0010] According to an aspect of the present invention, there is provided a method of forming patterns using the insulation layer etchant composition.

[0011] The above aspects of the present inventive concepts will be achieved by the
20 following features or constructions:

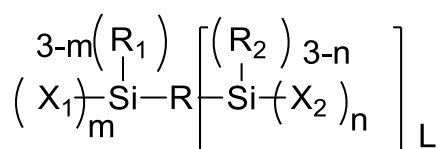
[0012] (1) An insulation layer etchant composition, comprising phosphoric acid; a multi-podal silane compound in which a plurality of silane groups are combined with each other via a linker group including at least one carbon atom; and a remainder of water.

[0013] (2) The insulation layer etchant composition according to the above (1), wherein each of the silane groups included in the multi-podal silane compound includes a plurality of passivation groups.

[0014] (3) The insulation layer etchant composition according to the above (2), wherein the passivation group includes an alkoxy group, halogen or a phosphate group.

[0015] (4) The insulation layer etchant composition according to the above (1), wherein the multi-podal silane compound includes a compound represented by Chemical Formula 1 below:

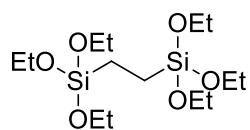
[0016] [Chemical Formula 1]



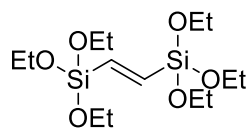
[0017] wherein, in the Chemical Formula 1 above, R represents the linker group, and is a divalent organic group including at least one carbon atom, R_1 and R_2 are each independently a C1 to C12 alkyl group or a C6 to C12 aryl group, X_1 and X_2 are each independently halogen, $-OR_3$ group or a phosphate group, R_3 is a C1 to C10 alkyl group capable of including an ether bond, or a C6 to C12 aryl group, L is an integer of 1 or 2, and m and n are each independently an integer of 1 to 3.

[0018] (5) The insulation layer etchant composition according to the above (4), wherein the multi-podal silane compound includes at least one selected from a group consisting of di-podal silane compounds represented by Chemical Formulae 2-1 to 2-7 below:

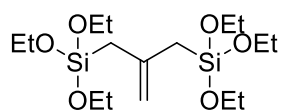
[0019] [Chemical Formula 2-1]



[0020] [Chemical Formula 2-2]

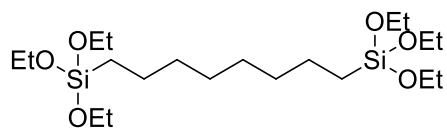


[0021] [Chemical Formula 2-3]

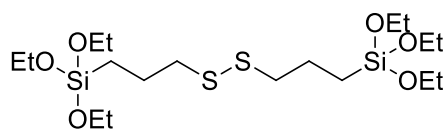


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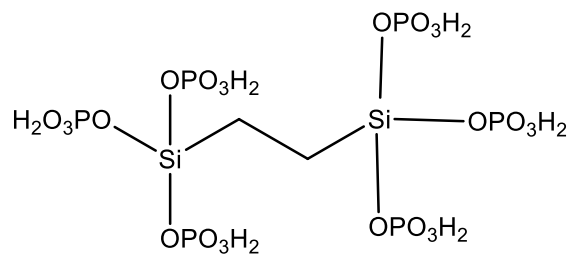
[0022] [Chemical Formula 2-4]



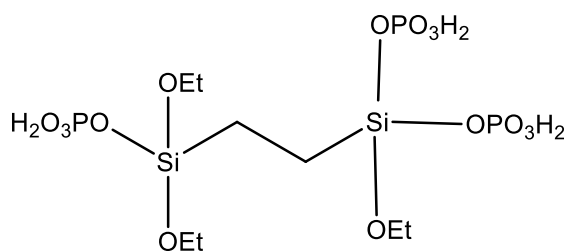
[0023] [Chemical Formula 2-5]



10 **[0024]** [Chemical Formula 2-6]



[0025] [Chemical Formula 2-7]

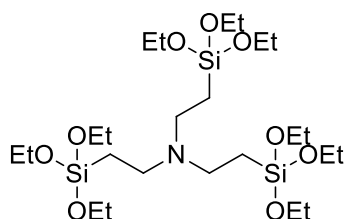


[0026] wherein, in the Chemical Formulae 2-1 to 2-7 above, Et represents an ethyl group.

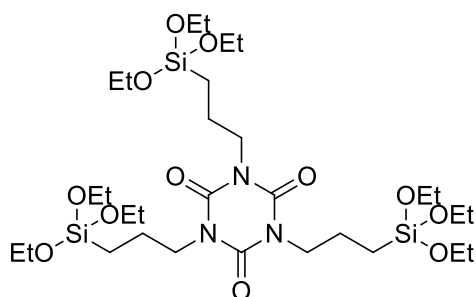
[0027] (6) The insulation layer etchant composition according to the above (4),

5 wherein the multi-podal silane compound includes at least one selected from a group consisting of tri-podal silane compounds represented by Chemical Formulae 3-1 and 3-2 below:

[0028] [Chemical Formula 3-1]



10 **[0029]** [Chemical Formula 3-2]



[0030] wherein, in the Chemical Formulae 3-1 and 3-2 above, Et represents an ethyl group.

[0031] (7) The insulation layer etchant composition according to the above (1),

15 wherein an amount of the multi-podal silane compound is in a range from 0.0001 wt%

to 1 wt% based on a total weight of the composition.

[0032] (8) The insulation layer etchant composition according to the above (1), wherein a compound including a siloxane bond (-Si-O-Si-) is excluded from the composition.

5 **[0033]** (9) A method of forming patterns, comprising: forming an oxide layer and a nitride layer on a substrate; and selectively etching the nitride layer using the insulation layer etchant composition according to any one of the above (1) to (8).

[0034] (10) The method according to the above (9), wherein the oxide layer includes a silicon oxide layer and the nitride layer includes a silicon nitride layer.

10 **[0035]** According to exemplary embodiments as described above, the insulation layer etchant composition may include phosphoric acid and a multi-podal silane compound. In the multi-podal silane compound, a plurality of passivation groups may be combined with each silicon atom so that a passivation effect for, e.g., a silicon oxide layer may be promoted.

15 **[0036]** Further, the multi-podal silane compound may include a linker group that may combine a plurality of silane groups, and may include at least one carbon atoms. A chelating effect for substantially protecting the silicon oxide layer may be implemented by the linker group so that the passivation effect for the silicon oxide layer may be additionally increased. Additionally, a dissociation of the silane groups may be
20 suppressed in phosphoric acid at a high temperature so that an etching performance may be maintained uniformly for a long period.

[0037] According to exemplary embodiments, the insulation layer etchant composition may be effectively utilized in a selective etching process for a silicon nitride layer while preventing the silicon oxide layer from being etched.

BRIEF DESCRIPTION OF THE DRAWINGS

[0038] FIGS. 1 to 3 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments; and

5 **[0039]** FIGS. 4 to 6 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0040] According to exemplary embodiments, an insulation layer etchant composition
10 including phosphoric acid and a multi-podal silane compound and having a high etching selectivity for a nitride layer relative to an oxide layer is provided. A method of forming patterns using the insulation layer etchant composition is also provided.

[0041] Hereinafter, the present invention will be described in detail with reference to the accompanying drawings. However, those skilled in the art will appreciate that
15 such embodiments described with reference to the accompanying drawings are provided to further understand the spirit of the present invention and do not limit subject matters to be protected as disclosed in the detailed description and appended claims.

[0042] <Insulation Layer Etchant Composition>

[0043] According to exemplary embodiments, an insulation layer etchant composition
20 may include phosphoric acid, a multi-podal silane compound and a remainder of water.

[0044] The insulation layer etchant composition may be provided on a structure including an oxide layer (e.g., a silicon oxide layer) and a nitride layer (e.g., a silicon nitride layer) to etch the nitride layer with a high etching selectivity without damaging the oxide layer.

[0045] For example, the insulation layer etchant composition may be used to selectively etch the silicon nitride layer in a fabrication of a semiconductor device.

[0046] Phosphoric acid may be represented by, e.g., a chemical formula H_3PO_4 , and may serve as a main etching ingredient for etching the nitride layer. In exemplary
5 embodiments, an amount of phosphoric acid may be in a range from about 80 weight percent (wt%) to about 95 wt% based on a total weight of the insulation layer etchant composition.

[0047] If the amount of phosphoric acid may be less than about 80 wt%, an overall etching rate may be degraded. If the amount of phosphoric acid may exceed about 95
10 wt%, an etching rate for the oxide layer or a conductive layer such as a metal layer may be also increased together with an etching rate for the nitride layer to reduce an etching selectivity for the nitride layer.

[0048] Preferably, the amount of phosphoric acid may be controlled within a range from about 80 wt% to about 90 wt% in consideration of the etching rate and the etching
15 selectivity.

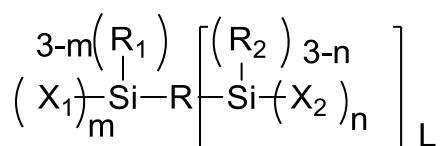
[0049] The multi-podal silane compound may indicate a compound in which a plurality of silane groups may be combined in a single molecule. In exemplary
embodiments, a di-podal compound in which two silane groups are combined in a single molecule, and/or a tri-podal silane compound in which three silane groups are
20 combined in a single molecule may be used.

[0050] The silane groups may include a silicon atom and, e.g., three passivation groups combined thereto. The passivation group may include, e.g., an alkoxy group, a halogen atom or a phosphate group ($-OP_3H_2$), and may be adsorbed on or chemically
interacted with a surface of the silicon oxide layer to form a passivation layer. The

multi-podal silane compound may include a plurality of the silane groups so that the number of the passivation groups may be increased to, e.g., 6 or 9, etc. Thus, a passivation effect with respect to a surface of the oxide layer such as the silicon oxide layer may be amplified.

- 5 **[0051]** In exemplary embodiments, the silane groups included in the multi-podal silane compound may be connected to each other via a linker group including at least one carbon compound. For example, in the multi-silane compound according to exemplary embodiments, a structure in which the silane groups are directly connected or connected via only an oxygen atom (-Si-O-Si) may be excluded.
- 10 **[0052]** In exemplary embodiments, the multi-podal silane compound may include a compound represented by Chemical Formula 1 below.

[0053] [Chemical Formula 1]



- [0054]** In the Chemical Formula 1 above, R represents the linker group, and may be a
 15 divalent organic group including at least one carbon atom. R₁ and R₂ may each independently represent a C1 to C12 alkyl group or a C6 to C12 aryl group.

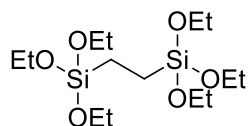
[0055] X₁ and X₂ may each independently represent halogen, -OR₃ group or a phosphate group, and R₃ may represent a C1 to C10 alkyl group capable of including an ether bond or a C6 to C12 aryl group.

- 20 **[0056]** L may be an integer of 1 or 2, and m and n may each be independently an integer of 1 to 3.

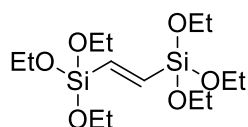
[0057] In some embodiments, the multi-podal compound may include at least one of

the di-podal silane compounds represented by Chemical Formulae 2-1 to 2-7 below.

[0058] [Chemical Formula 2-1]

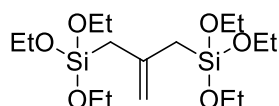


[0059] [Chemical Formula 2-2]

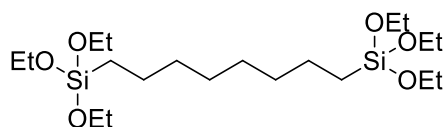


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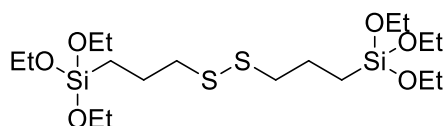
[0060] [Chemical Formula 2-3]



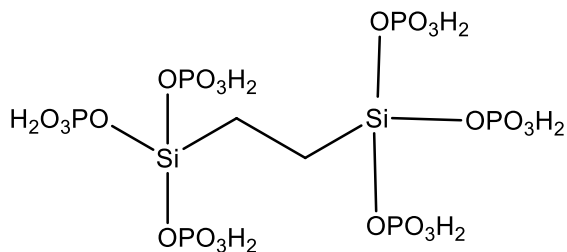
[0061] [Chemical Formula 2-4]



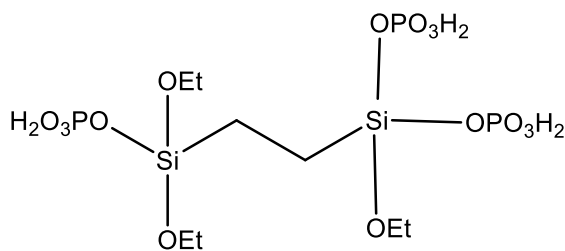
10 **[0062]** [Chemical Formula 2-5]



[0063] [Chemical Formula 2-6]



[0064] [Chemical Formula 2-7]



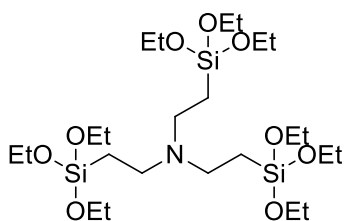
[0065] The linker group in the tri-podal silane compound may include a linker center for combining three silane groups. Three bonding sites may be diverged from the linker center such that the three silane groups may be combined.

- 5 **[0066]** In some embodiments, the linker center may include a nitrogen atom. In this case, solubility or compatibility of the tri-podal silane compound with respect to phosphoric acid may be improved.

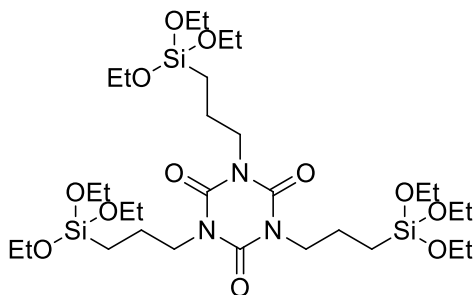
[0067] For example, the multi-podal silane compound may include at least one of the tri-podal silane compounds represented by Chemical Formula 3-1 or Chemical Formula

10 3-2 below.

[0068] [Chemical Formula 3-1]



[0069] [Chemical Formula 3-2]



- 15 **[0070]** In the insulation layer etchant composition according to exemplary

embodiments as described above, the silane groups including a plurality of the passivation groups may be isolated from each other by the linker group in a single molecule. Thus, a coverage of the silane groups which may be combined with or adsorbed on a surface of the oxide layer may be increased. Additionally, a chelating
5 effect may be provided by the linker group so that a passivation effect for the oxide layer may be effectively implemented.

[0071] The linker group may have an organic-based structure, and thus may block a permeation of phosphoric acid that is an inorganic acid so that the oxide layer may be additionally protected.

10 **[0072]** In a comparative example, a siloxane compound may be employed for protecting the oxide layer. In the siloxane compound, silicon atom neighboring each other may be directly combined via an oxygen atom (-Si-O-Si-). Thus, a distance between the neighboring silicon atoms is excessively small, and thus the chelating effect and coverage increase by the multi-podal silane compound according to exemplary
15 embodiments may not be substantially realized.

[0073] Further, the siloxane compound may have a structure similar to that of silicon oxide, and thus may be dissociated by phosphoric acid together with the silicon oxide layer. For example, the siloxane compound may be dissociated in an etching process at a high temperature of 150 °C or more, and thus an initial etching capability may not
20 be constantly maintained.

[0074] However, according to exemplary embodiments, the multi-podal silane compound including the linker group may be used instead of the siloxane compound. Accordingly, the passivation effect for the oxide layer may be amplified, and uniform etching property (e.g., the etching rate) may be maintained for a long period.

[0075] In some embodiments, a fluorine ion generating species (e.g., a fluoride or a fluorine ion salt such as ammonium fluoride) may be excluded from the insulation layer etchant composition. Accordingly, etching damages of the oxide layer by a fluorine ion may be avoided.

5 **[0076]** In some embodiments, the insulation layer etchant composition may not include an ingredient such as an oxime-based compound which may generate residues on an etching object. Accordingly, the silicon oxide layer may be protected by the multi-podal silane compound, and an etching efficiency for the silicon nitride layer may be enhanced by phosphoric acid.

10 **[0077]** In some embodiments, the insulation layer etchant composition may include the multi-podal silane compound in an amount ranging from about 0.0001 wt% to about 1 wt% based on a total amount of the composition. If the amount of the multi-podal silane compound is less than about 0.0001 wt%, an oxide layer passivation may not be substantially realized. If the amount of the multi-podal silane compound exceeds
15 about 1 wt%, an etching capability from phosphoric acid may be deteriorated.

[0078] Preferably, the amount of the multi-podal silane compound may be controlled within a range from about 0.001 wt% to about 0.1 wt% based on the total amount of the composition in a consideration of the oxide layer passivation and the etching rate.

[0079] The insulation layer etchant composition may include a remainder of water (e.g.,
20 deionized water). For example, phosphoric acid may be provided as an aqueous solution (e.g., 85% phosphoric acid), and the multi-podal silane compound may be included in the amount range as described above based on 100 parts by weight of the phosphoric acid aqueous solution.

[0080] In some embodiments, the insulation layer etchant composition may consist

essentially of the phosphoric acid, the multi-podal silane compound and a remainder of water. In some embodiments, the insulation layer etchant composition may further include an additive such as an etching enhancer without degrading the passivation effect of the multi-podal silane compound and the etching efficiency of phosphoric acid.

5 **[0081]** <Method of Forming Pattern >

[0082] FIGS. 1 to 3 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments.

[0083] Referring to FIG. 1, an oxide layer 110 and a nitride layer 120 may be formed on a substrate 100.

10 **[0084]** The substrate 100 may include a semiconductor material such as single crystalline silicon, single crystalline germanium, etc., or may include polysilicon.

[0085] In exemplary embodiments, the oxide layer 110 may be formed of silicon oxide. The oxide layer 110 may be formed by a chemical vapor deposition (CVD) process, a sputtering process, a physical vapor deposition (PVD) process, an atomic layer
15 deposition (ALD) process, etc.

[0086] The nitride layer 120 may be formed on the oxide layer 110. In exemplary embodiments, the nitride layer 120 may be formed of silicon nitride by a CVD process, a PVD process, a sputtering process, an ALD process, etc.

[0087] Referring to FIG. 2, a photoresist pattern 130 may be formed on the nitride
20 layer 120. For example, a photoresist layer may be formed on the nitride layer 120, and a portion of the photoresist layer may be removed by a selective exposure process and a developing process.

[0088] Accordingly, the photoresist pattern 130 partially exposing a top surface of the nitride layer 120 may be formed.

[0089] Referring to FIG. 3, a wet etching process may be performed using the insulation layer etchant composition according to exemplary embodiments and using the photoresist pattern 130 as an etching mask.

[0090] Accordingly, an exposed portion of the nitride layer 120 may be removed to form a nitride pattern 125. As described above, the insulation layer etchant composition according to exemplary embodiments may provide remarkably improved oxide passivation by the multi-podal silane compound. Thus, a surface of the oxide layer 110 may not be substantially etched or damaged, and the nitride layer 120 may be selectively etched.

[0091] For an etching efficiency, the insulation etchant composition may be heated to about 150 °C or more. The multi-podal silane compound may be stable even at a high temperature, and thus an initial etching rate and passivation may be uniformly maintained.

[0092] The photoresist pattern 130 may be removed after the etching process by a strip process and/or an ashing process.

[0093] As illustrated in FIGS. 1 to 3, the nitride layer 120 may be partially removed. Alternatively, the nitride layer 120 may be wholly removed using the etchant composition. In this case, a top surface of the oxide layer 110 may be entirely protected by the multi-podal silane compound to be prevented from etching damages.

[0094] FIGS. 4 to 6 are schematic cross-sectional views illustrating a method of forming patterns in accordance with exemplary embodiments.

[0095] Referring to FIG. 4, a plurality of oxide layers 210 and nitride layers 220 may be alternately and repeatedly stacked on a substrate 200.

[0096] Referring to FIG. 5, a through pattern 230 penetrating the oxide layers 210 and

the nitride layers 220 may be formed. For example, the oxide layers 210 and the nitride layers 220 may be commonly etched by a dry etching process to form an opening, and a filling material may be formed in the opening to form the through pattern 230. The through pattern 230 may be formed of a semiconductor material such as polysilicon,
5 or a conductive material such as a metal.

[0097] Referring to FIG. 6, the nitride layers 220 may be selectively removed using the etchant composition according to exemplary embodiments as described above.

[0098] Accordingly, the oxide layers 210 may remain on a sidewall of the through pattern 230, and gaps 240 may be defined by spaces from which the nitride layers 220
10 are removed. A conductive layer such as a metal layer may be formed in the gaps 240. The oxide layers 210 may be protected by the multi-podal silane compound during the etching process from etching damages.

[0099] The methods of forming patterns as described above are provided as exemplary implementations, and the insulation layer etchant composition may be also employed to
15 form various insulation structure included in a semiconductor device or a display device (e.g., a gate insulation layer, a barrier layer, an isolation layer, etc.).

[00100] Hereinafter, preferred embodiments will be described to more concretely understand the present invention with reference to examples. However, it will be apparent to those skilled in the art that such embodiments are provided for illustrative
20 purposes and various modifications and alterations may be possible without departing from the scope and spirit of the present invention, and such modifications and alterations are duly included in the present invention as defined by the appended claims.

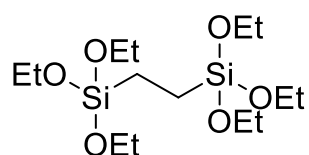
[00101] Examples and Comparative Examples

[00102] 0.1 part by weight of multi-podal silane compounds as listed below was

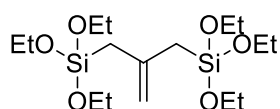
mixed in 100 parts by weight of 85% phosphoric acid aqueous solution to form etchant compositions of Examples.

[00103] In the chemical formulae below, “Et” designates an ethyl group, and “Me” designates a methyl group.

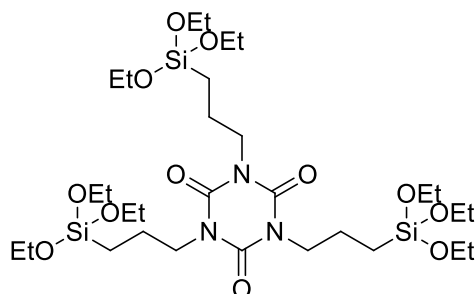
5 **[00104]** 1) Example 1



[00105] 2) Example 2

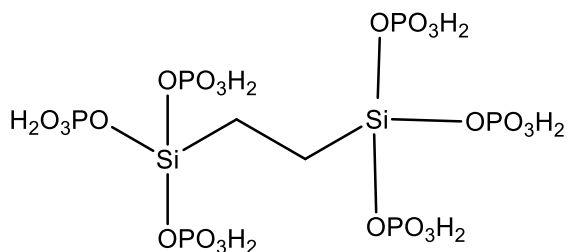


[00106] 3) Example 3

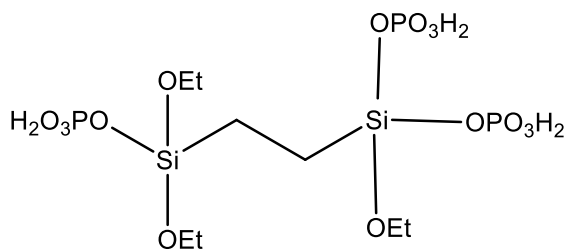


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[00107] 4) Example 4

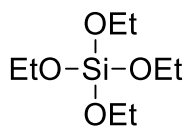


[00108] 5) Example 5

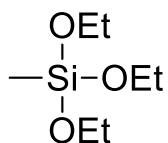


[00109] 0.1 part by weight of silicon-based compounds as listed below was mixed in 100 parts by weight of 85% phosphoric acid aqueous solution to form etchant compositions of Comparative Examples.

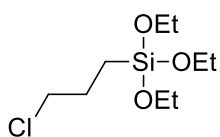
5 **[00110]** 1) Comparative Example 1



[00111] 2) Comparative Example 2

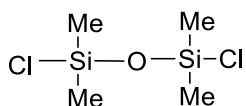


[00112] 3) Comparative Example 3



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[00113] 4) Comparative Example 4



[00114] Experimental Example

[00115] (1) Measuring etching rate (E/R) of silicon nitride (SiN) layer

15 **[00116]** A wafer including a silicon nitride (SiN) layer having a thickness of 5,000 Å

thereon was cut to form a sample having a dimension 2*2cm². The sample was immersed in the compositions of Examples and Comparative Examples at 160 °C for 3 minutes. After the immersion, the sample was washed by a deionized water (DIW) and dried. After the drying, a thickness of the sample was measured using a scanning
 5 electron microscope (SEM) to measure an etching rate (Å/min).

[00117] (2) Measuring etching rate of silicon oxide (SiO₂) layer

[00118] A wafer including a silicon oxide (SiO₂) layer having a thickness of 400 Å was cut to form a sample having a dimension 2*2cm². The sample was immersed in the compositions of Examples and Comparative Examples at 160 °C for 3 minutes.
 10 After the immersion, the sample was washed by a deionized water (DIW) and dried. After the drying, a thickness of the sample was measured using Ellipsometer to measure an etching rate (Å/min).

[00119] The results are shown in Table 1 below.

[00120] [Table 1]

	SiN E/R (Å/min) (A)	SiO ₂ E/R (Å/min) (B)	Etching Selectivity
Example 1	110	0.1 or less	1100 or more
Example 2	107	0.1 or less	1070 or more
Example 3	108	0.1 or less	1080 or more
Example 4	113	0.1 or less	1130 or more
Example 5	110	0.1 or less	1100 or more
Comparative Example 1	109	3.2	34
Comparative Example 2	112	3.1	36
Comparative Example 3	107	3.4	31
Comparative Example 4	112	3.7	30

[00121] Referring to Table 1 above, the compositions of Examples including the multi-podal silane compound showed improved passivation effect for the oxide layer compared to that in the compositions of Comparative Examples, and the etching selectivity for the nitride layer greater than about 1000 was achieved.

What is claimed is:

1. An insulation layer etchant composition, comprising:
phosphoric acid;

5 a multi-podal silane compound in which a plurality of silane groups are
combined with each other via a linker group including at least one carbon atom; and
a remainder of water.

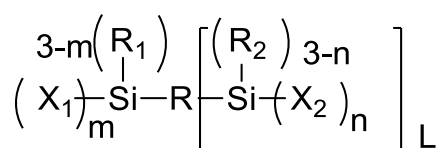
2. The insulation layer etchant composition according to claim 1, wherein
10 each of the silane groups included in the multi-podal silane compound includes a
plurality of passivation groups.

3. The insulation layer etchant composition according to claim 2, wherein
the passivation group includes an alkoxy group, halogen or a phosphate group.

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4. The insulation layer etchant composition according to claim 1, wherein
the multi-podal silane compound includes a compound represented by Chemical
Formula 1 below:

[Chemical Formula 1]



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wherein, in the Chemical Formula 1 above, R represents the linker group, and
is a divalent organic group including at least one carbon atom,

R₁ and R₂ are each independently a C1 to C12 alkyl group or a C6 to C12 aryl group,

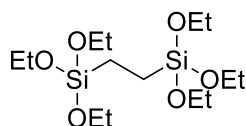
X₁ and X₂ are each independently halogen, –OR₃ group or a phosphate group,

R₃ is a C1 to C10 alkyl group capable of including an ether bond, or a C6 to C12 aryl group,

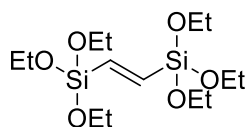
L is an integer of 1 or 2, and m and n are each independently an integer of 1 to 3.

5. The insulation layer etchant composition according to claim 4, wherein the multi-podal silane compound includes at least one selected from a group consisting of di-podal silane compounds represented by Chemical Formulae 2-1 to 2-7 below:

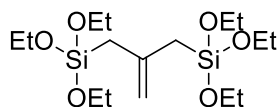
[Chemical Formula 2-1]



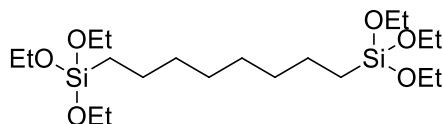
[Chemical Formula 2-2]



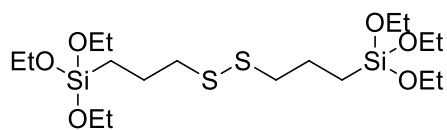
[Chemical Formula 2-3]



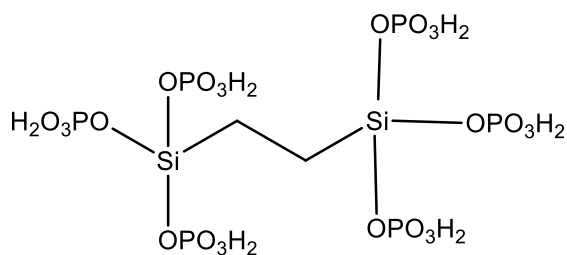
[Chemical Formula 2-4]



[Chemical Formula 2-5]

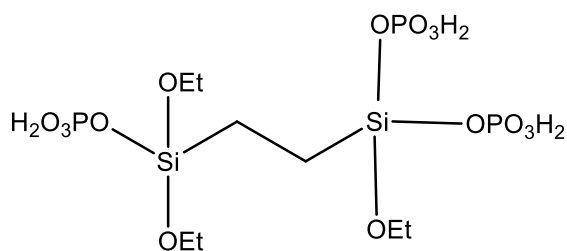


[Chemical Formula 2-6]



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[Chemical Formula 2-7]

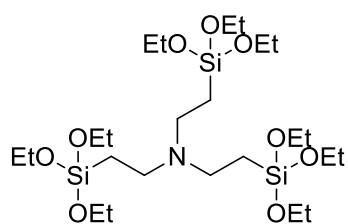


wherein, in the Chemical Formulae 2-1 to 2-7 above, Et represents an ethyl group.

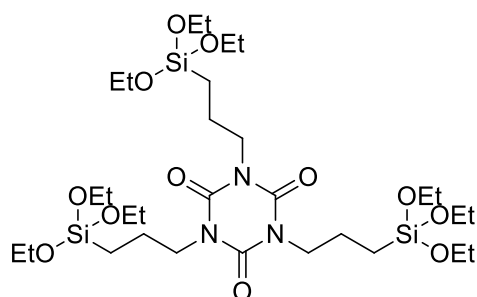
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6. The insulation layer etchant composition according to claim 4, wherein the multi-podal silane compound includes at least one selected from a group consisting of tri-podal silane compounds represented by Chemical Formulae 3-1 and 3-2 below:

[Chemical Formula 3-1]



[Chemical Formula 3-2]



wherein, in the Chemical Formulae 3-1 and 3-2 above, Et represents an ethyl group.

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7. The insulation layer etchant composition according to claim 1, wherein an amount of the multi-podal silane compound is in a range from 0.0001 wt% to 1 wt% based on a total weight of the composition.

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8. The insulation layer etchant composition according to claim 1, wherein a compound including a siloxane bond (-Si-O-Si-) is excluded from the composition.

9. A method of forming patterns, comprising:

forming an oxide layer and a nitride layer on a substrate; and

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selectively etching the nitride layer using the insulation layer etchant composition according to any one of claims 1 to 8.

10. The method according to claim 9, wherein the oxide layer includes a silicon oxide layer and the nitride layer includes a silicon nitride layer.

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