

- 1 -

A COMMON BIAS CIRCUIT FOR A PLURALITY OF DISCRETE
IC'S EACH HAVING THEIR OWN BIAS CIRCUITRY

BACKGROUND

5 For an integrated circuit (IC) to be powered from a single voltage power supply, a bias point is established internal or external to the chip. This may be done inside the IC as, for example, in the TA7630 IC manufactured by the Toshiba Company of Japan. In such a case, the bias voltage is available at a pin of the chip for coupling thereto a large filter
1 0 capacitor since it is not practicable to put large capacitors within the circuit housing. In the alternative, the bias can be established external to the IC by an external resistor divider or zener diode circuits, as with respect to the TA9187 chip also manufactured by the Toshiba Company of Japan. Because of different IC designs, and IC to IC variations and other
1 5 component tolerances, a tolerance in the magnitude of the bias voltage is to be expected. Because of this tolerance in the bias voltage, coupling capacitors are used to block this DC component from coupling between chips to prevent the difference tolerance voltage from being amplified. It is also necessary to filter each bias supply to eliminate crosstalk or
2 0 feedback within the chip.

 It is a common practice in integrated circuits, including integrated circuits having a bias supply generated internal to the IC, for providing bias to individual amplifier portions disposed within the same IC. In such a case, the bias supply and the individual portions within the
2 5 chip are designed to operate with each other without signal coupling capacitors. In such a case, precautions are taken in the design of the chip to assure this compatibility within the chip. This is not the case for whole discrete IC's which can be operated along with other chips of which the IC designer has no control over.

3 0 Some examples of IC's which provide an internal bias to individual portions within the same housing are shown in the RCA Integrated Circuits for Linear Applications Databook, copyrighted 1986 by the RCA Corporation, U.S.A. In particular, the block diagram of the CA3060 Operational Transconductance Amplifier Array shows three operational
3 5 amplifiers with a bias regulator. The circuit for a tri-level comparator circuit shows each of the three operational amplifiers receiving bias from the bias regulator. A similar situation is shown in block diagrams for the CA3401, CA3450, CA3493, and CA5422 integrated circuits, and an applications note for the CA3130, all of which show operational amplifiers

on the same chip receiving bias from a common bias network also on the chip and receiving power from the V+ terminal.

- The present invention recognizes that if all discrete IC's were to operate with the same bias level, e.g. 1/2 of the same supply voltage which is coupled to some or all of the chips in a television receiver or the like, it would be possible to couple the bias/filter points together and force all of the IC's to be coupled to the same bias voltage. This would allow the discrete IC's to have the signal leads DC coupled and to eliminate the AC coupling capacitors otherwise required for coupling signal between chips.
- 1 0 Additionally, the individual bias bypass capacitors required for each IC would not be required. Accordingly, it is desired to be able to eliminate signal coupling capacitors otherwise required between discrete IC's and to eliminate the individual bias bypass capacitors otherwise required for the discrete IC's.
- 1 5 As used herein, the terms discrete IC's and chips is intended to include monolithic circuits as well as non-monolithic circuits such as hybrid IC's and encapsulated modules.

SUMMARY OF THE INVENTION

- 2 0 Briefly, the present invention is directed to a circuit for operating discrete integrated circuits from a common bias source by DC coupling the individual bias circuits of the discrete IC's together to eliminate signal coupling capacitors otherwise required between the discrete IC's and to eliminate the individual bias bypass capacitors
- 2 5 otherwise required for the discrete IC's.

BRIEF DESCRIPTION OF THE DRAWINGS

- Figure 1 shows a block diagram of a prior art bias connection for discrete IC's.
- 3 0 Figure 2 shows a block diagram of the coupling of bias circuits for discrete IC's according to aspects of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

- Referring now to Figure 1, there is shown a block diagram of a
- 3 5 prior art bias circuit configuration. The bias for integrated circuit 10 is generated by external bias generating circuit 12 comprising a resistor 14 coupled to a zener diode 16 with the series circuit coupled between the positive supply voltage Vcc and ground. A capacitor 18 is coupled across zener diode 16 for filtering the bias voltage generated across zener diode

16 with the bias voltage being provided to IC 10 at line 20. In the exemplary embodiment, the bias is $V_{cc}/2$.

IC 22 has its bias generated internally by series resistors 24 and 26 coupled between V_{cc} and ground with the bias being generated at junction 28. For the reasons discussed above, filter capacitor 30 is coupled to the bias node 28 and AC coupling capacitors 32 and 34 are required for coupling the AC signal to chip 22.

Referring now to Figure 2 wherein members common to Figure 1 have been designated like numbers, there is shown a block diagram bias circuit configuration according to the present invention. Junction 28 of IC 22 has been coupled to bias generating circuit 12 as is the bias pin for IC 10. AC signal coupling capacitors 32 and 34 are no longer required and filter capacitor 30 is eliminated as being redundant with capacitor 18. Resistors 36 and 38 substitute for resistor 40 of Figure 1 to couple the bias voltage from bias generating circuit 12 to IC 10 with little or no voltage drop while providing AC isolation so as not to short the AC signal to ground through capacitor 18.

Thus, all of the exemplary IC's operate at the same $V_{cc}/2$ bias supply by coupling the bias/filter points of the discrete IC's together. This allows the effected stages to be DC coupled and individual bias bypass capacitors eliminated. Additionally, since the fractional V_{cc} bias supply acts as an AC signal ground, ground modulation problems between the various IC's is reduced or eliminated. It should be noted that it may be desirable that the common bias generating circuit 12 have a sufficiently low impedance to "swamp out" the generally higher impedance bias generating circuits internal to the IC's.

It should be noted that this approach would also work for other fractional bias points with respect to V_{cc} or ground, e.g., $V_{cc}/3$, if appropriate. It should further be noted for some of the commonly bias coupled IC's, that the bias voltage will not be at exactly the correct fraction of V_{cc} with respect to ground and there may be a slight reduction of dynamic range for the individual IC.

In the exemplary embodiment amplifiers 40 and 42 are LM 324 IC's and, if appropriate, also have their bias circuitry (not shown) common with the other IC's.

CLAIMS:

1. Apparatus comprising:

a first circuit;

a first bias voltage source for deriving a first bias voltage for at least a portion of said first circuit, said first bias voltage being available at
5 a first terminal;

said first circuit and said first bias voltage source being incorporated within an integrated circuit, said first terminal being a terminal of said integrated circuit;

a second circuit separate from said integrated circuit;

10 a second bias voltage source for deriving a second bias voltage for at least a portion of said second circuit, said second bias voltage available at a second terminal; and

means DC coupling said first terminal of said first bias source to said second terminal of said second bias source for equalizing said first and
15 second bias voltages.

2. The apparatus recited in claim 1 further including means for coupling a signal between said portion of said first circuit and said portion of said second circuit without DC isolation.

3. The apparatus recited in claim 1 wherein said first and second
20 bias sources share a single filter circuit.

4. The apparatus recited in claim 1 wherein said first and second bias voltages are at least approximately equal even in the absence of said means DC coupling said first terminal of said first bias source to said second terminal of said second bias source.

25 5. The apparatus recited in Claim 1, wherein said first and second bias voltage sources derive said first and second bias voltages from the same supply voltage.

6. The apparatus recited in Claim 5 wherein said first and second bias voltages are approximately equal to one-half of said supply voltage
30 even in the absence of said means DC coupling said first terminal of said first bias source to said second terminal of said second bias source.

7. Apparatus comprising:

a first circuit;

a first bias voltage source for deriving a first bias voltage for at
35 least a portion of said first circuit; said first bias voltage being available at a first terminal;



said first circuit and said first bias voltage source being incorporated within an integrated circuit; said first terminal being a terminal of said integrated circuit;

a second circuit separate from said integrated circuit;

5 a second bias voltage source for deriving a second bias voltage for at least a portion of said second circuit; said second bias voltage available at a second terminal;

means DC coupling said first terminal of said first bias source to said second terminal of said second bias source for equalizing said first and
10 second bias voltages; and

means for coupling a signal between said portion of said first circuit and said portion of said second circuit without DC isolation.

8. Apparatus comprising:

a first circuit;

15 a first bias voltage source for deriving a first bias voltage for at least a portion of said first circuit, said first bias voltage being available at a first terminal;

said first circuit and said first bias voltage source being incorporated within a first integrated circuit, said first terminal being a
20 terminal of said integrated circuit;

a second circuit separate from said integrated circuit;

a second bias voltage source for deriving a second bias voltage for at least a portion of said second circuit, said second bias voltage available at a second terminal;

25 said second circuit and said second bias voltage source being incorporated within a second integrated circuit, said second terminal being a terminal of said integrated circuit; and

means DC coupling said first terminal of said first bias source to said second terminal of said second bias source for equalizing said first and
30 second bias voltages.

9. The apparatus recited in claim 8 further including means for coupling a signal between said portion of said first circuit and said portion of said second circuit without DC isolation.

10. The apparatus recited in claim 8 wherein said first and
35 second bias sources share a single filter circuit.



11. The apparatus recited in claim 8 wherein said first and second bias voltages are at least approximately equal even in the absence of said means DC coupling said first terminal of said first bias source to said second terminal of said second bias source.

5 12. The apparatus recited in Claim 8, wherein said first and second bias voltage sources derive said first and second bias voltages from the same supply voltage.

10 13. The apparatus recited in Claim 12, wherein said first and second bias voltages are approximately equal to one-half of said supply voltage even in the absence of said means DC coupling said first terminal of said first bias source to said second terminal of said second bias source.

14. Apparatus comprising:

a first circuit;

15 a first bias voltage source for deriving a first bias voltage for at least a portion of said first circuit;

said first bias voltage being available at a first terminal; said first circuit and said said first bias voltage source being incorporated within a first integrated circuit; said first terminal being a terminal of said integrated circuit;

20 a second circuit separate from said integrated circuit;

a second bias voltage source for deriving a second bias voltage for at least a portion of said second circuit; said second bias voltage available at a second terminal;

25 said second circuit and said second bias voltage source being incorporated within a second integrated circuit, said second terminal being a terminal of said integrated circuit;

means DC coupling said first terminal of said first bias source to said second terminal of said second bias source for equalizing said first and second bias voltages; and

30 means for coupling a signal between said portion of said first circuit and said portion of said second circuit without DC isolation.

15. A circuit substantially as hereinbefore described with reference to Figure 2 of the drawings.



* C L M S *