



DYNAMIC CMOS CIRCUITS WITH NOISE IMMUNITY

ABSTRACT

Dynamic CMOS circuits are provided with improved noise immunity. These circuits comprise first and second stacked NFET devices (12, 14) connected respectively between ground and a first node. An input node is coupled to the first NFET device (12) closest to ground and a clock node coupled to the second NFET device (14) closest to the first node. A PFET device (36) is connected between the input node and a node (38) formed by the stacked NFET devices (12, 14). The first NFET device (12) and the PFET device (36) form an inverter for receiving an input signal (IN), the switch point of the inverter being adjustable by adjusting the PFET/NFET ratio of the inverter, thereby increasing the noise immunity of the circuit.

Figure 2