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FIG. 1

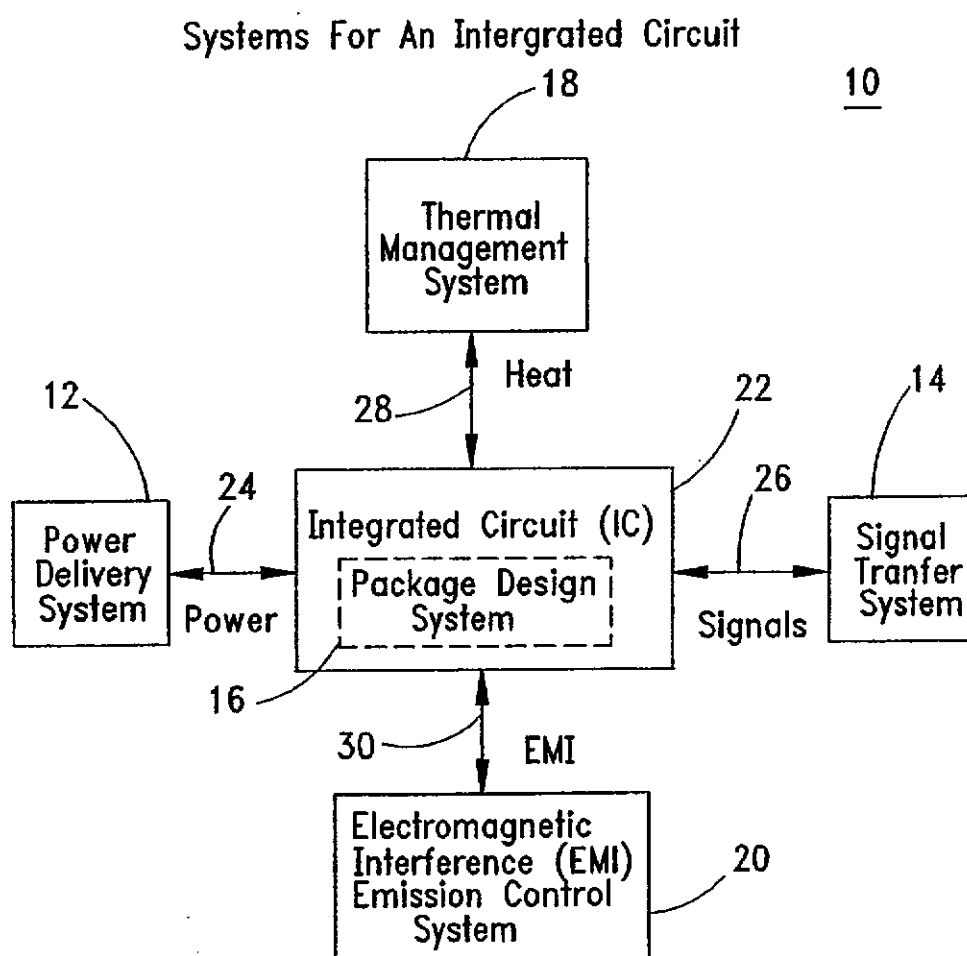


FIG. 2

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Power Delivery System And Signal Transfer For An Integrated Circuit

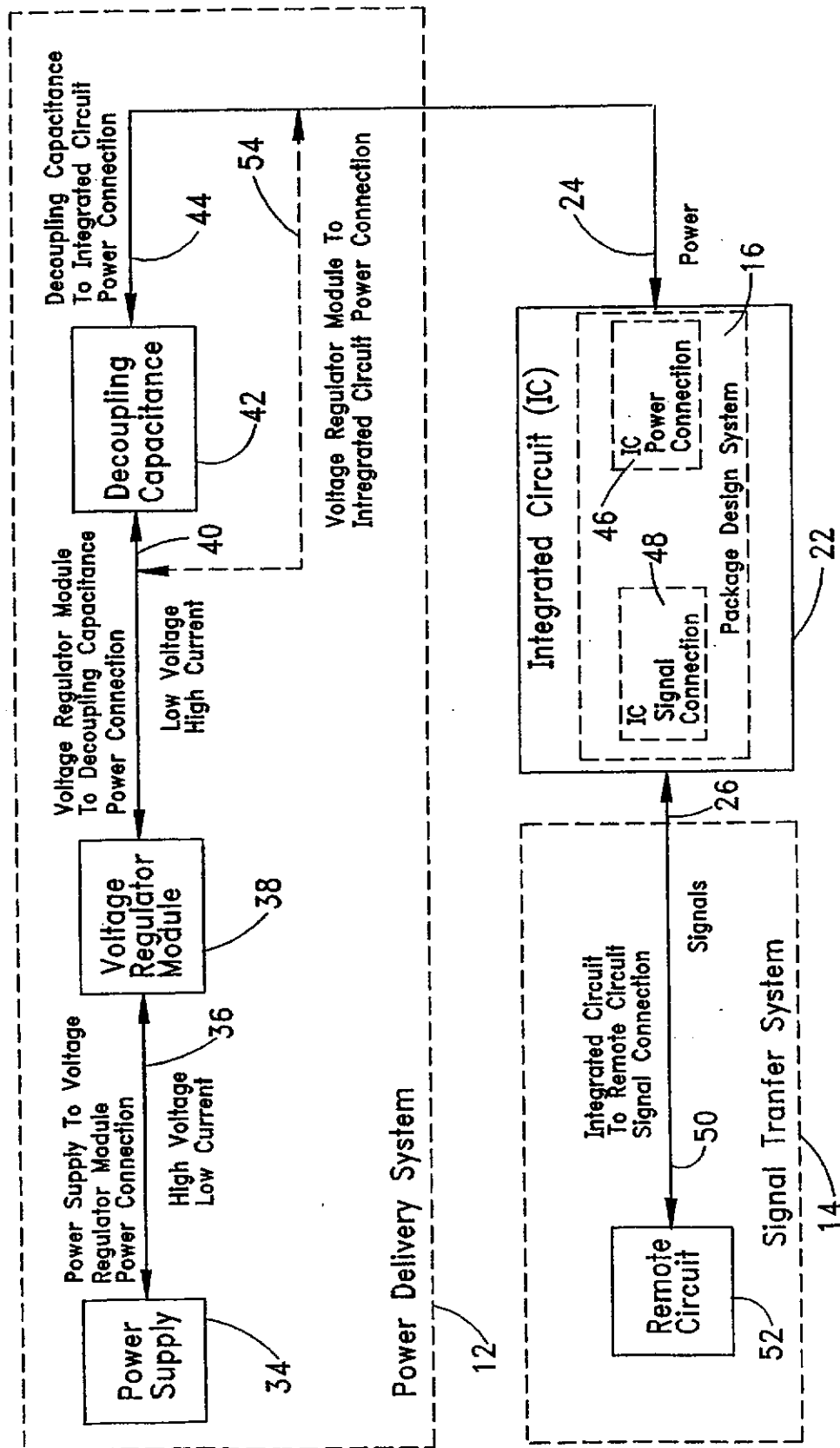


FIG. 3

Table Listing Alternative Locations For Each Block Shown In FIG.2
And Alternative Connections Between The Blocks Shown In FIG.2

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	(34)	36	(38)	40	(42)	44	(46)	(22)	(48)	50	(52)
	A	B	C	D	E	F	G	H	I	J	K
1	Power Supply Location	Power Supply To Voltage Regulator Module Power Connection	Voltage Regulator Module Location	Voltage Regulator Module To Decoupling Capacitance Power Connection	Decoupling Capacitance Location	Decoupling Capacitance to IC Power Connection	IC Power Connection Location	Integrated Circuit(IC) Location	IC Signal Connection Location	IC to Remote Circuit Signal Connection	Remote Circuit Location
2	Remote	Conductor	Connector	Conductor	Connector	Conductor	Top of IC	Connector	Top of IC	Conductor	Connector
3		PCB Trace	PCB	PCB Trace	PCB	PCB Trace	Side of IC	PCB	Side of IC	PCB Trace	PCB
4			Conductor		Conductor		Bottom of IC	Conductor	Bottom of IC		Conductor

FIGS. 4A-4E Integrated Circuit, As Shown in Figs. 1, 2, 3A and 3B, Having Various Levels Of Integration (0-4)

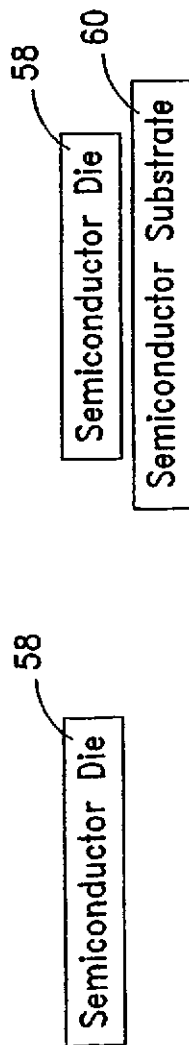


FIG. 4A (Level 0)

FIG. 4B (Level 1)

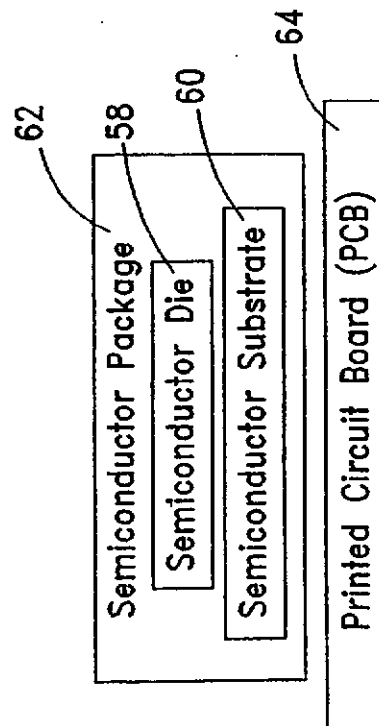


FIG. 4D (Level 3)

FIG. 4E (Level 4)

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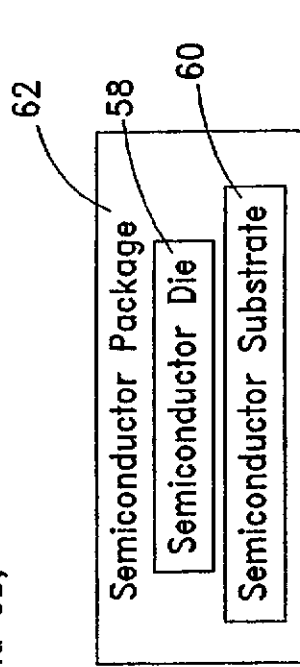
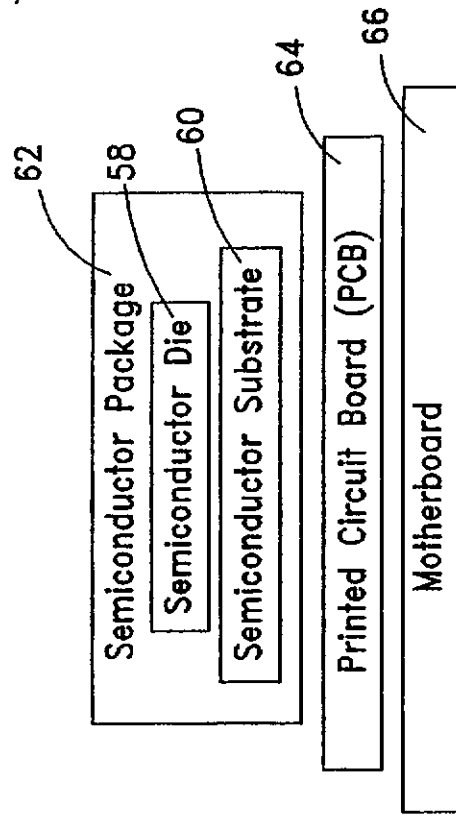
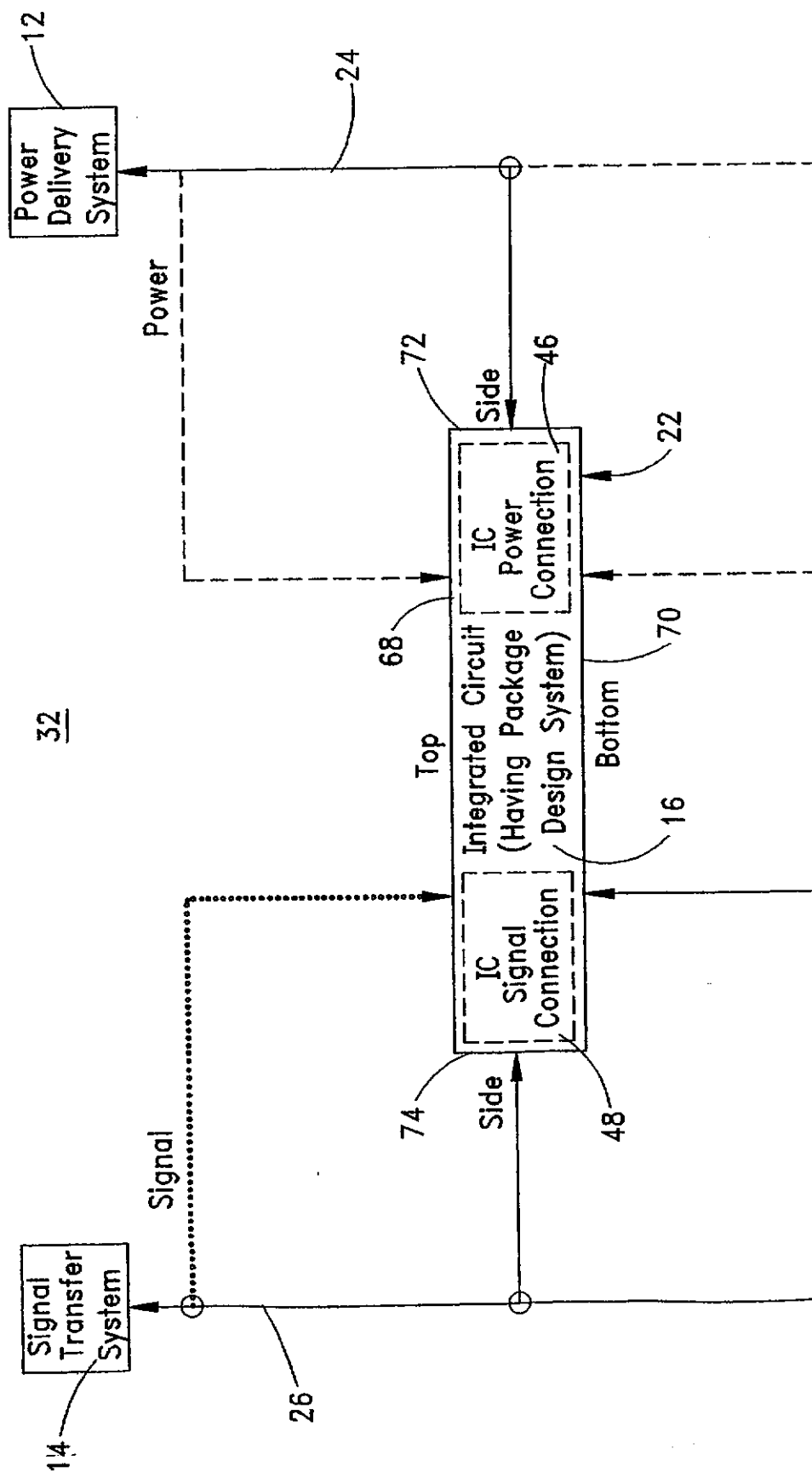


FIG. 4C (Level 2)



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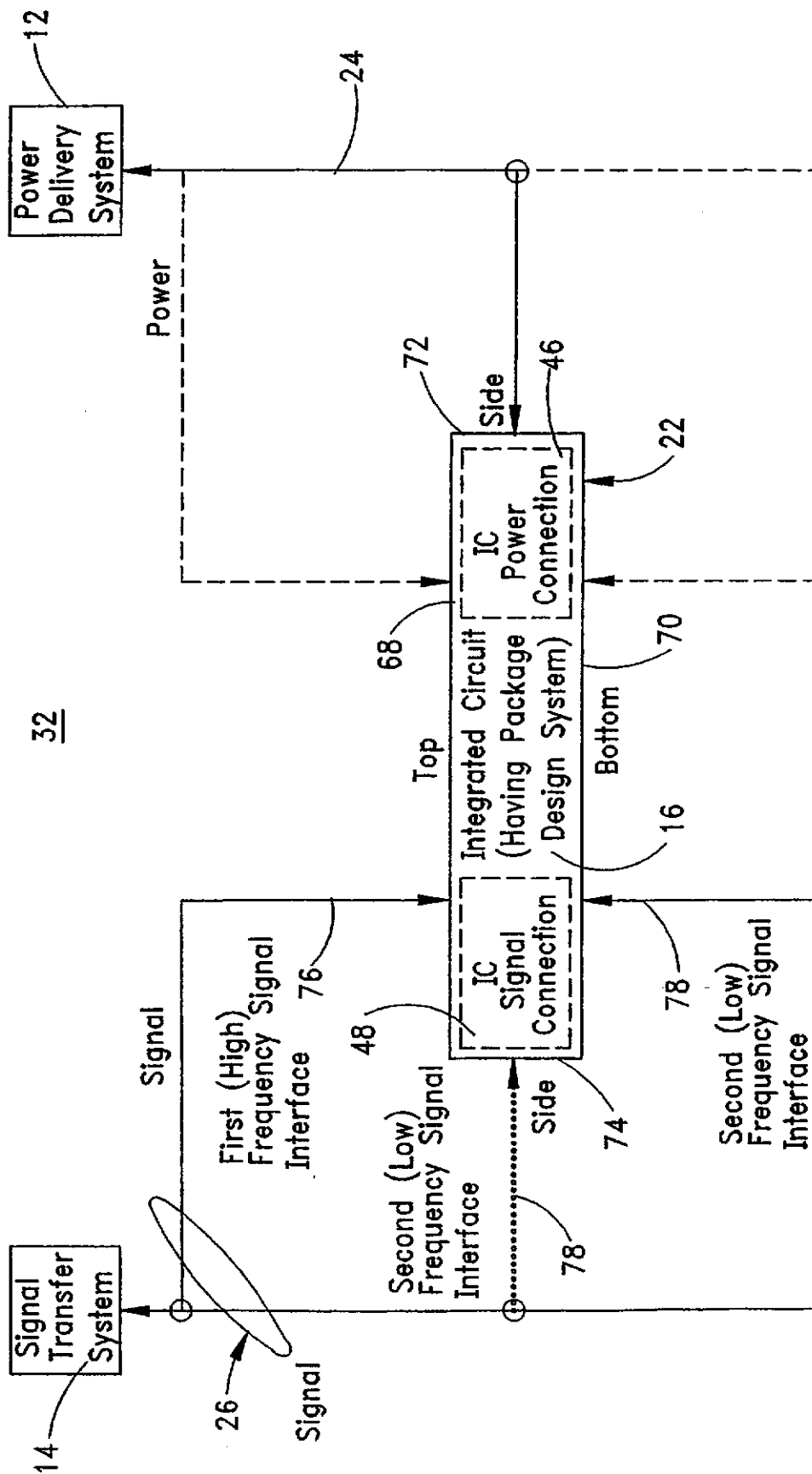
FIG. 5 Integrated Circuit, As Shown in FIGS. 4A-4E, Having Top, Bottom, And/or Side Signal And/or Power Connection Locations



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FIG. 6A

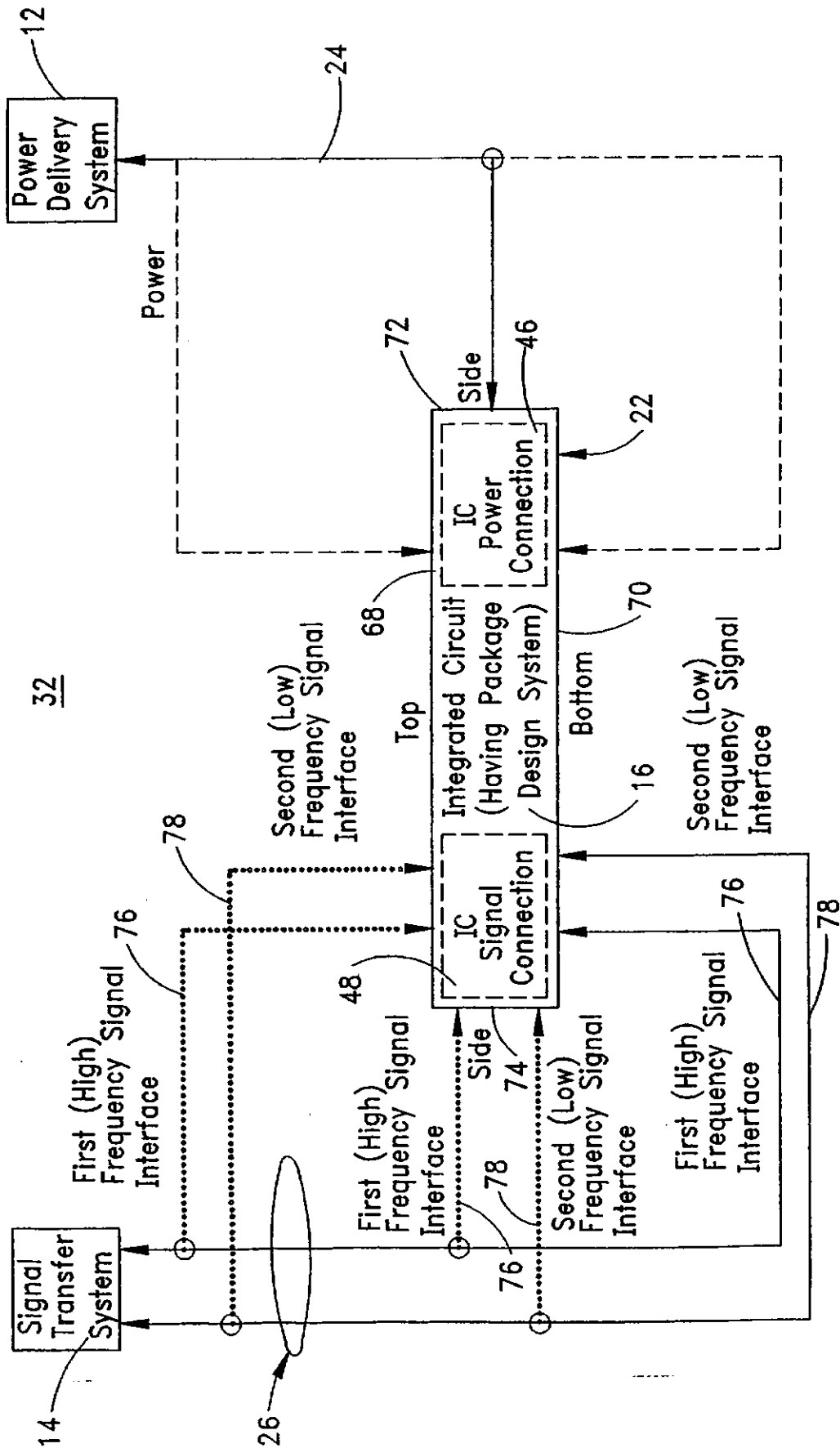
Integrated Circuit, As Shown in FIG. 5, Having A First (High) Frequency Signal Interface And A Second (Low) Frequency Signal Interface, Different From The First Frequency Signal Interface, Each Coupled To Different Sides Of The Integrated Circuit



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FIG. 6B

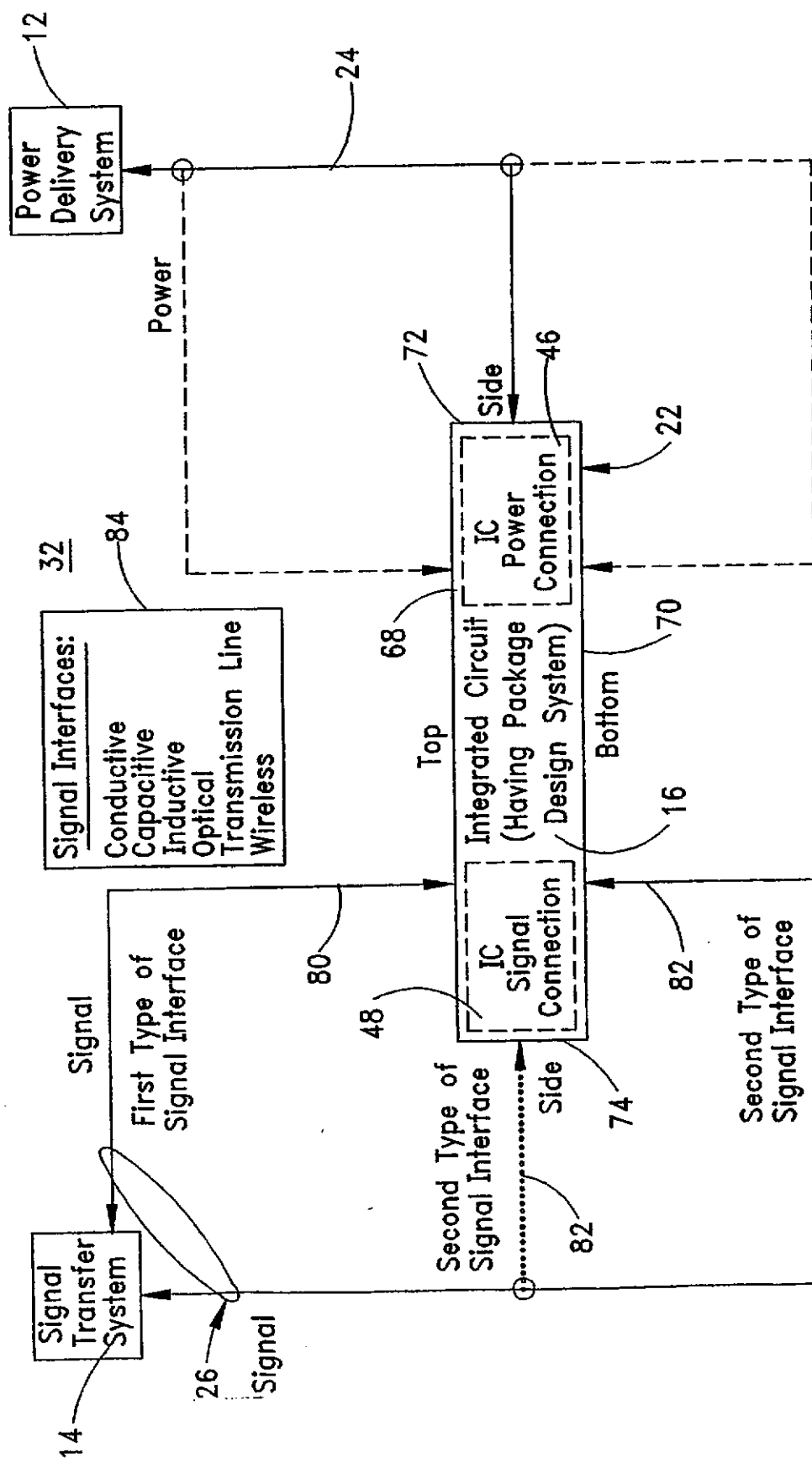
Integrated Circuit, As Shown in FIG. 5, Having A First (High) Frequency Signal Interface And A Second (Low) Frequency Signal Interface, Different From The First Frequency Signal Interface, Each Coupled To The Same Side Of The Integrated Circuit



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FIG. 7A

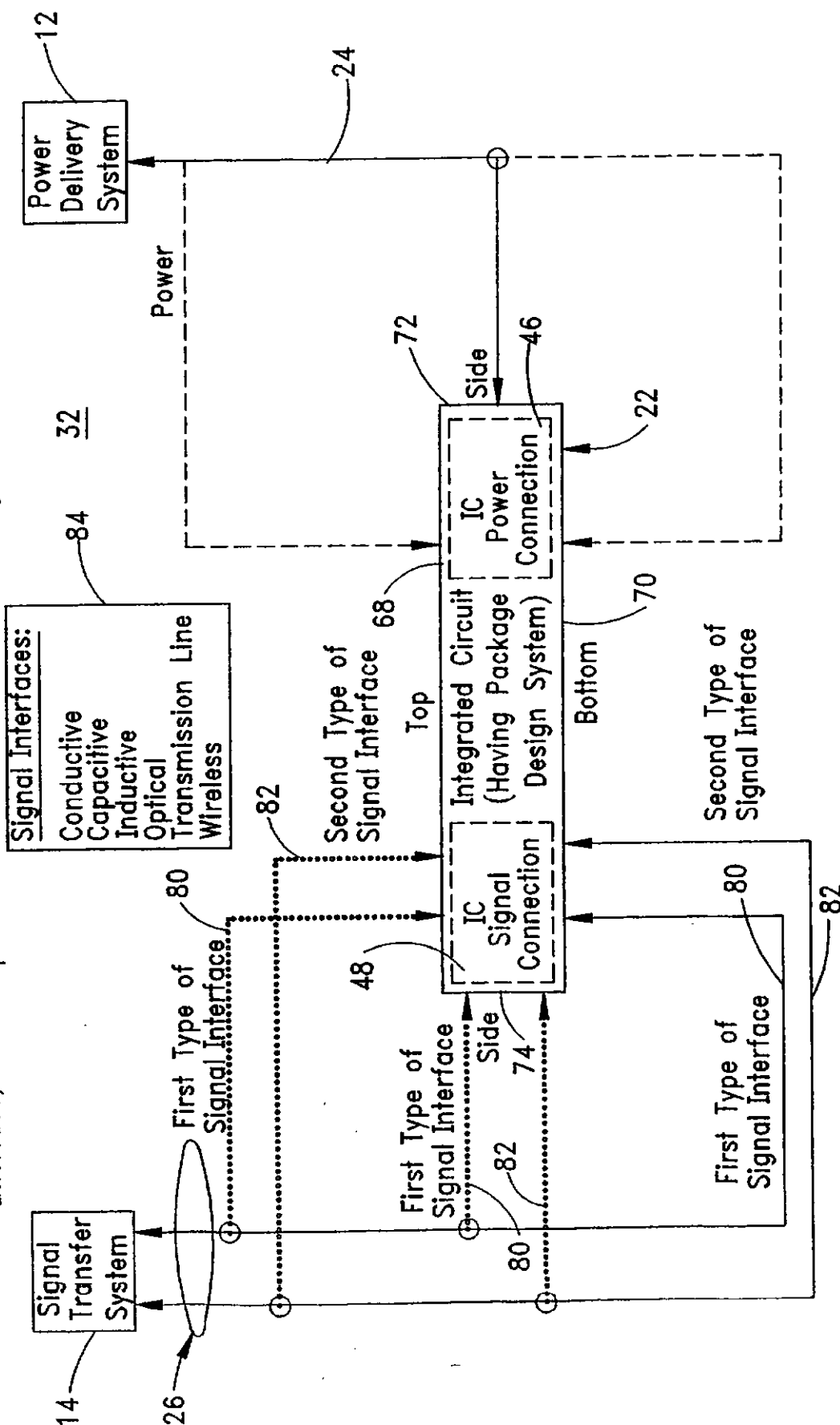
Integrated Circuit, As Shown in FIG. 5, Having A First Type Of Signal Interface And A Second Type Of Signal Interface, Different From the First Type Of Signal Interface, Each Coupled To Different Sides Of The Integrated Circuit



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FIG. 7B

Integrated Circuit, As Shown in FIG. 5, Having A First Type Of Signal Interface And A Second Type Of Signal Interface, Different From the First Type Of Signal Interface, Each Coupled To Different Sides Of The Integrated Circuit



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FIGS.8A and 8B Integrated Circuit,As Shown in FIGS.4C and 5, Having Signal And/Or Power Connections Located Outside and Flush With,Respectively,the Semiconductor Package

FIG.8A

(Outside)
22

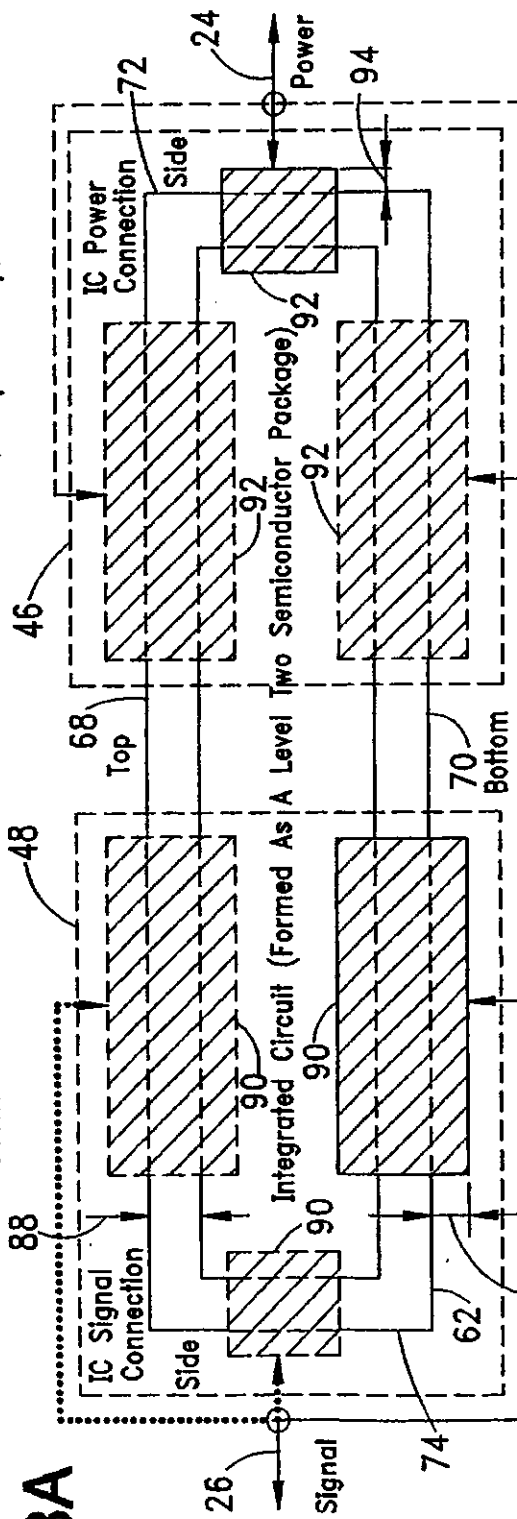
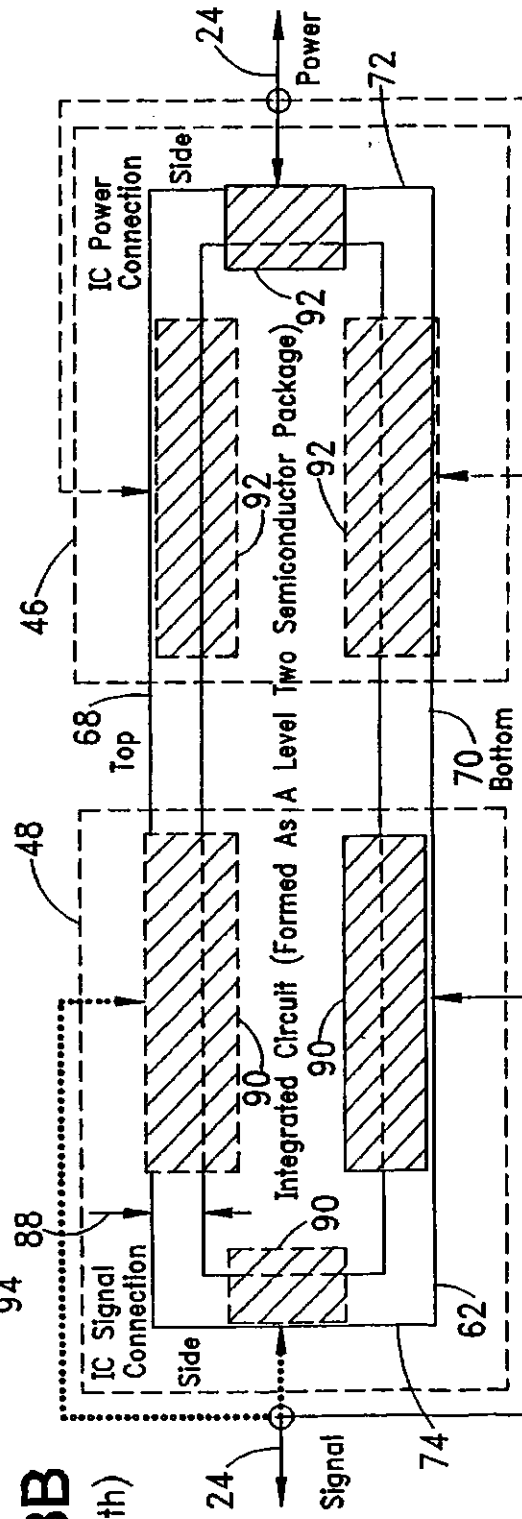


FIG.8B

(Flush With)
22



FIGS. 8C and 8D

Integrated Circuit,As Shown in FIGS.4C and 5, Having Signal And/Or Power Connections Located Recessed and Inside, Respectively,the Semiconductor Package

FIG. 8C

(Recessed)

22

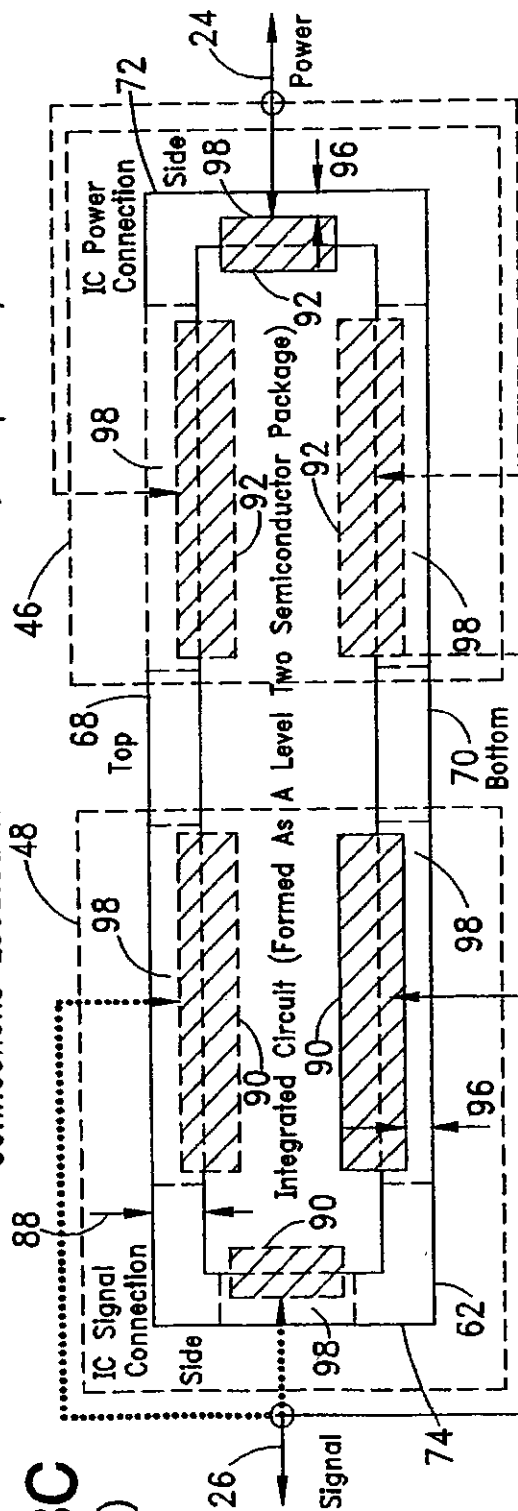
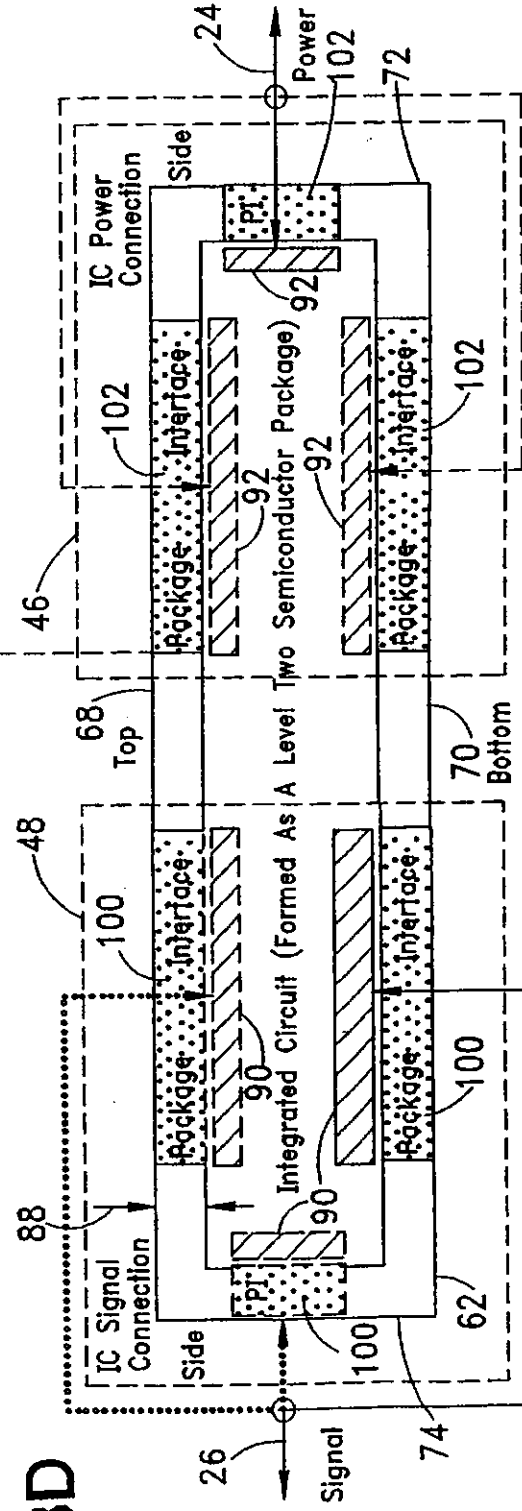


FIG. 8D

(Inside)

22



FIGS. 9A, 9B, 9C

Integrated Circuit, As Shown in FIGS. 4A, 4B, 4C, 4D or 4E and Fig. 5, Having Signal And/or Power Connections Located on the Top, Side And/or Bottom of the Integrated Circuit

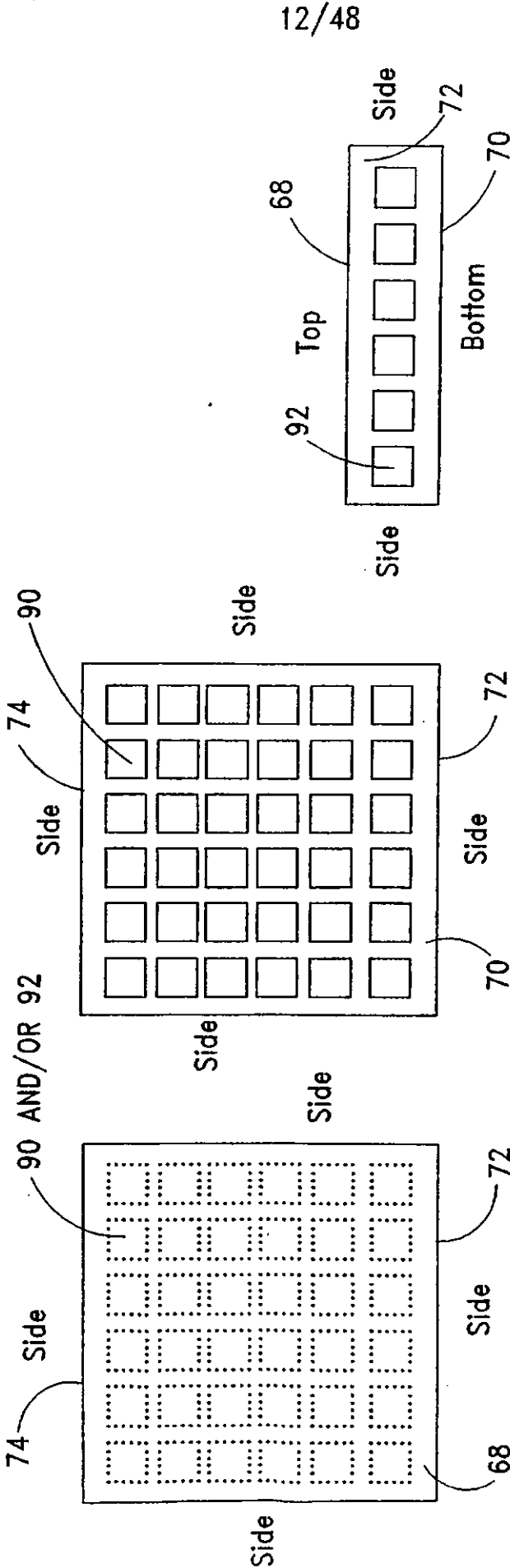


FIG. 9A 22

Top of IC
Alternate Power And/or
Signal Connections

FIG. 9B 22

Bottom of IC
Preferred Signal Connections
With or Without Power Connections

FIG. 9C 22

Side of IC
Preferred Signal Connections
With or Without Power Connections

FIGS.10A,10B,10C

Integrated Circuit,As Shown in FIGS.4A,4B,4C,4D or 4E and Fig.5,Having Signal And/or Power Connections Located on the Top,Side And/or Bottom of the Integrated Circuit

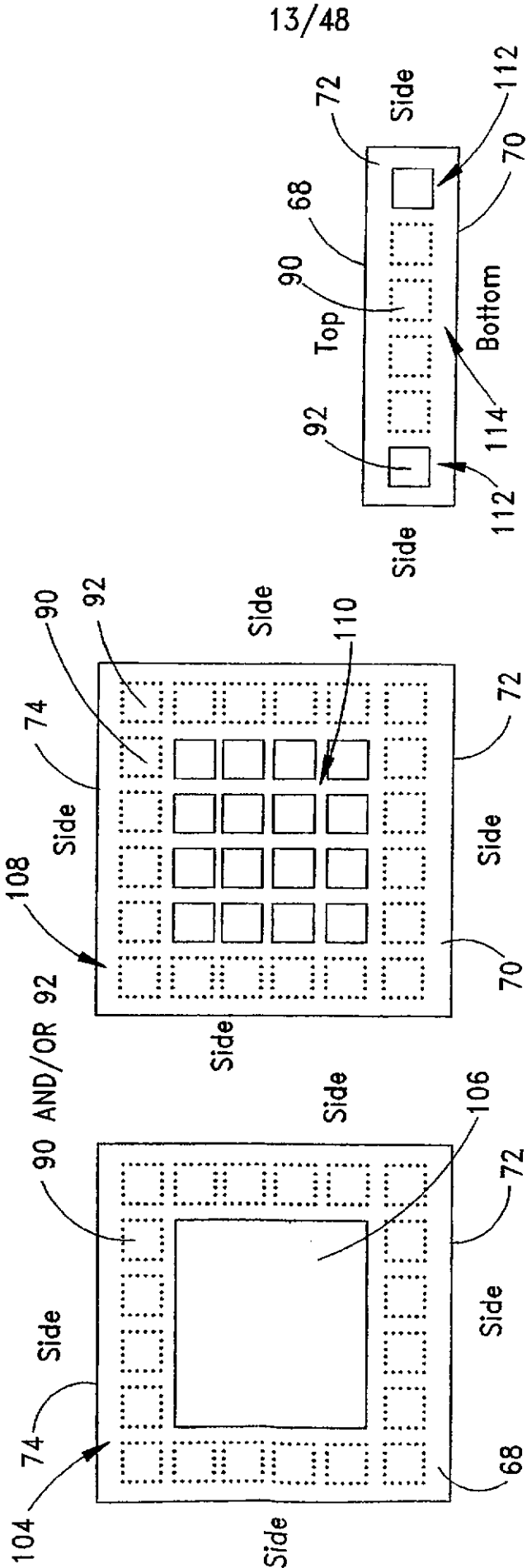


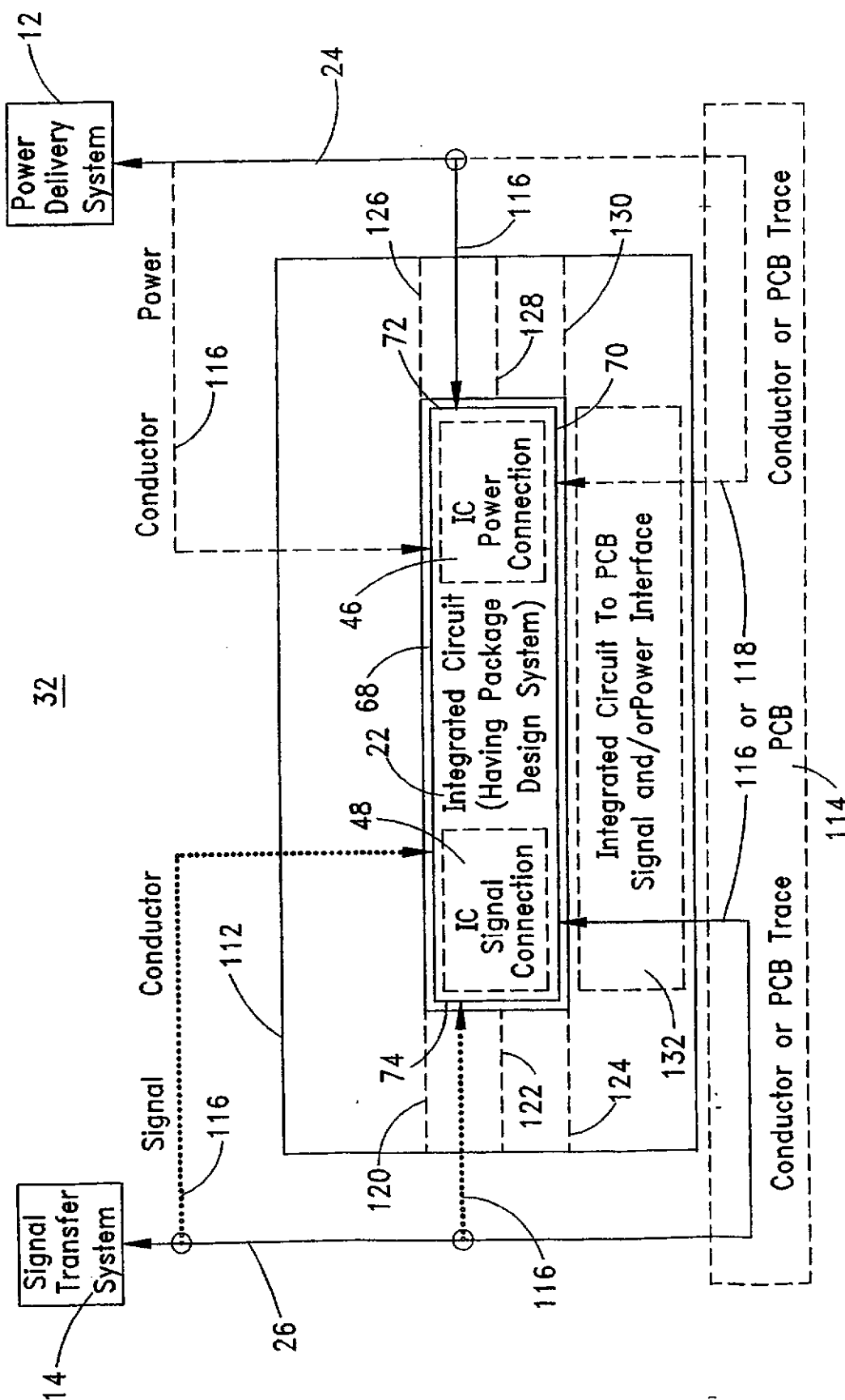
FIG.10A 22
Top of IC
Alternate Power And/or
Signal Connections

FIG.10B 22
Bottom of IC
Preferred Signal Connections
With or Without Power Connections

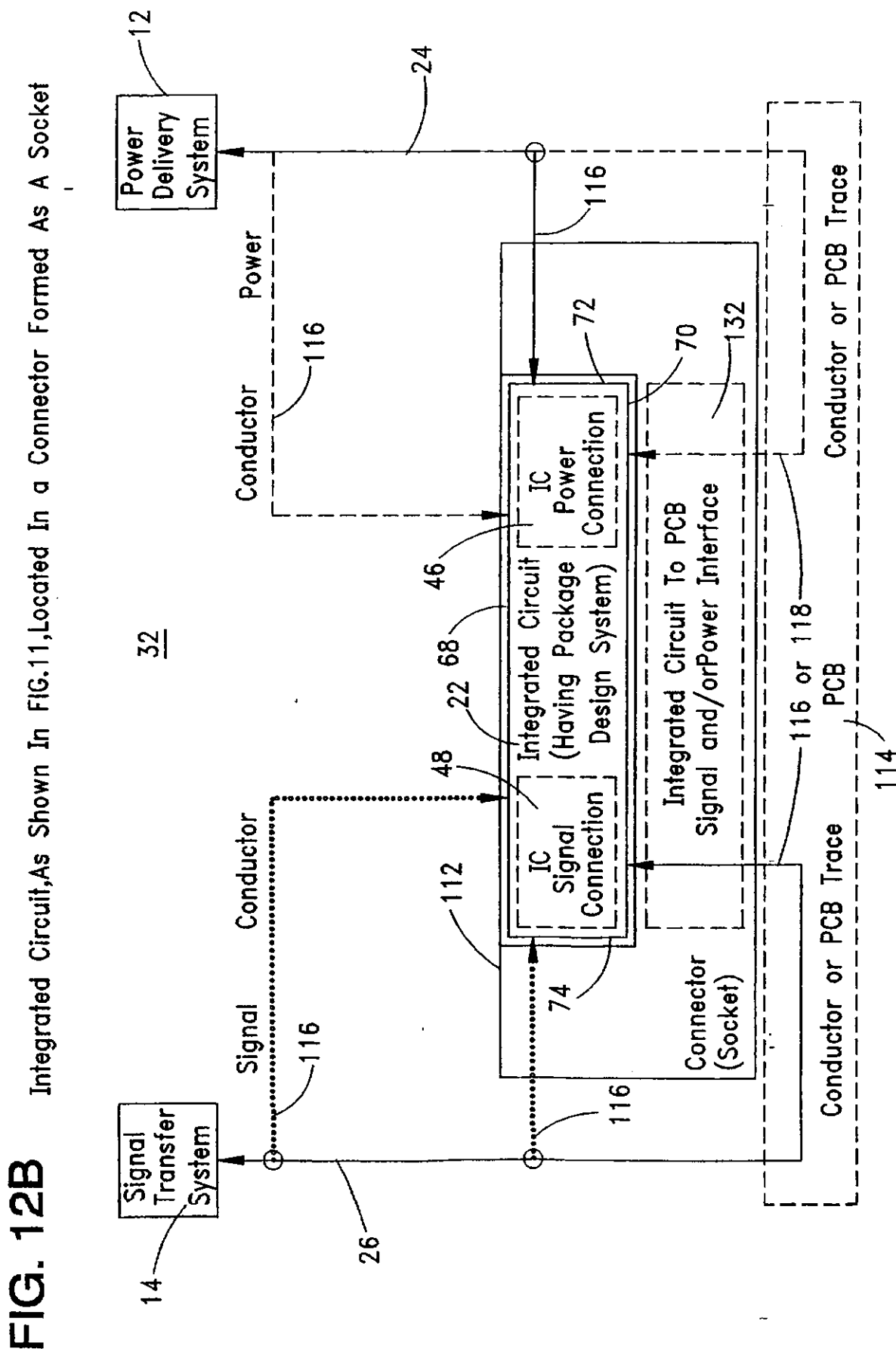
FIG.10C 22
Side of IC
Preferred Power Connections with or
Without Alternate Signal Connections

FIG. 11

Integrated Circuit, As Shown In FIG. 5, Located in a Connector or on a Printed Circuit Board (PCB) and Having Signal And/or Power Connections Formed As a Conductor And/or As a PCB Trace



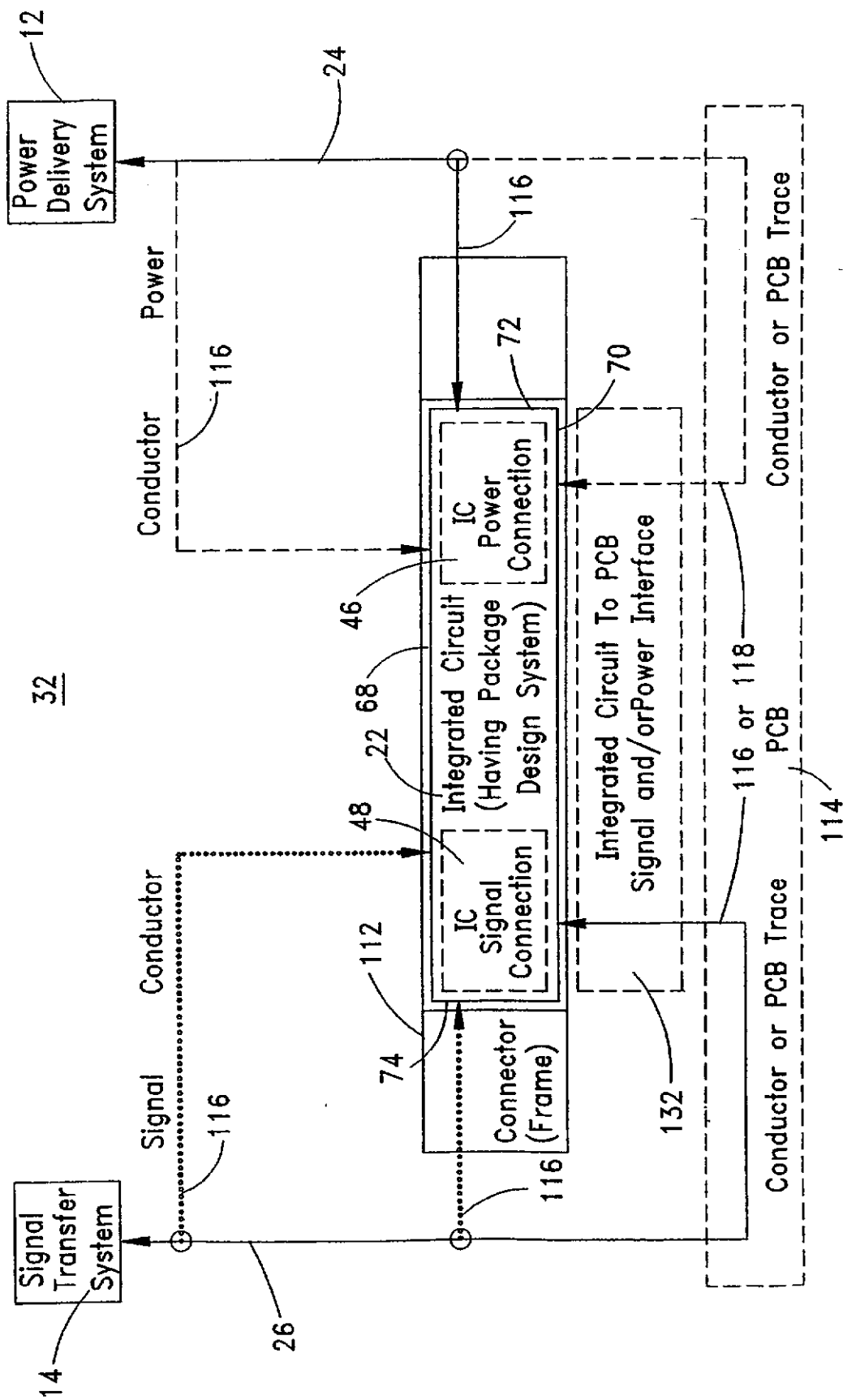
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FIG. 12C

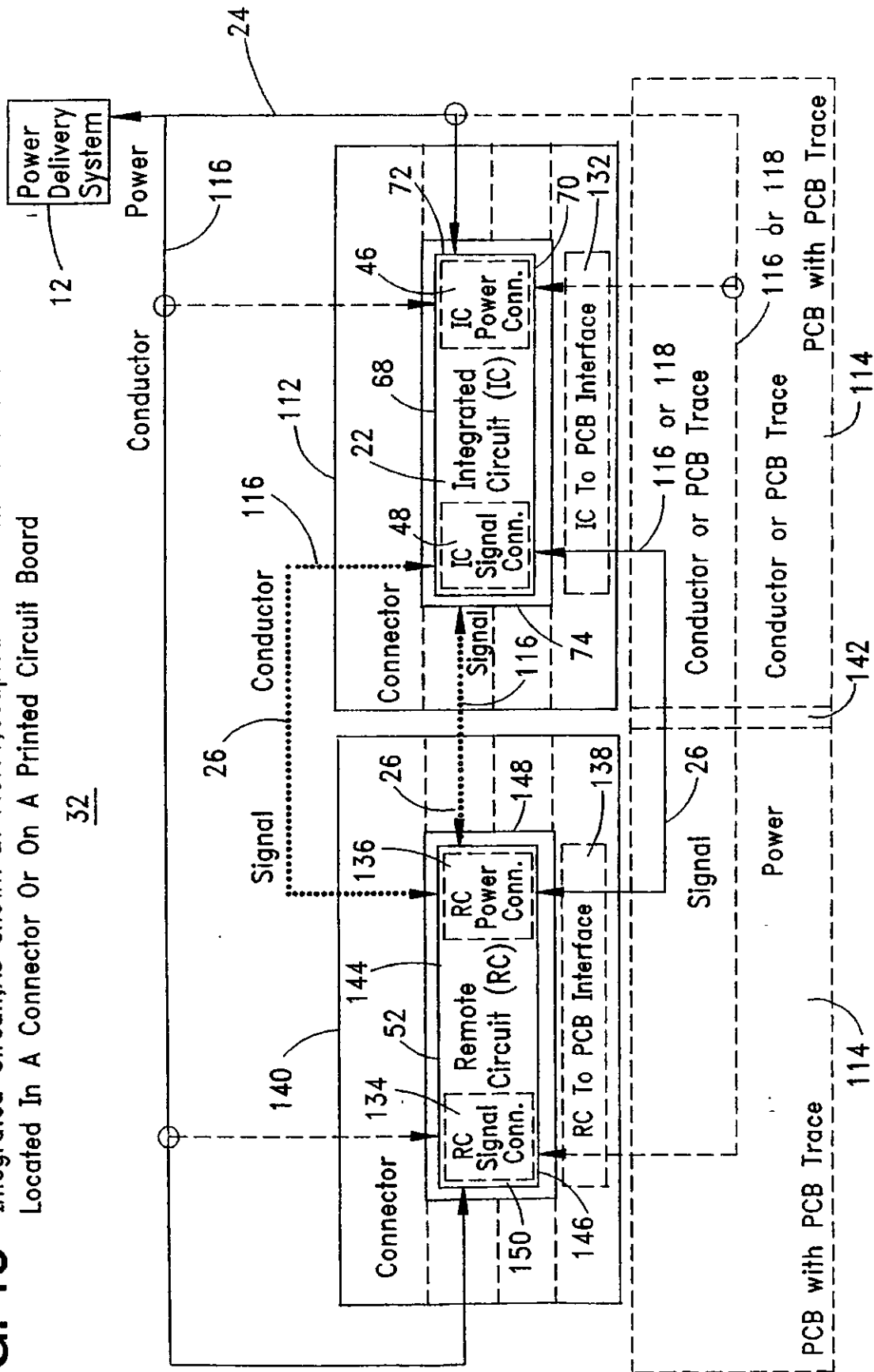
Integrated Circuit, As Shown In FIG. 11, Located In a Connector Formed As A Frame



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FIG. 13 Integrated Circuit, As shown In FIG. 11, Coupled To A Remote Circuit Located In A Connector Or On A Printed Circuit Board

32



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FIG. 14

Integrated Circuit and Remote Circuit, As Shown In FIG. 13, Coupled Together In A Stacked Arrangement

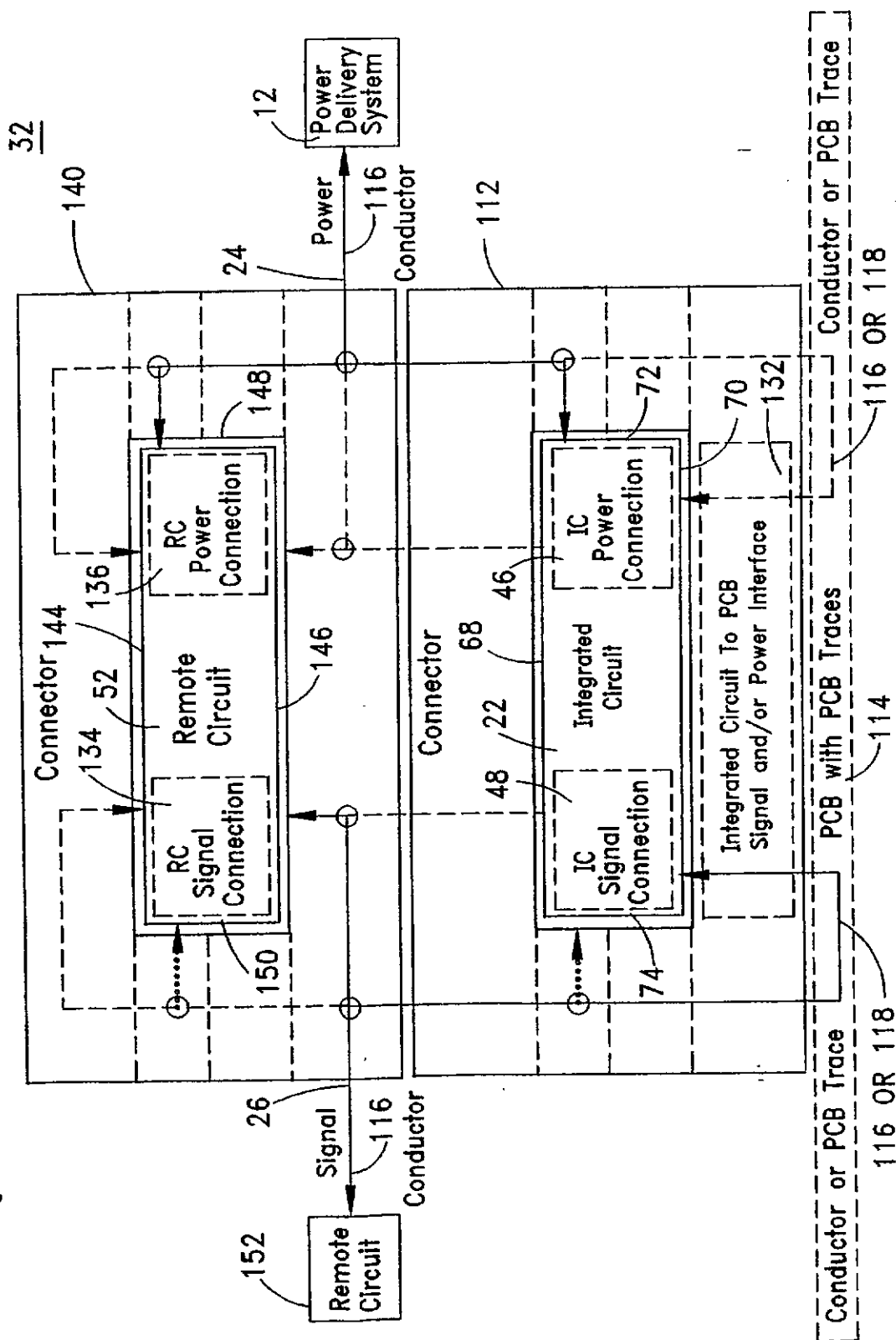


FIG. 15 Integrated Circuit And Remote Circuit,As Shown In FIGS. 13 or 14,Each Having A Voltage Regulator Module And Decoupling Capacitance Located In A Connector ,

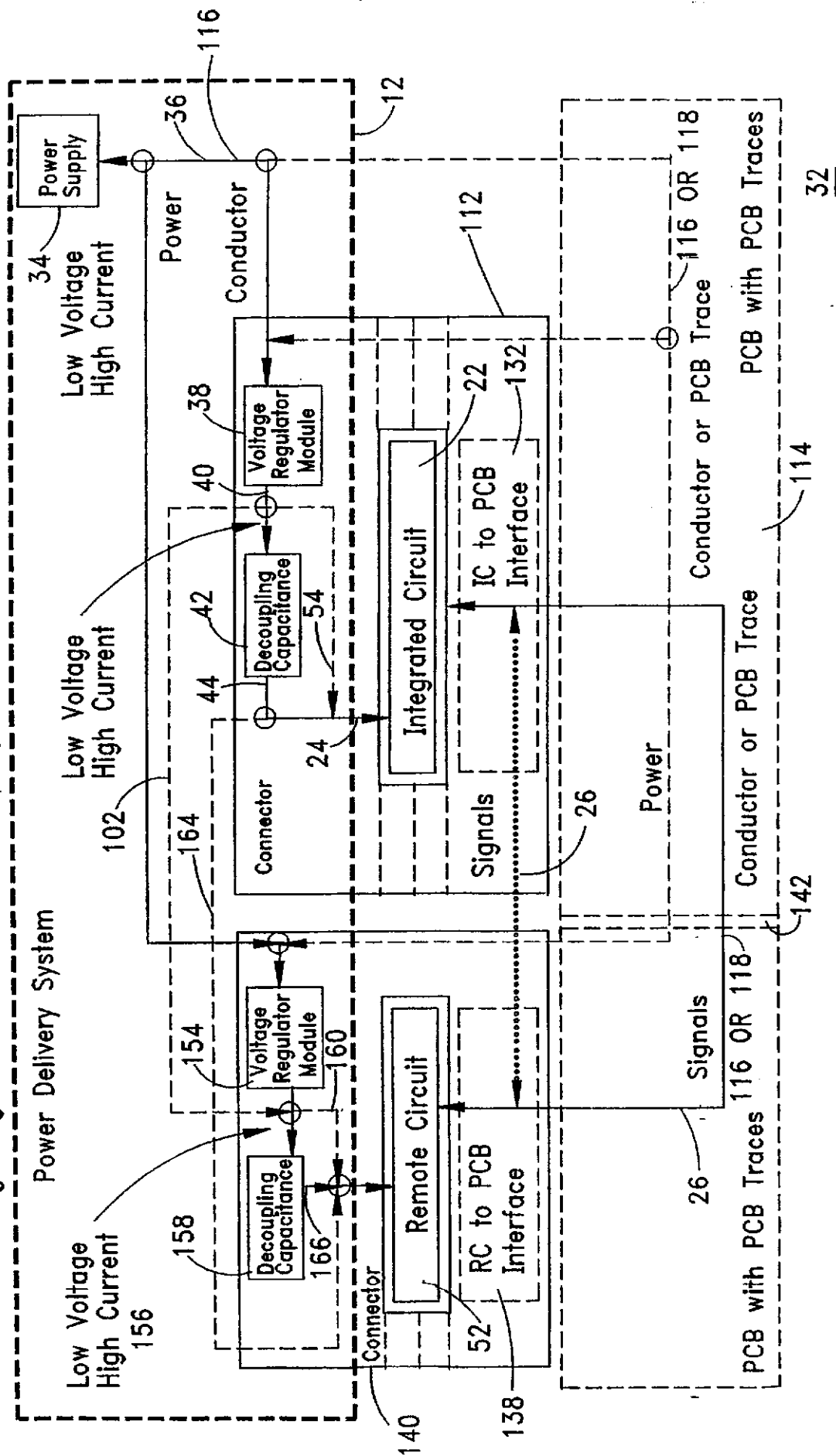
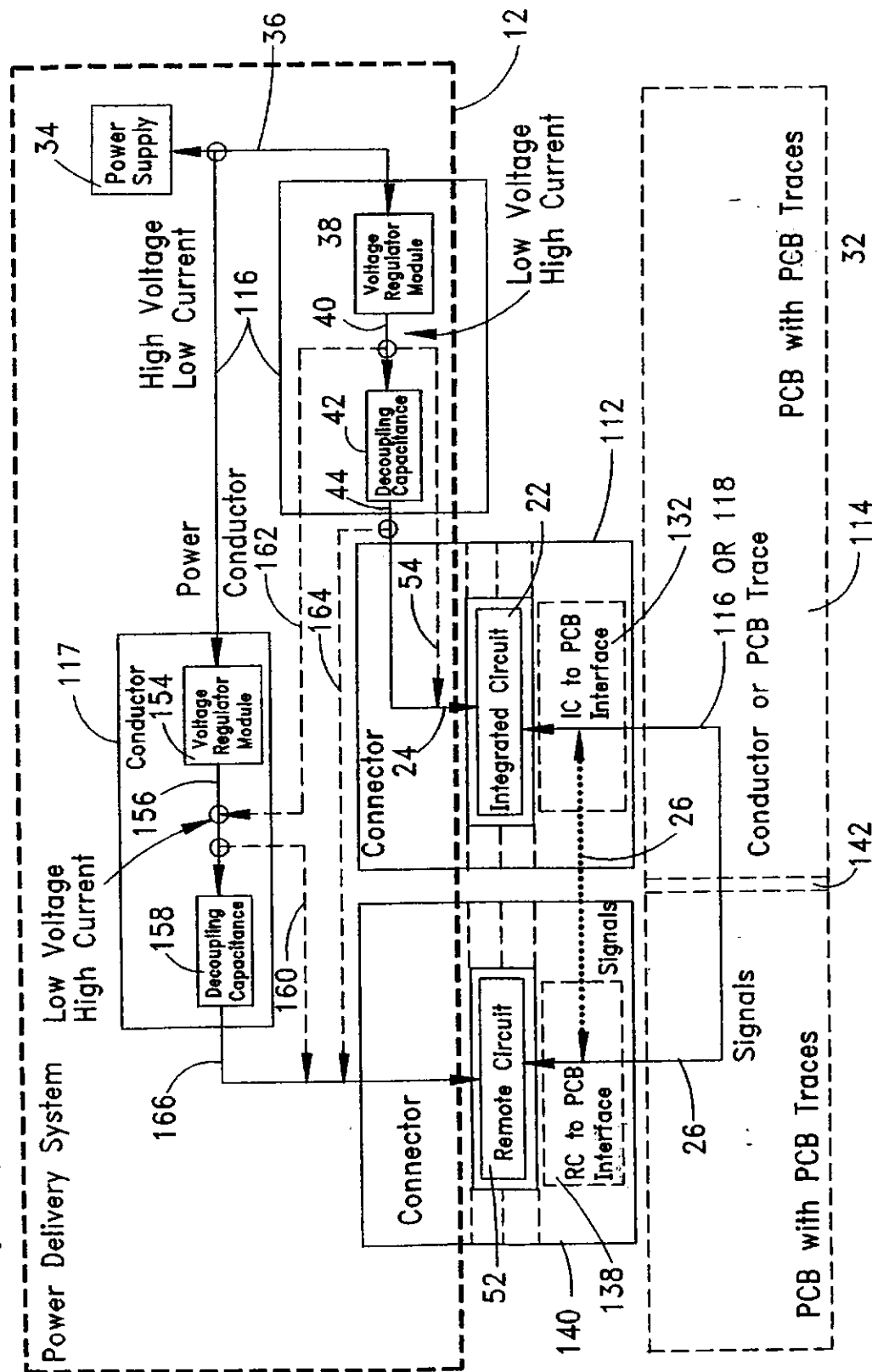


FIG. 16

Integrated Circuit And Remote Circuit, As Shown In FIGS. 13 or 14, Each Having A Voltage Regulator Module And Decoupling Capacitance Located In A Conductor



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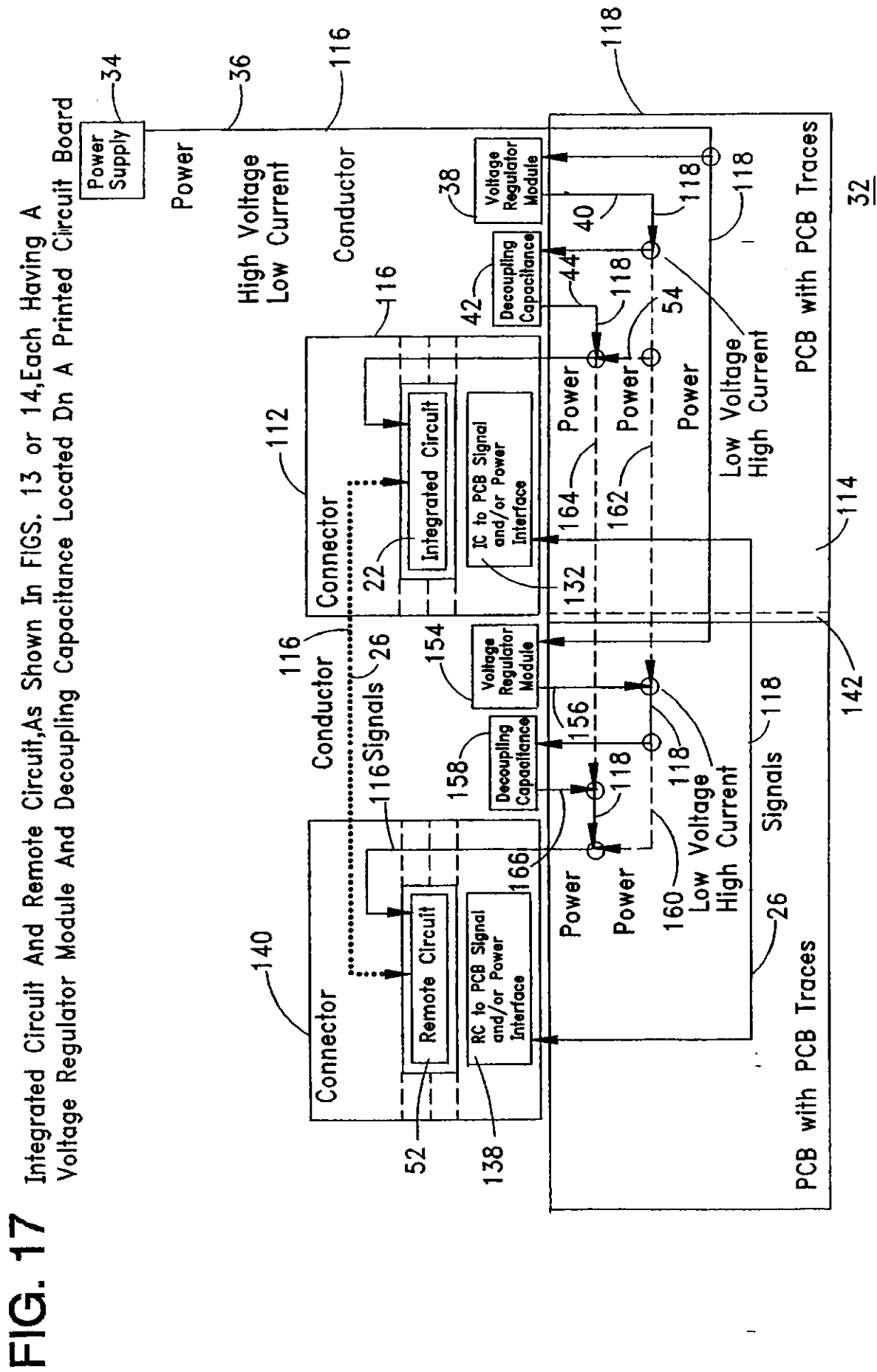
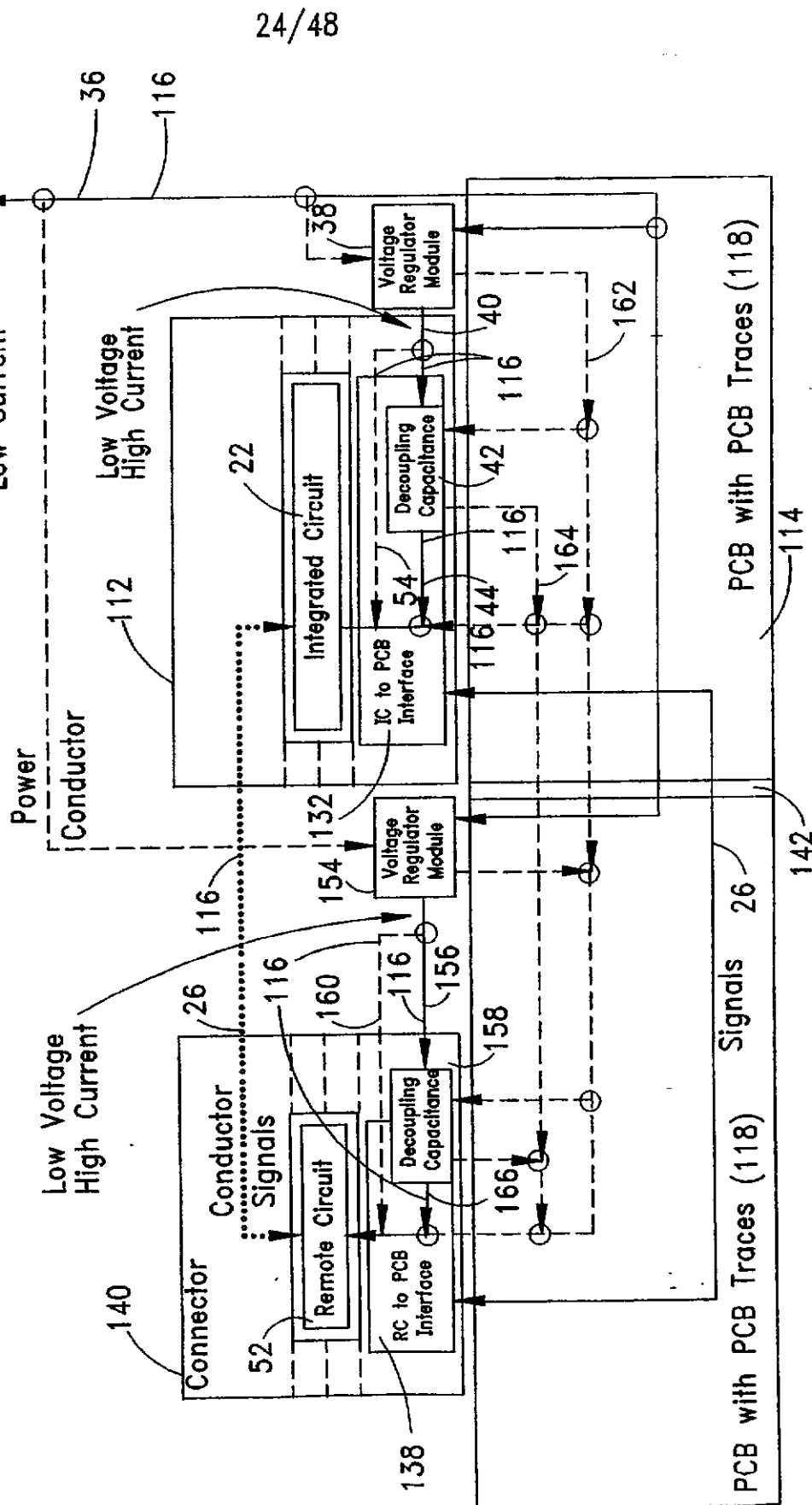


FIG. 19 Integrated Circuit and Remote Circuit, As Shown In FIGS. 13 or 14, Each Having A Voltage Regulator Module Located In A Connector

32



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FIG. 20 Integrated Circuit, AS Shown In FIG. 11, And Having A Thermal Management System And An Electromagnetic Interference (EMI) Control System

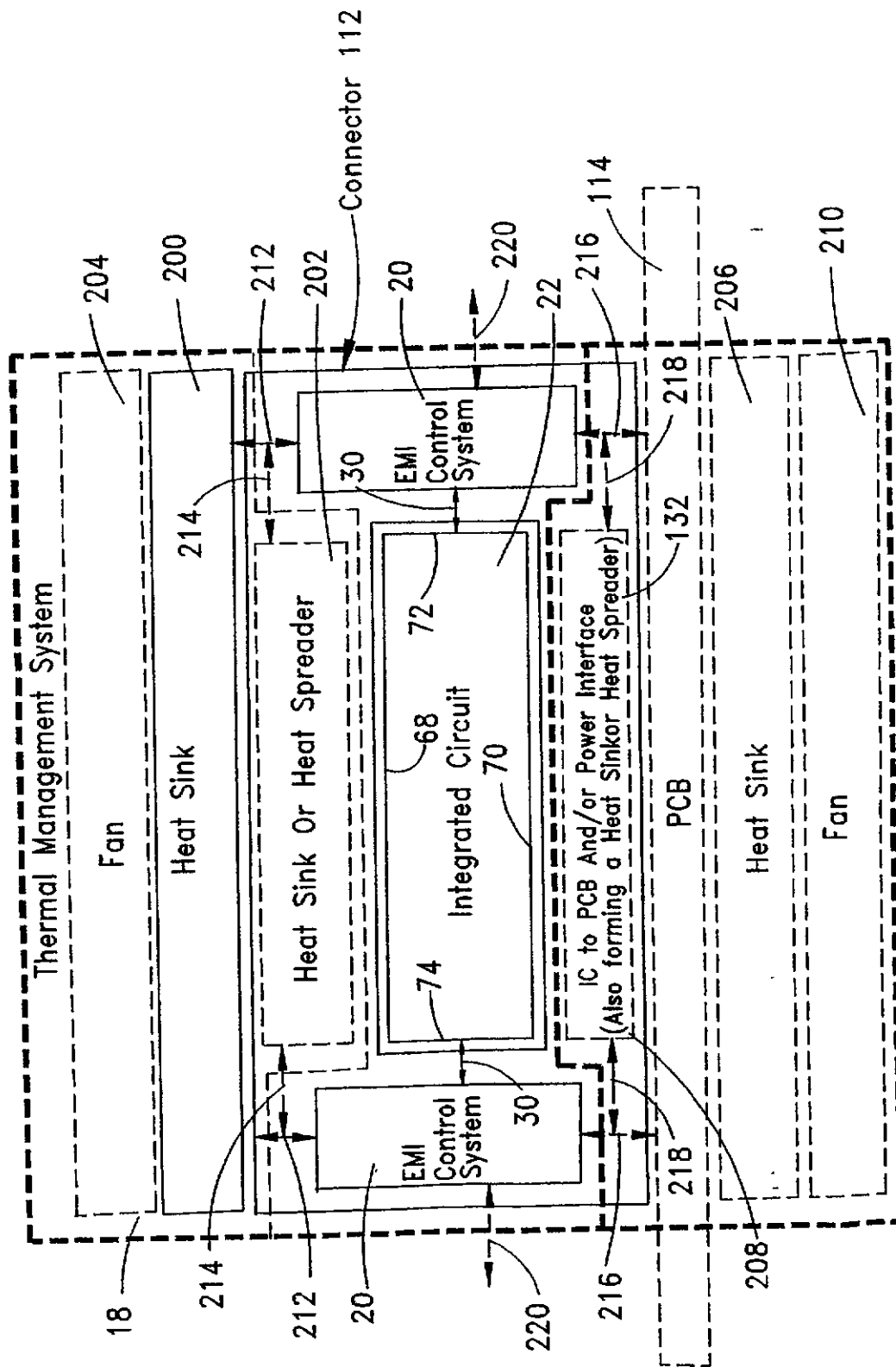


FIG. 21

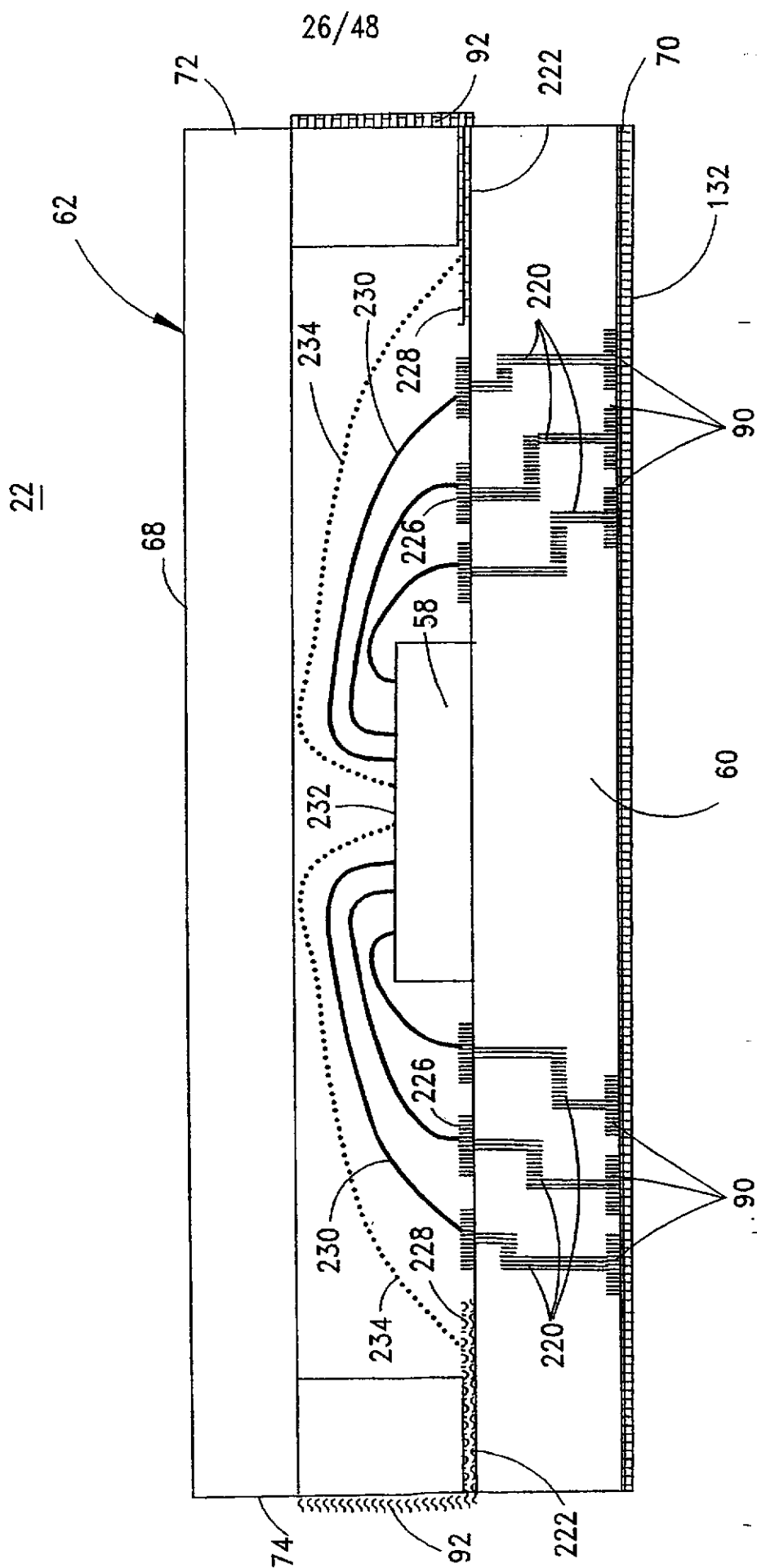


FIG. 23

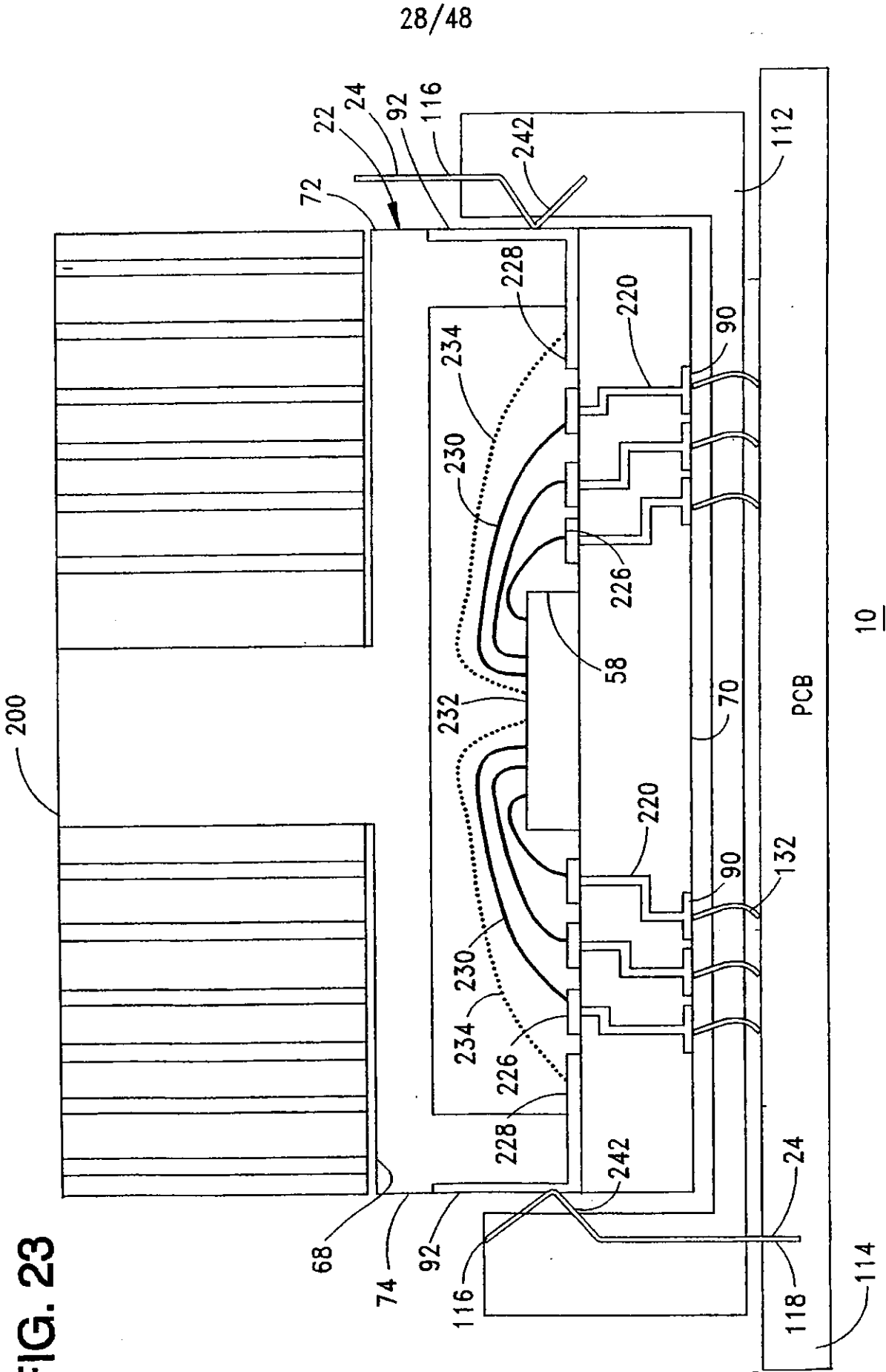
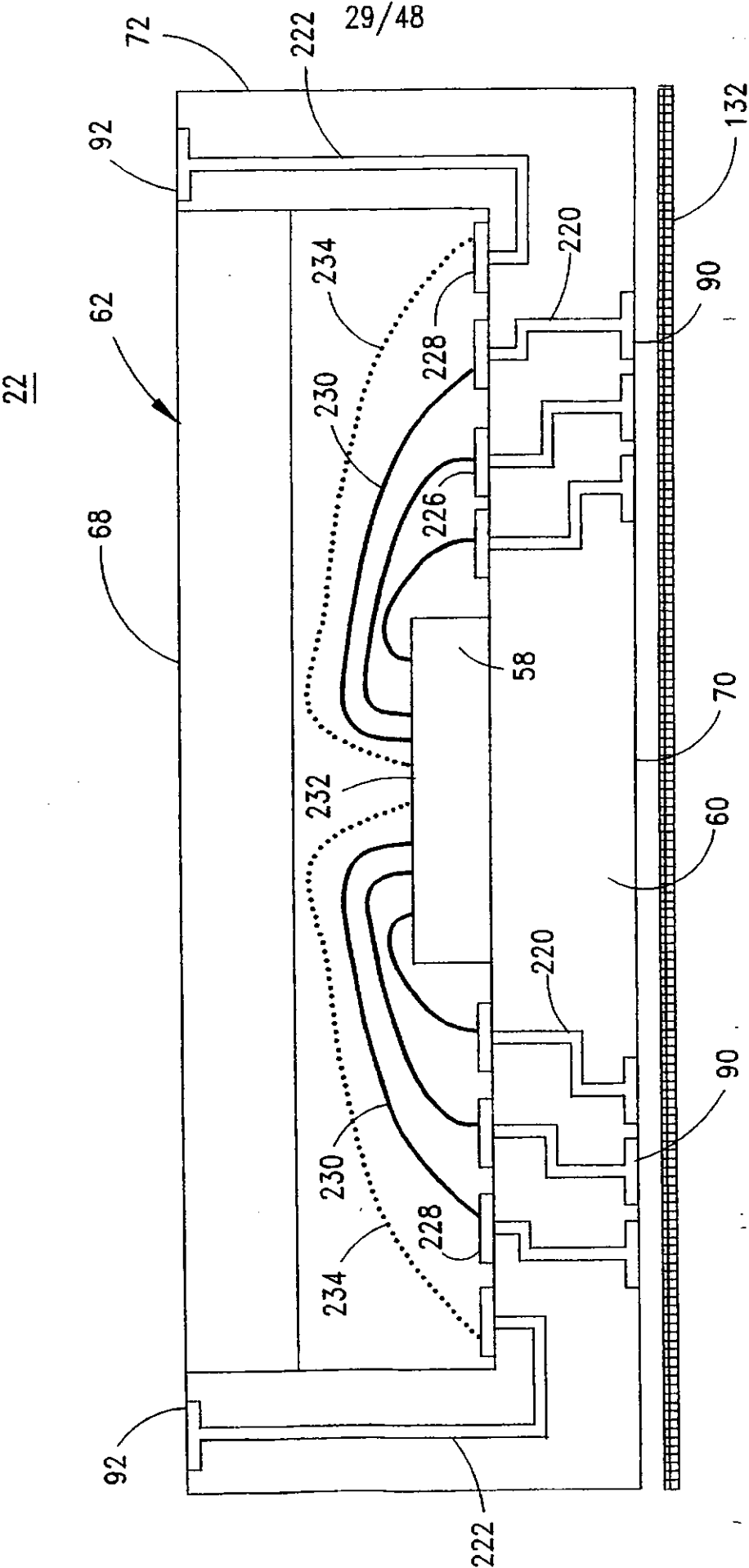


FIG. 24



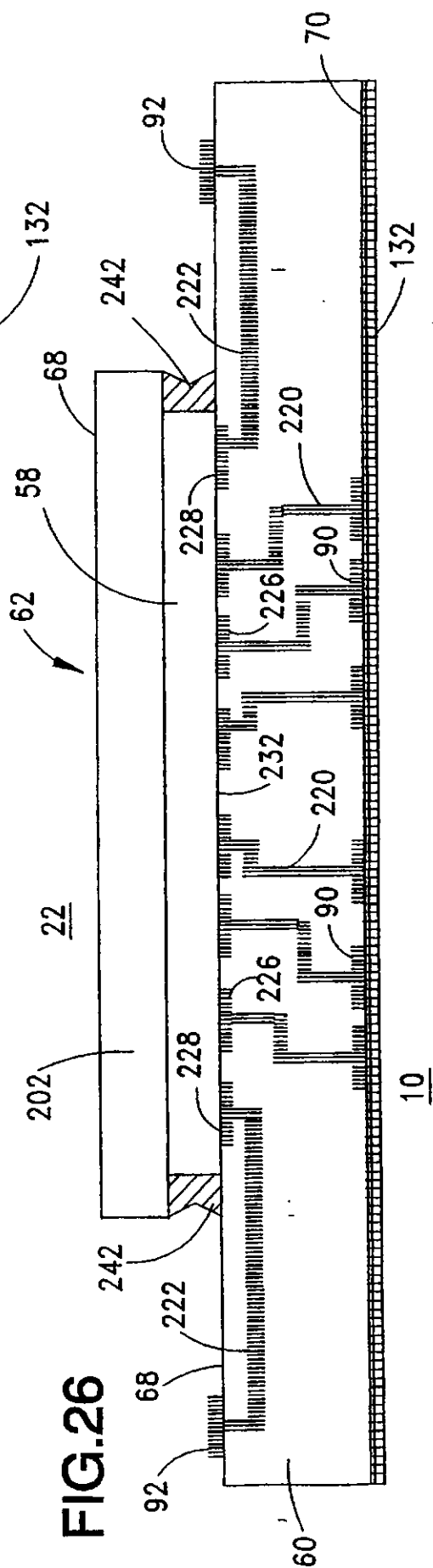
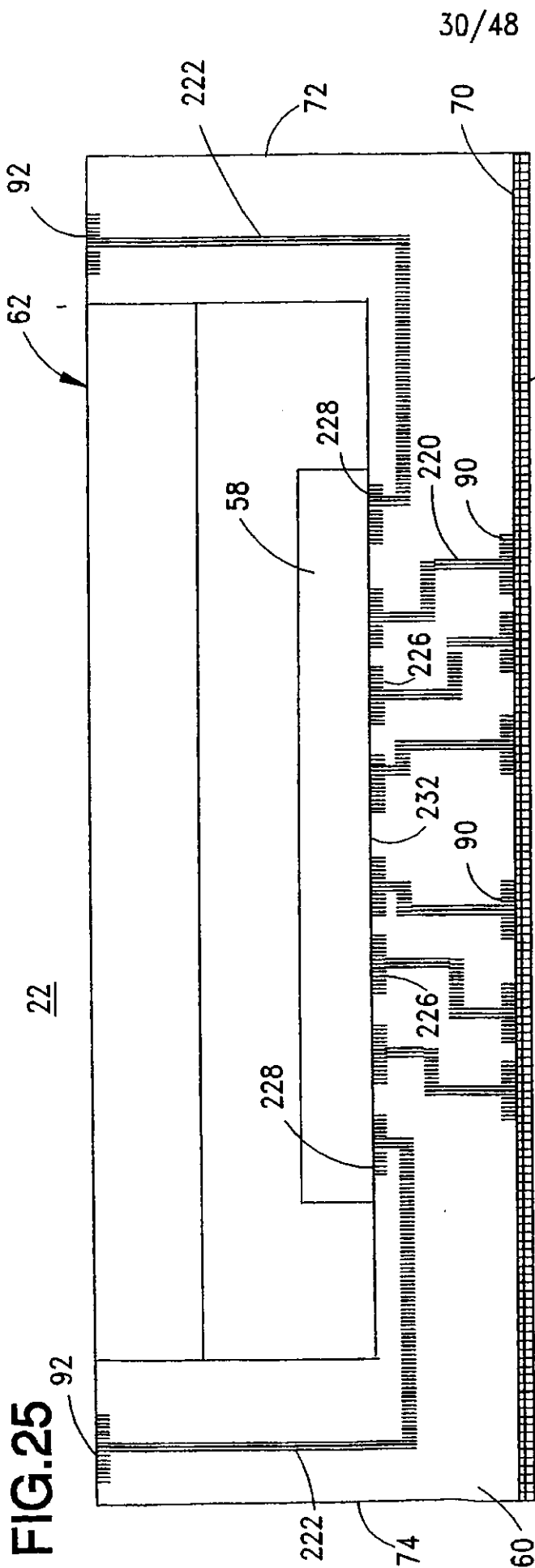


FIG. 27

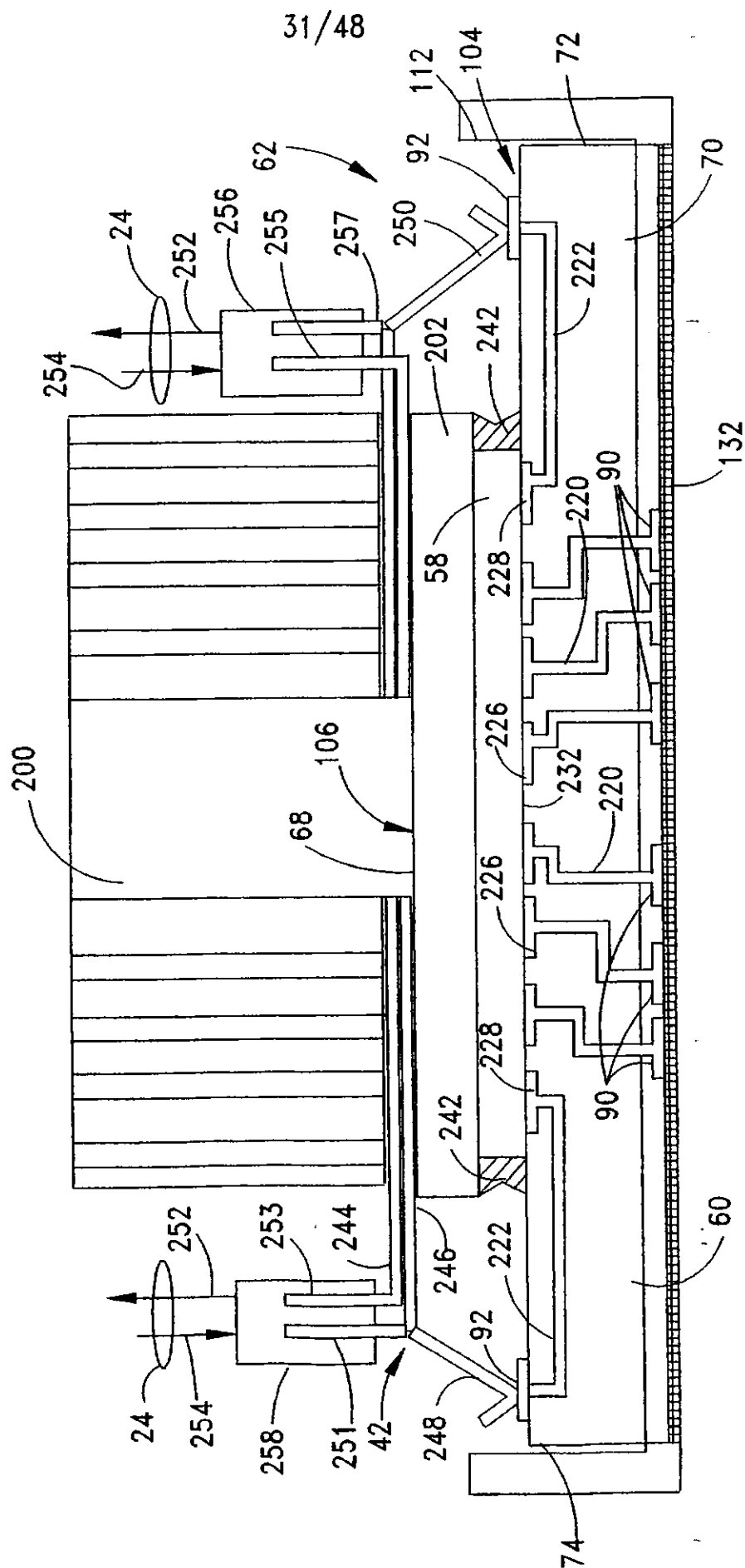


FIG. 28

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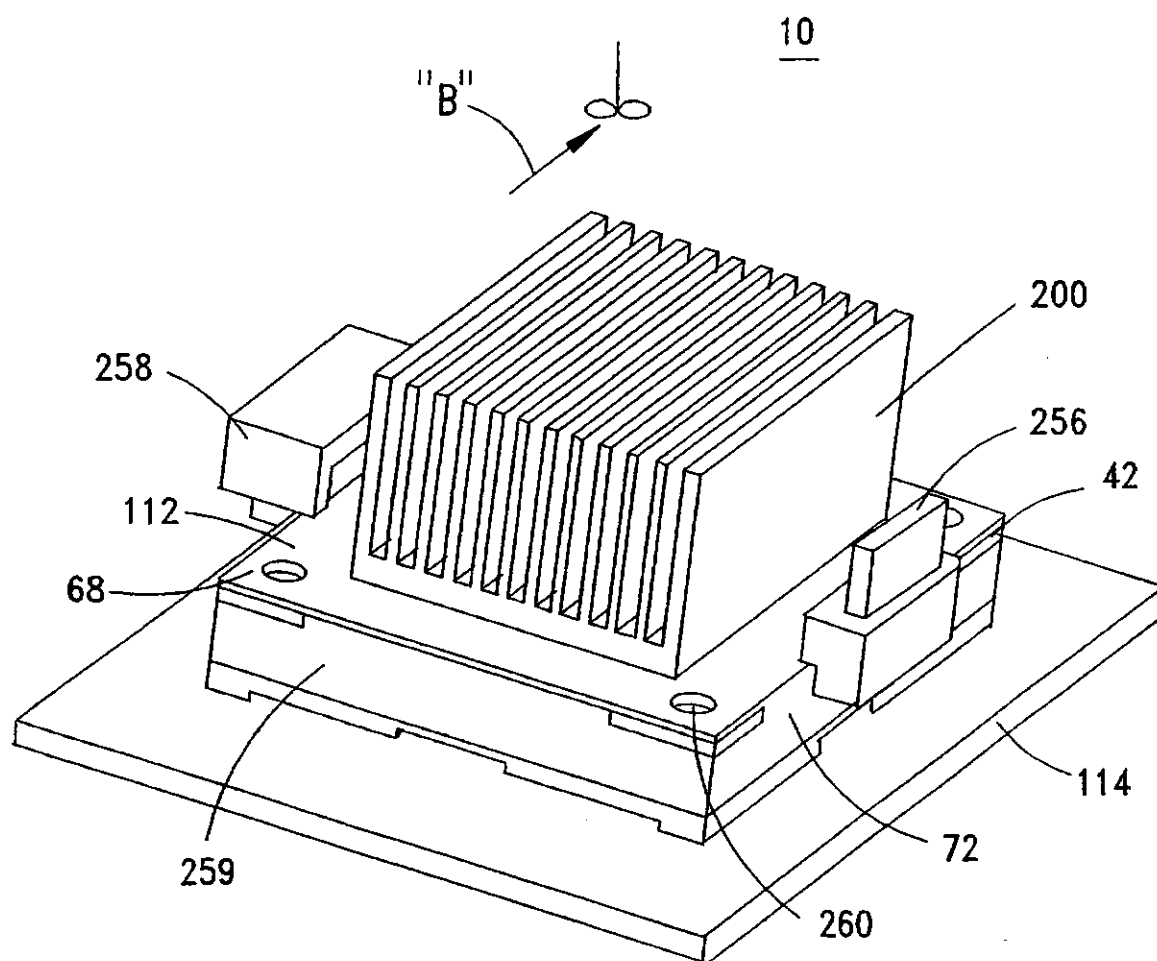
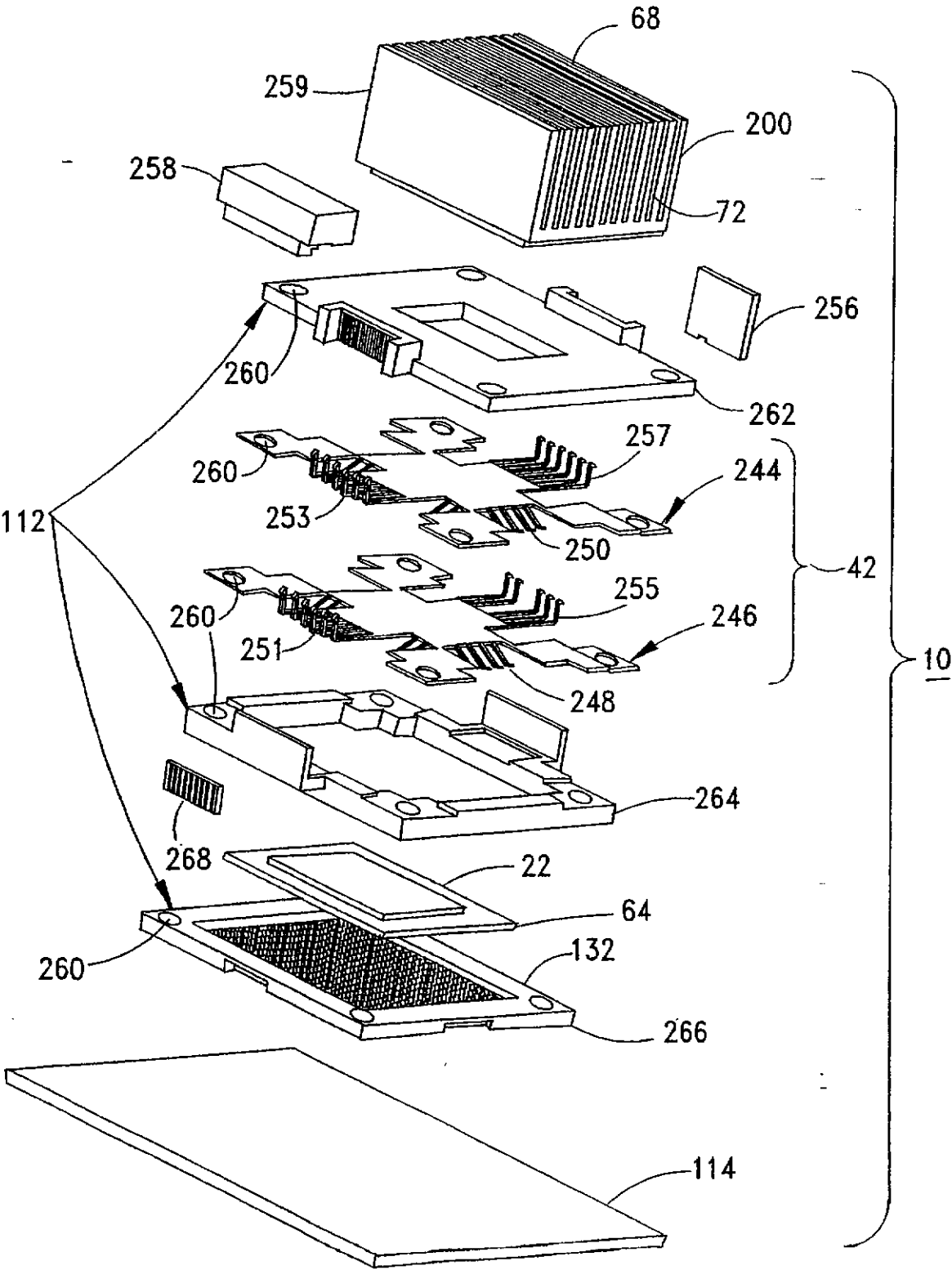


FIG. 29



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FIG. 32

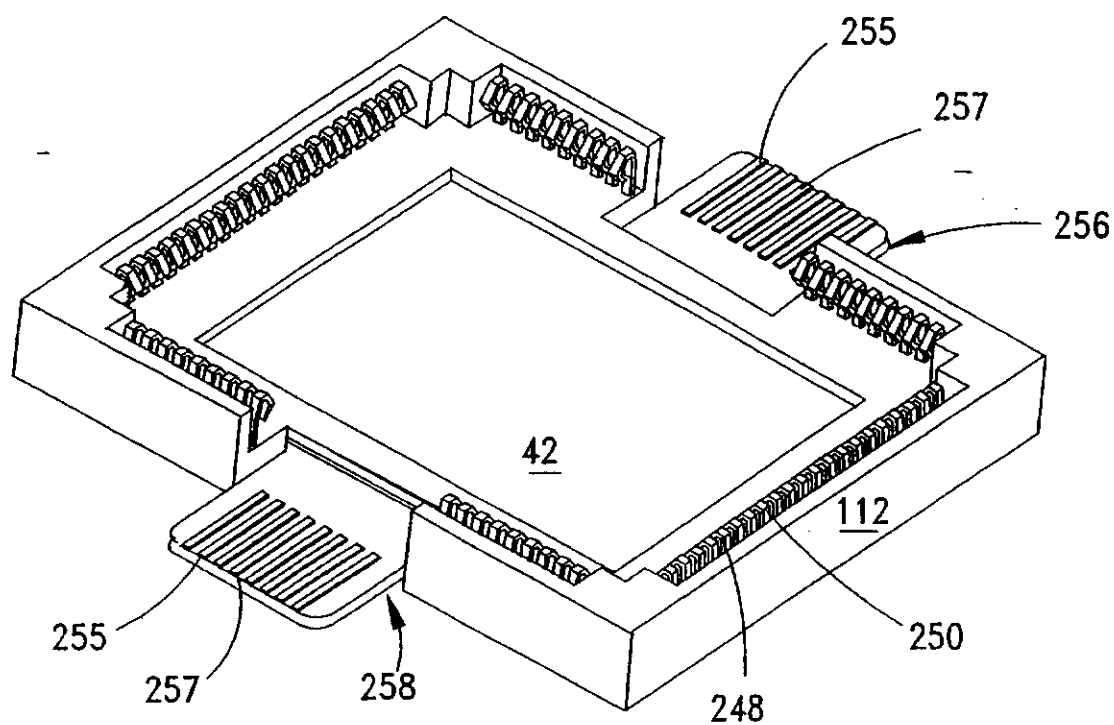
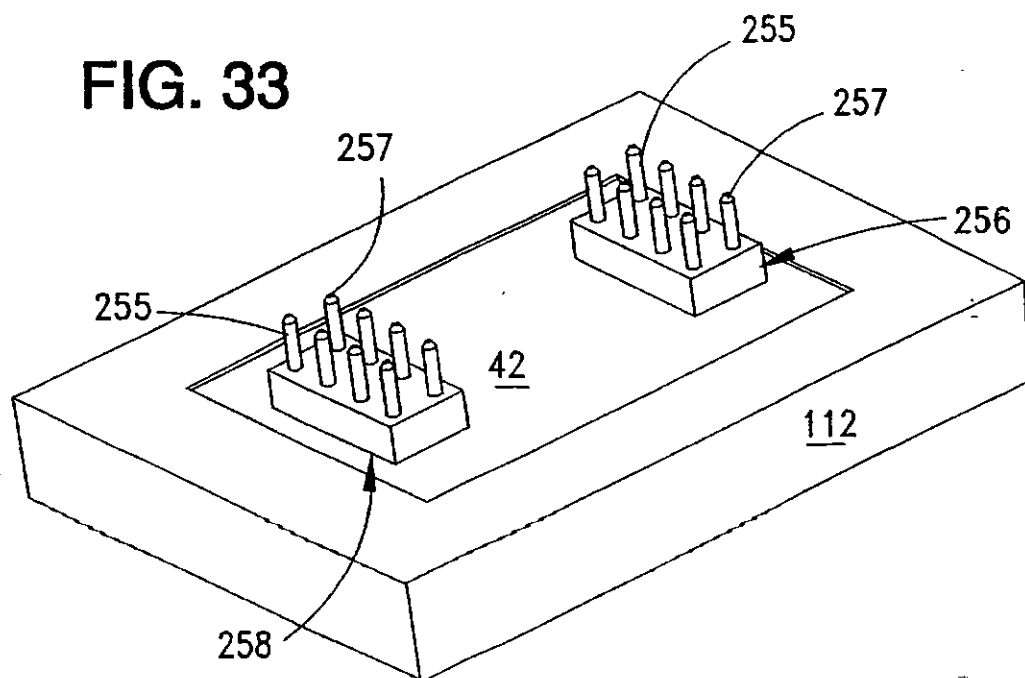


FIG. 33



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FIG. 34

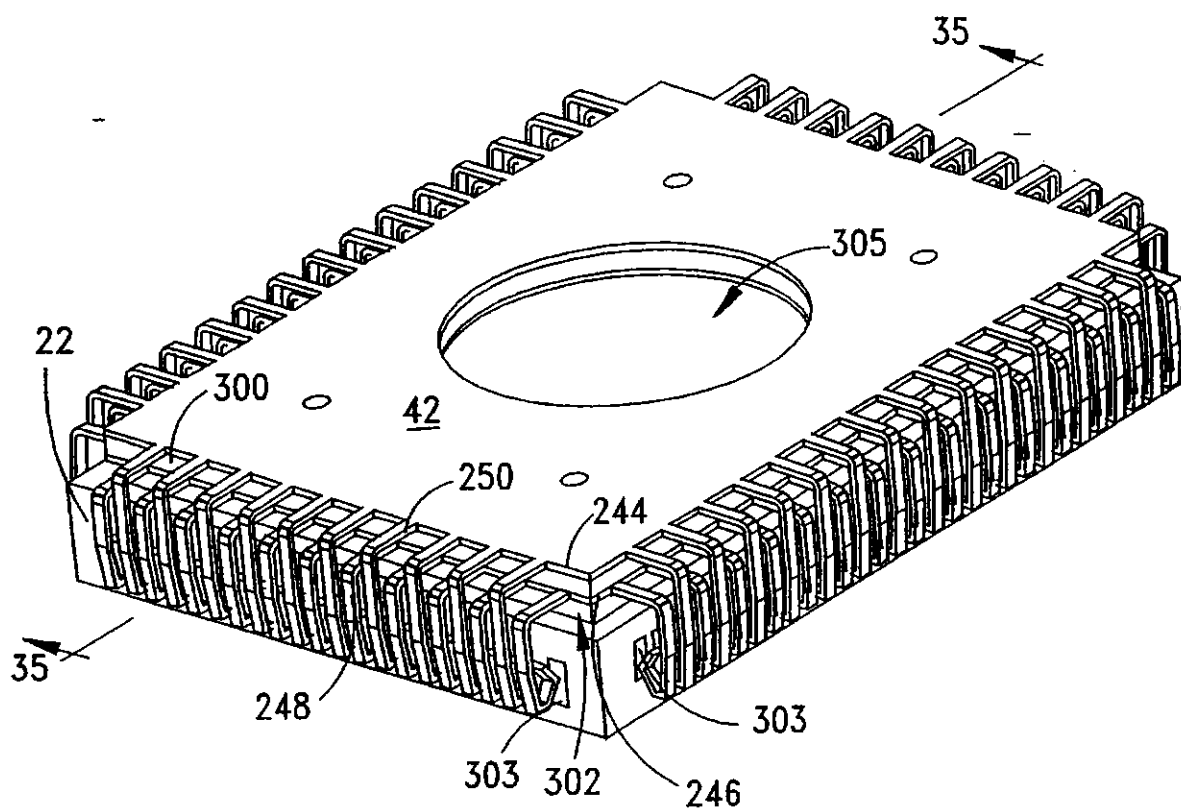


FIG. 35

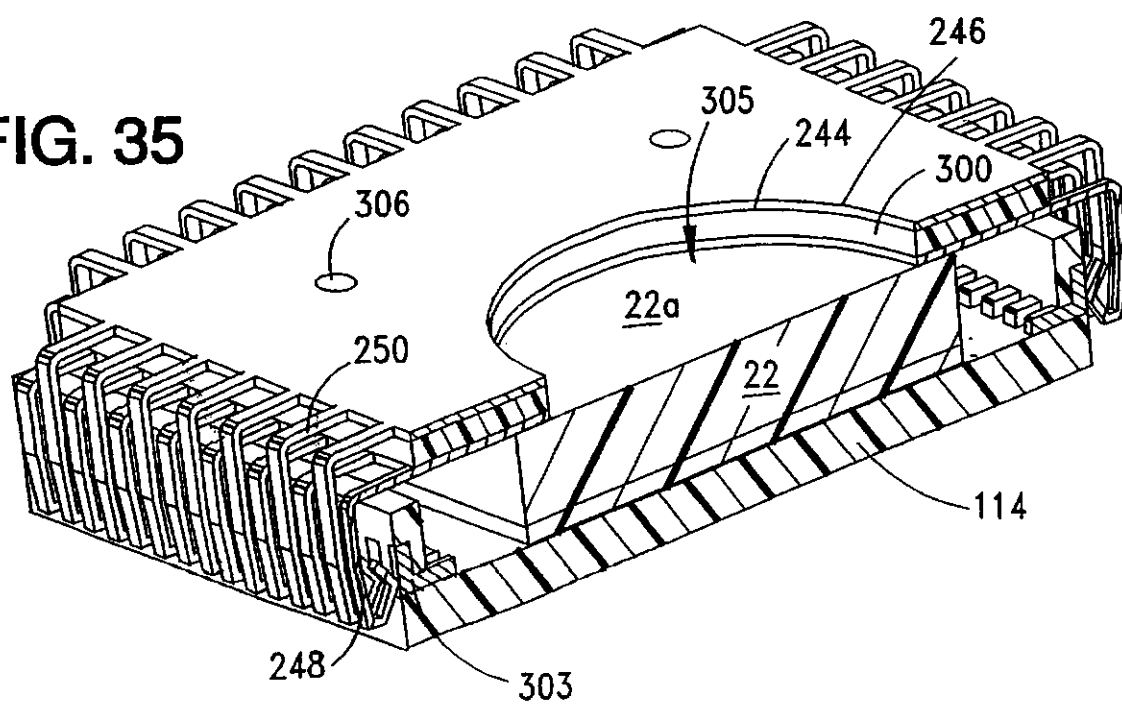


FIG.37

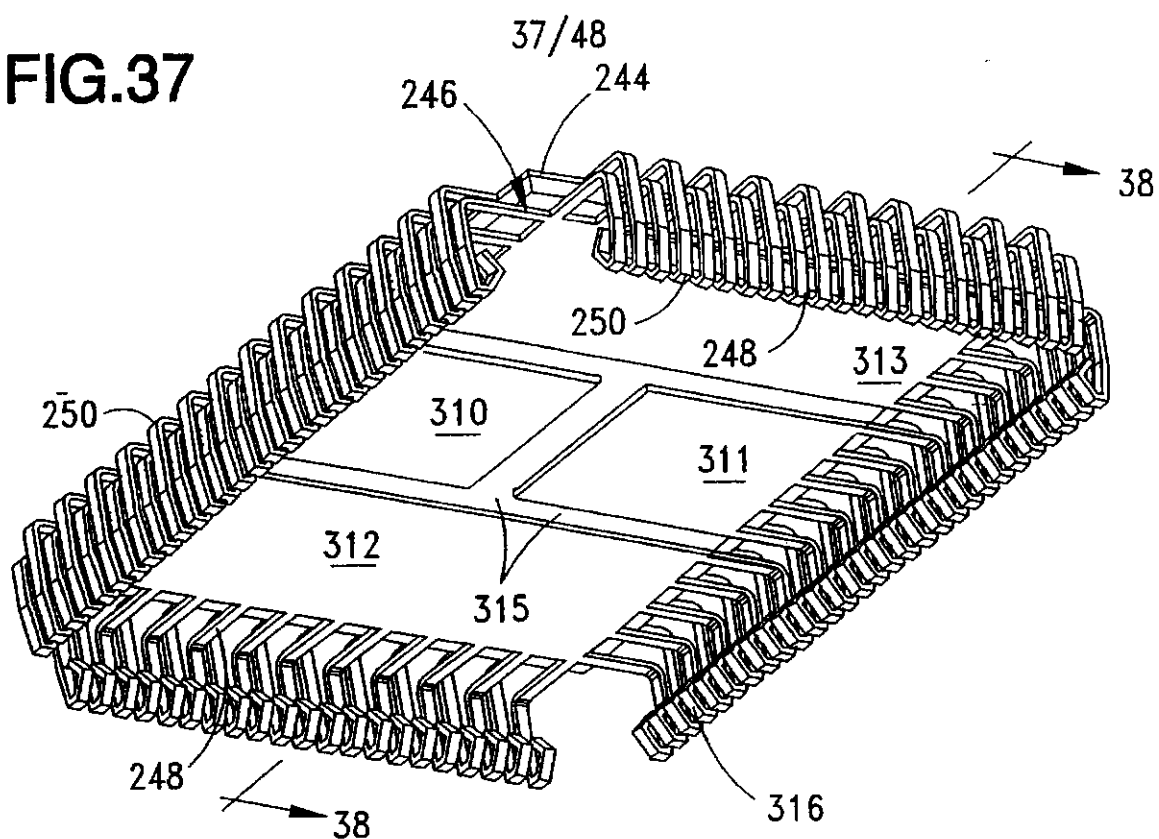
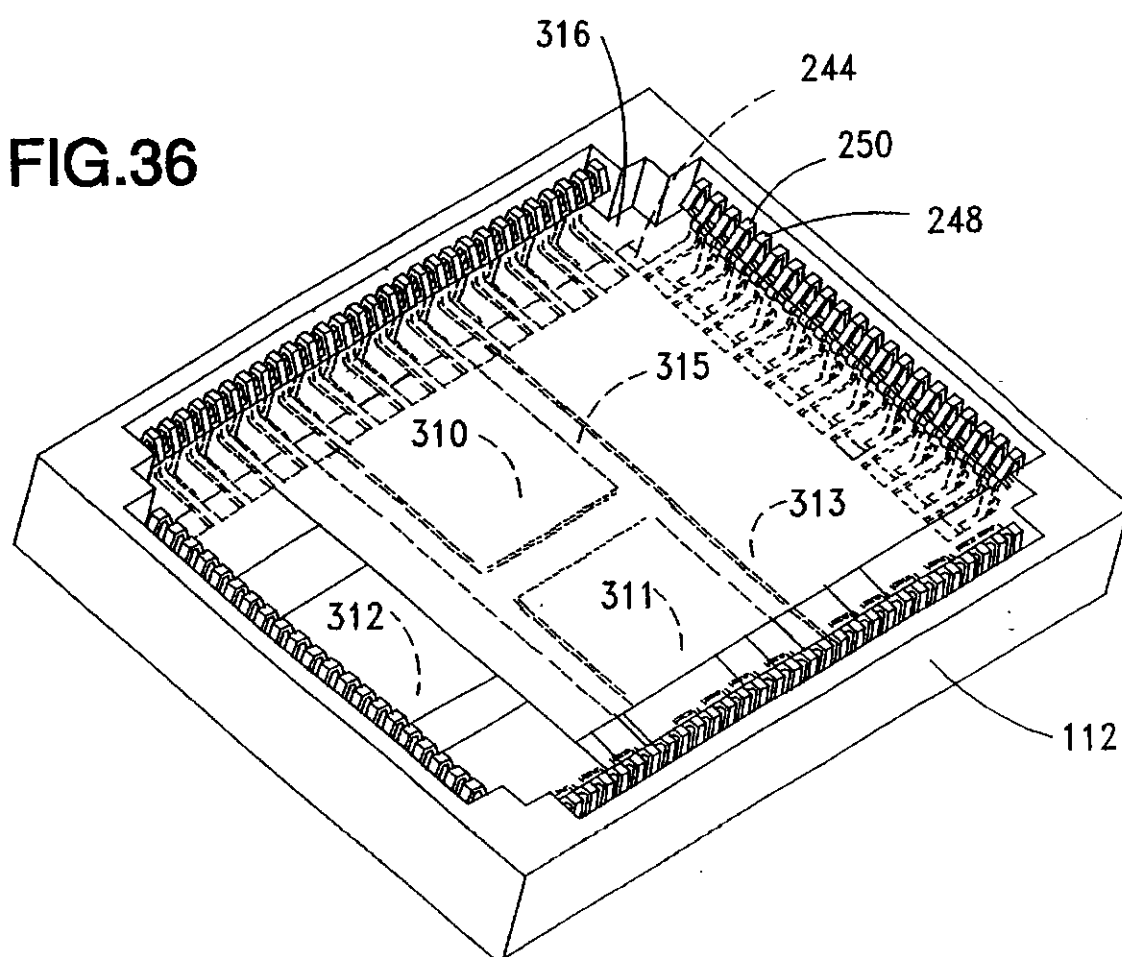


FIG.36



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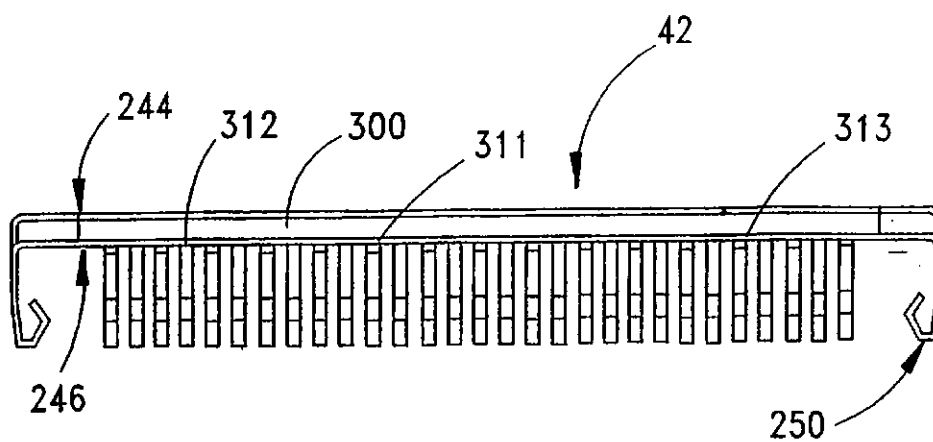
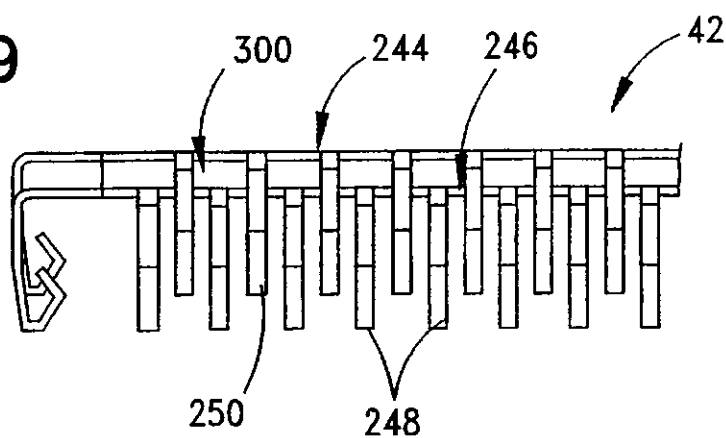
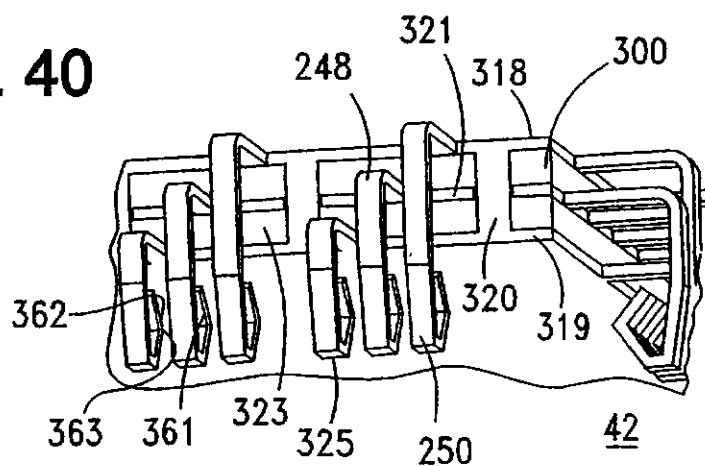
FIG. 38**FIG. 39****FIG. 40**

FIG. 41

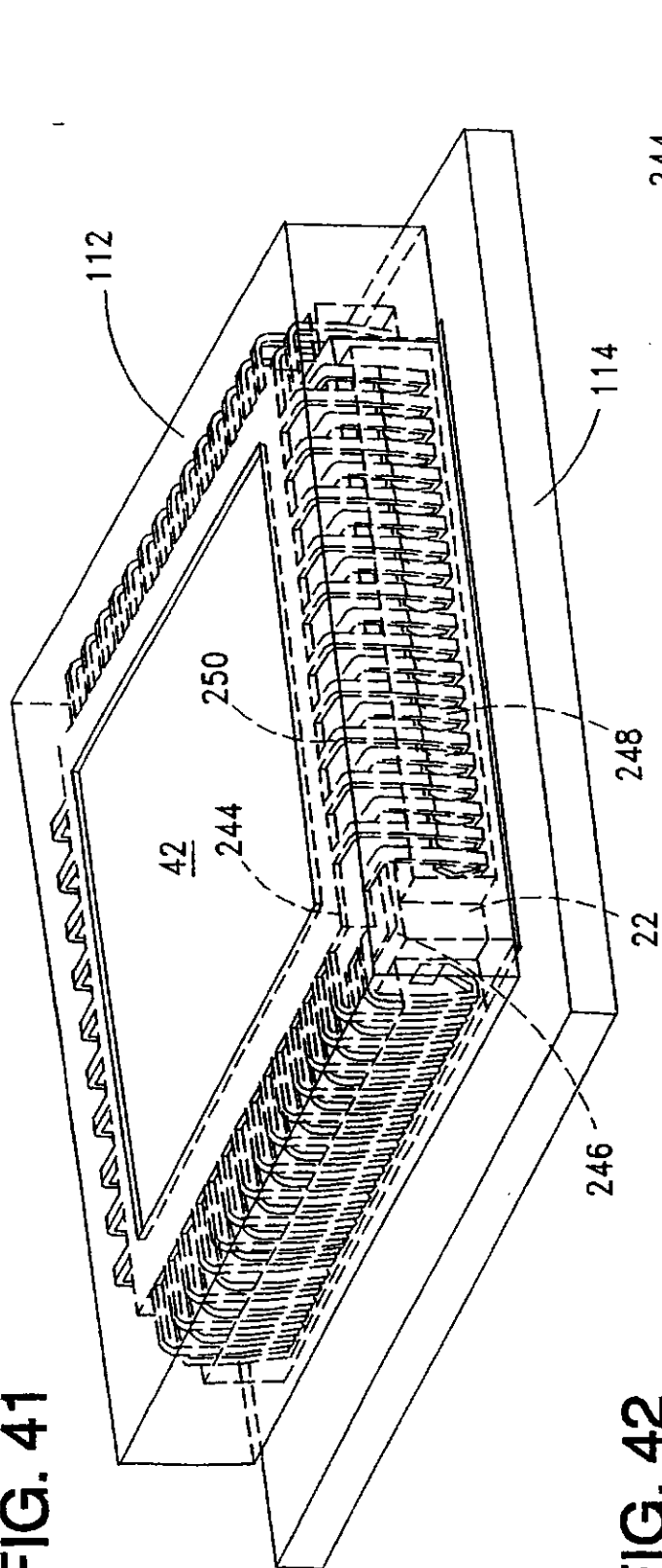
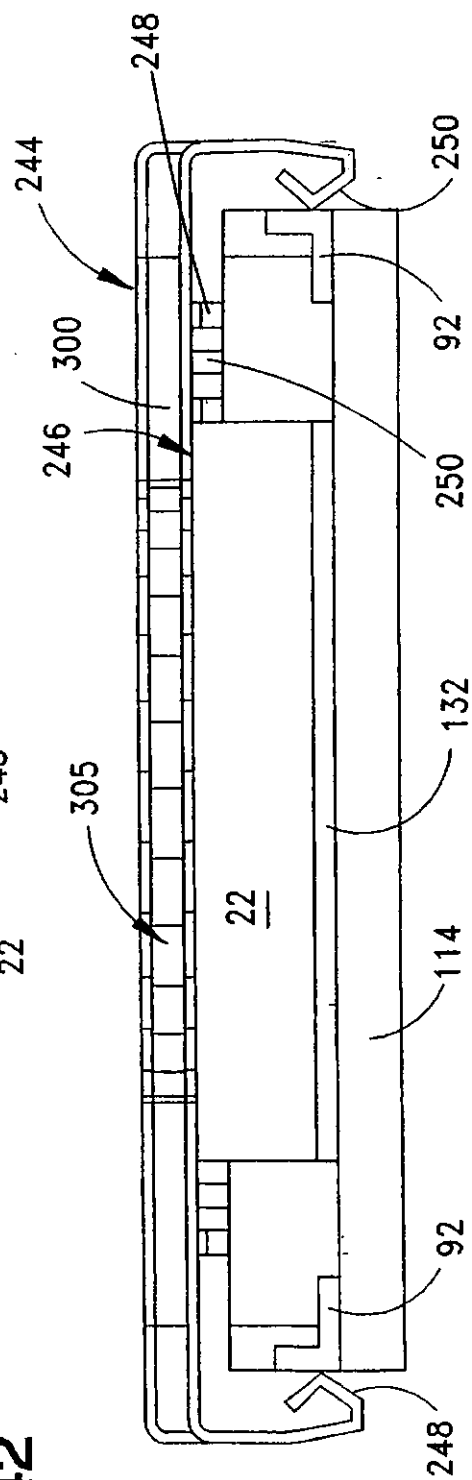


FIG. 42



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FIG.43

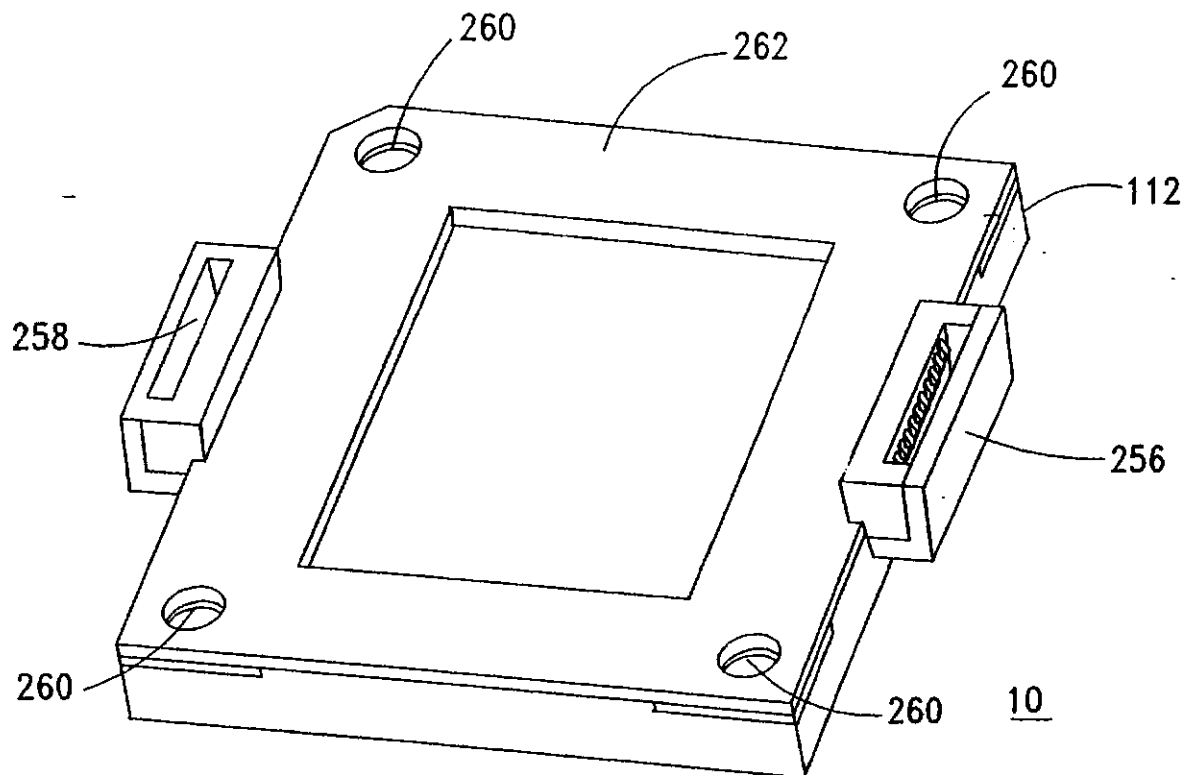
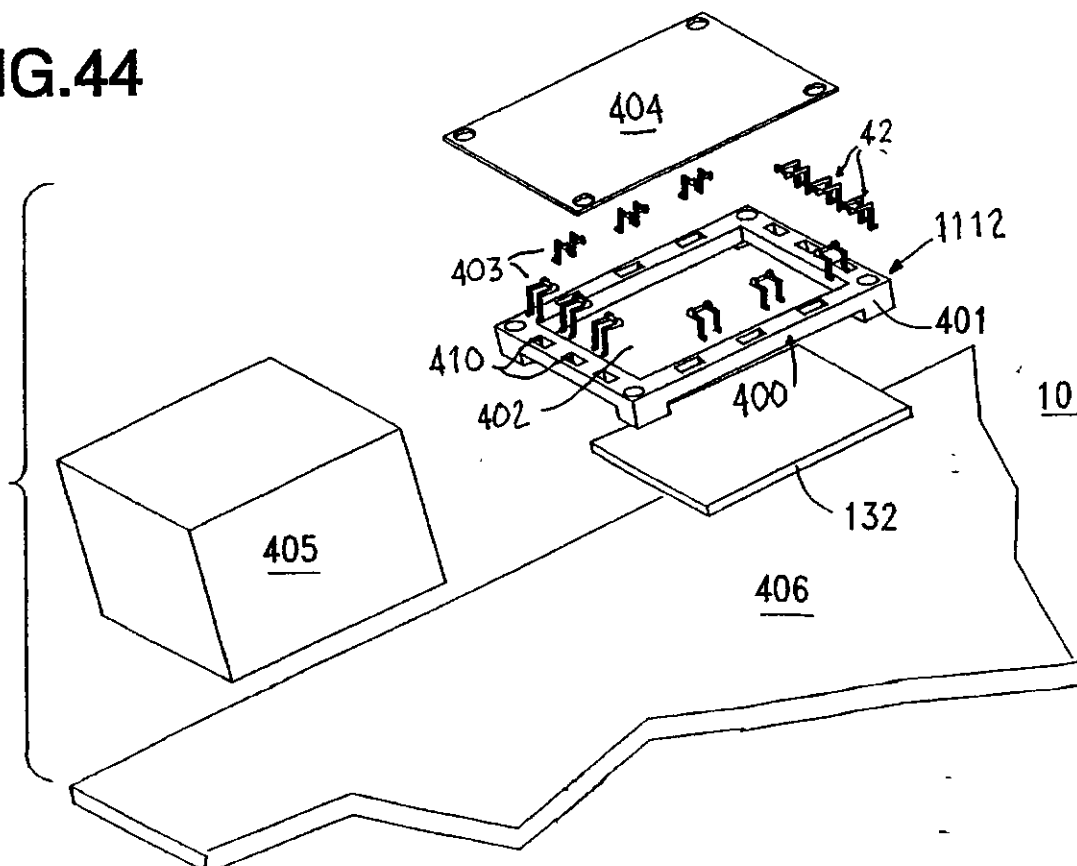


FIG.44



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FIG. 45

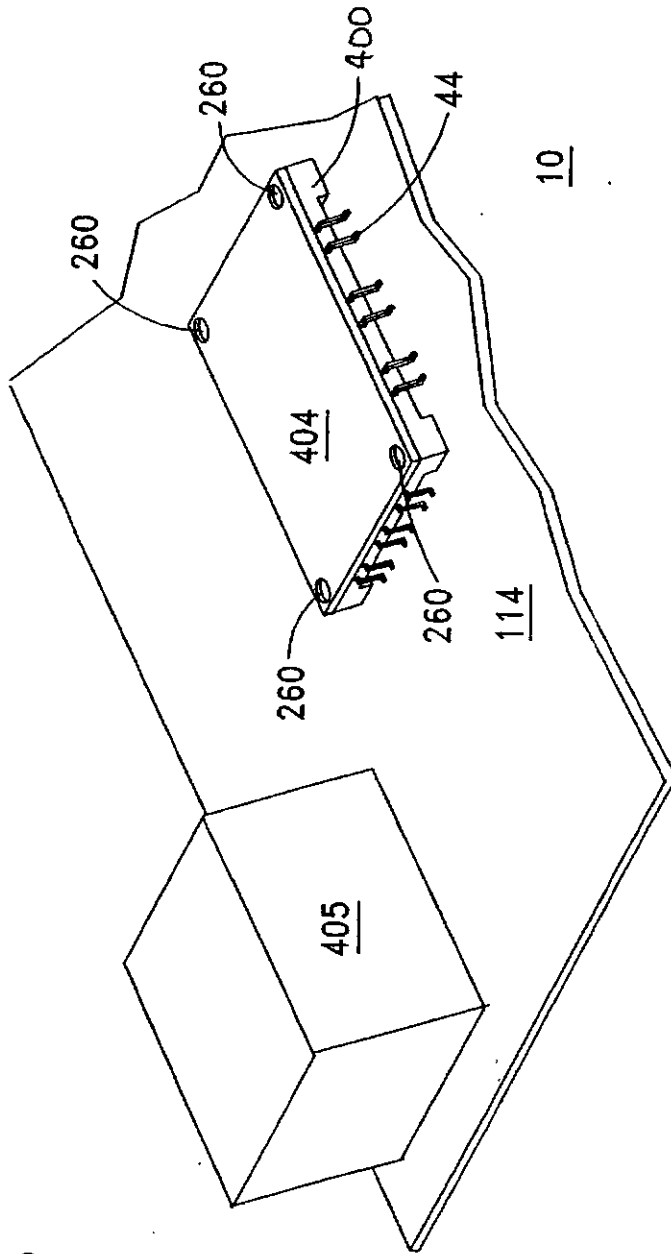


FIG. 46

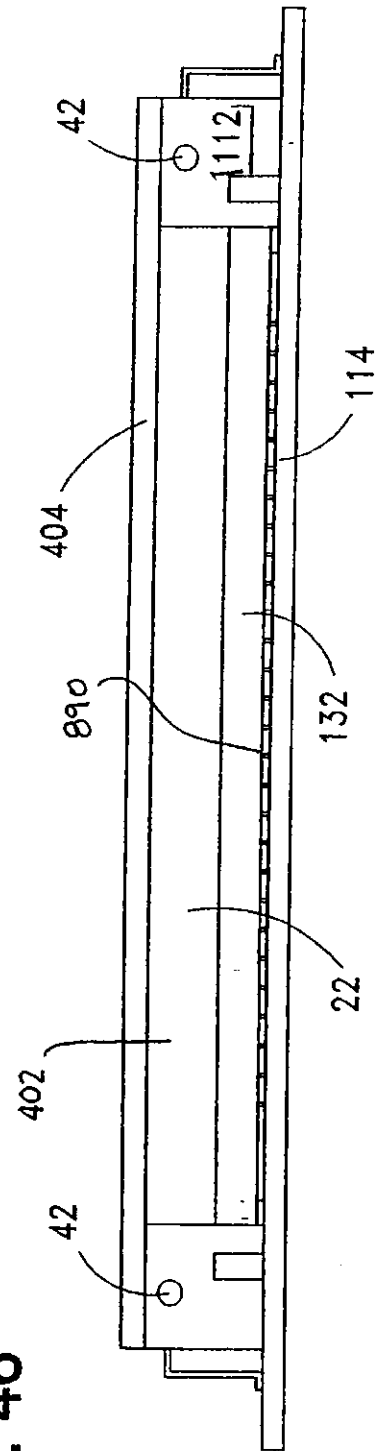
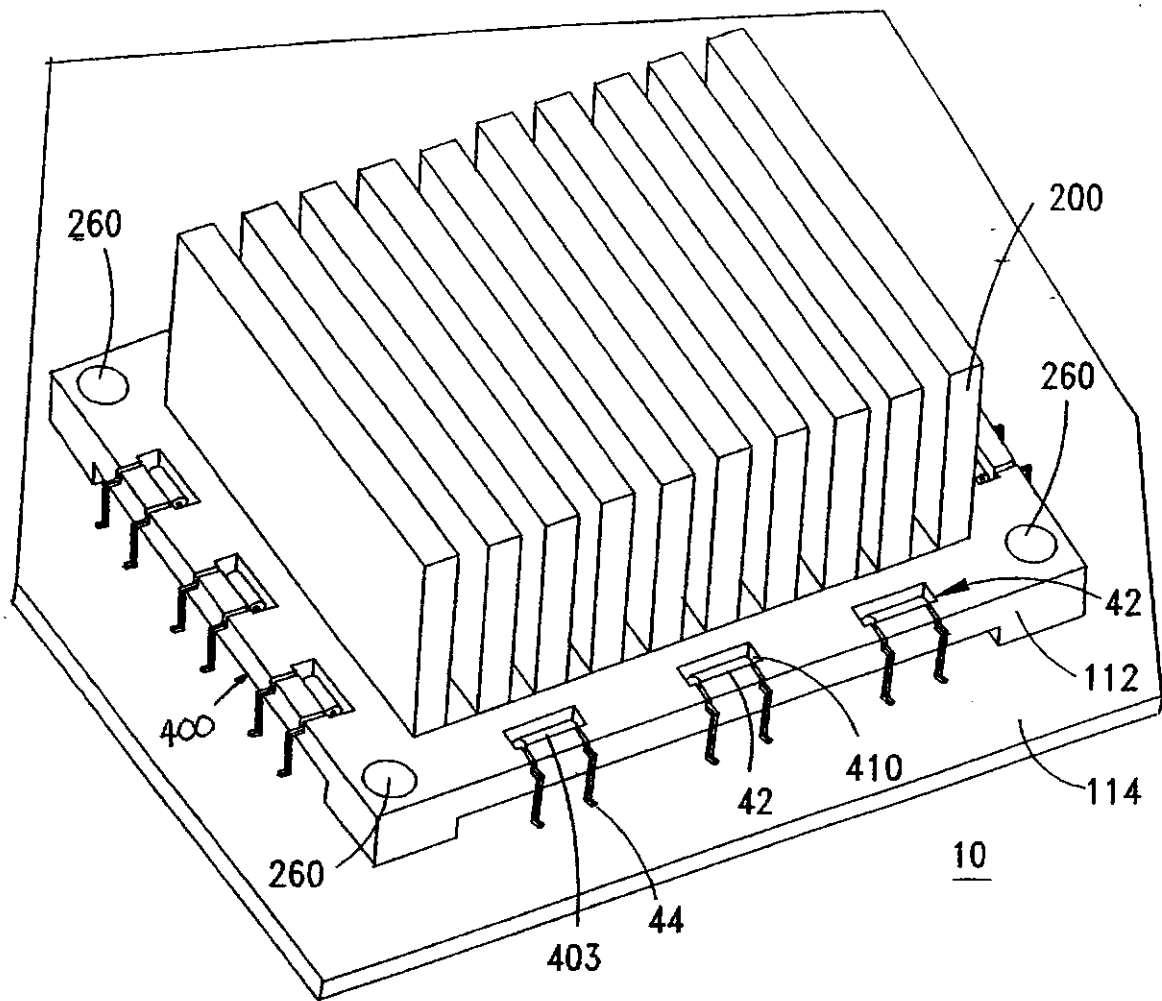
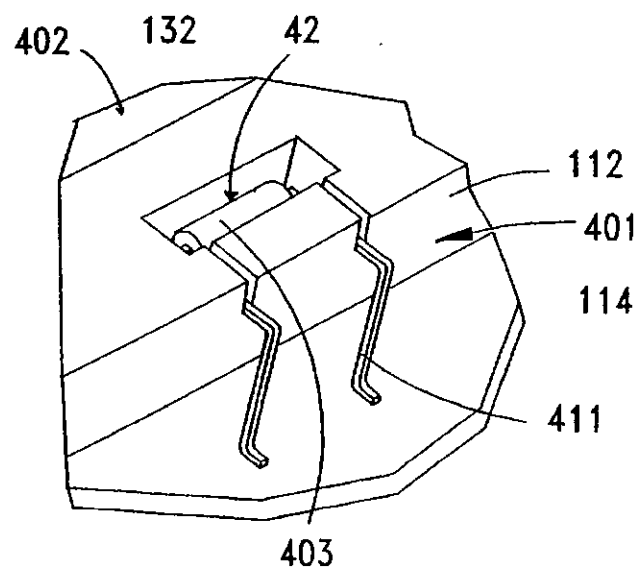


FIG.47

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**FIG.48**

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FIG.49

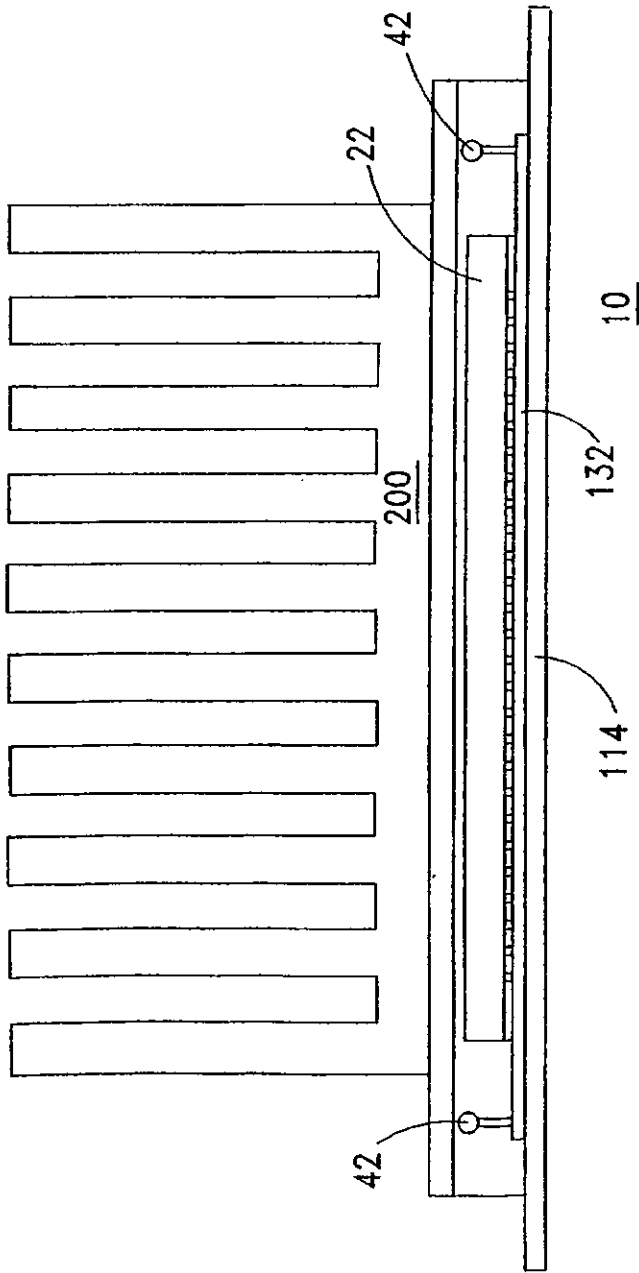
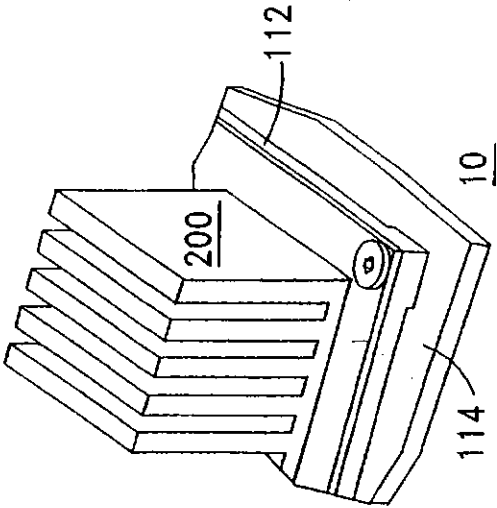


FIG.50



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FIG. 51

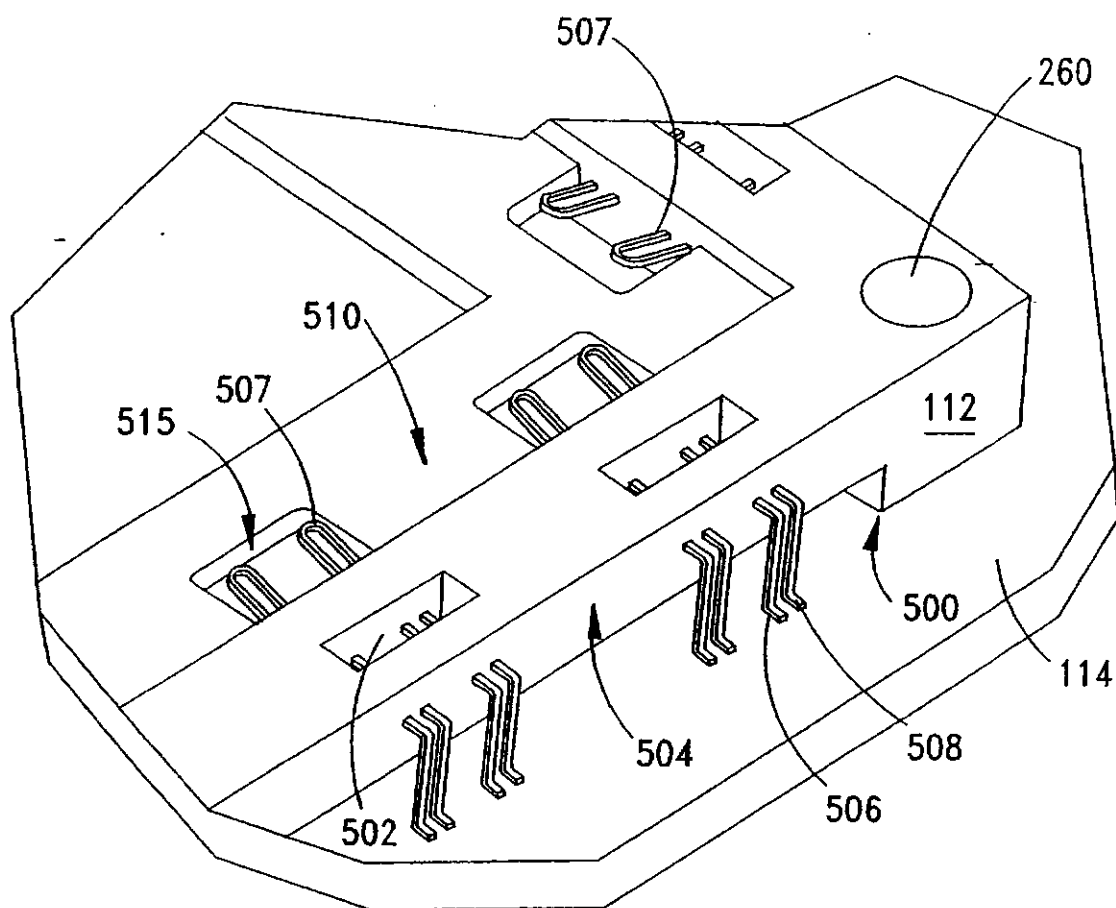
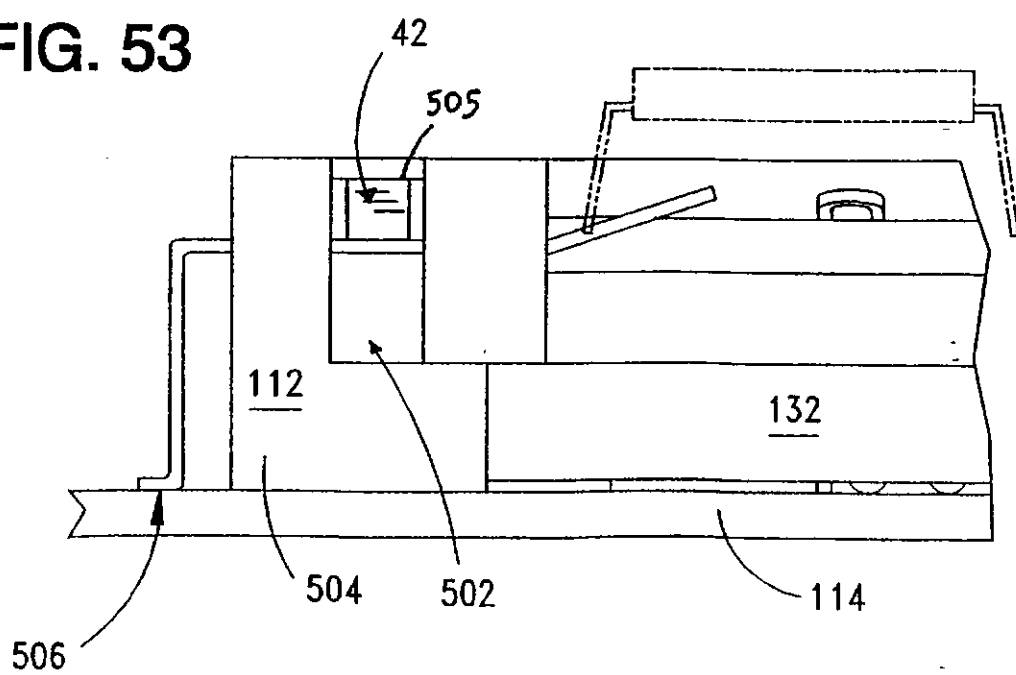
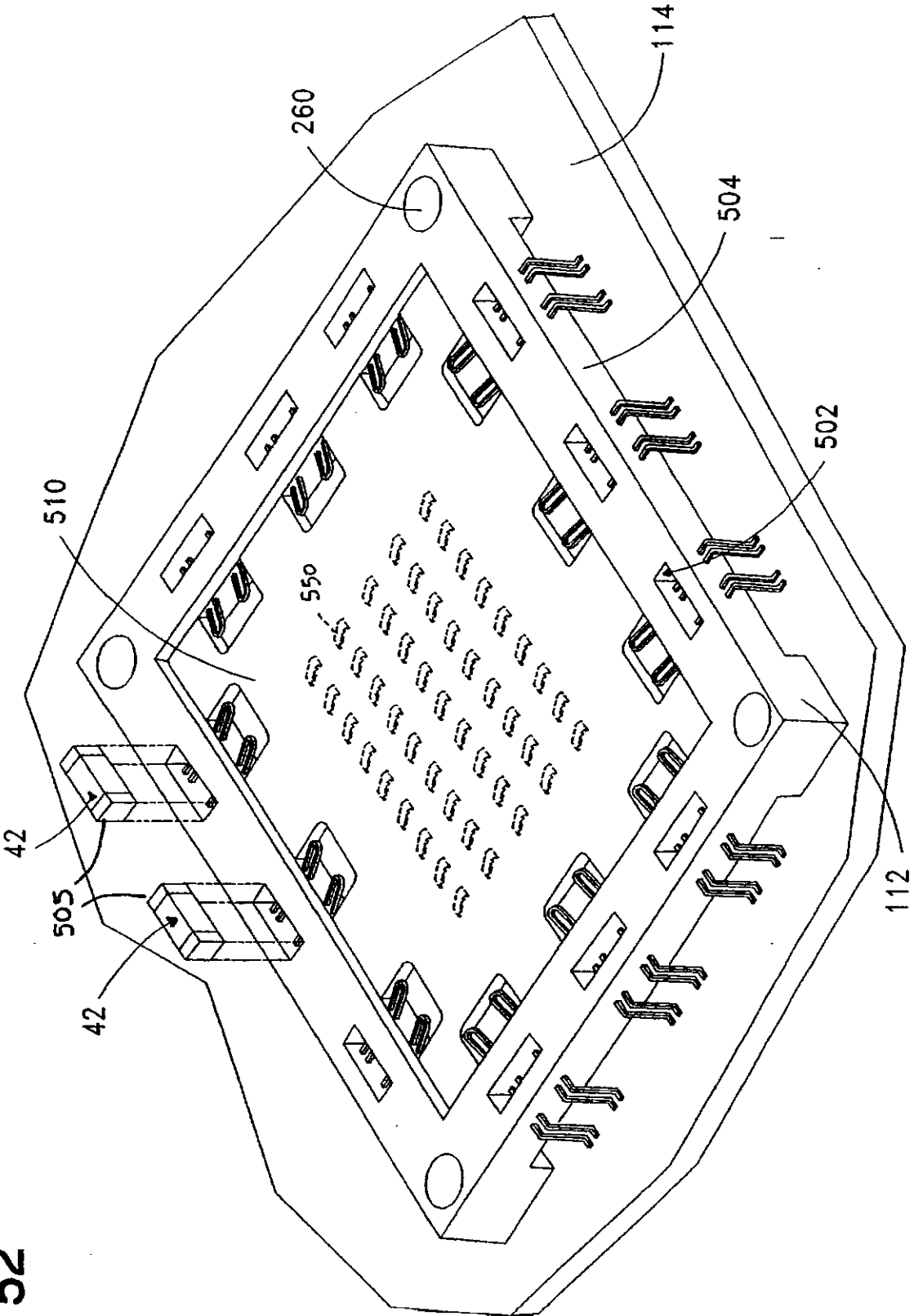


FIG. 53



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FIG. 52



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FIG. 54

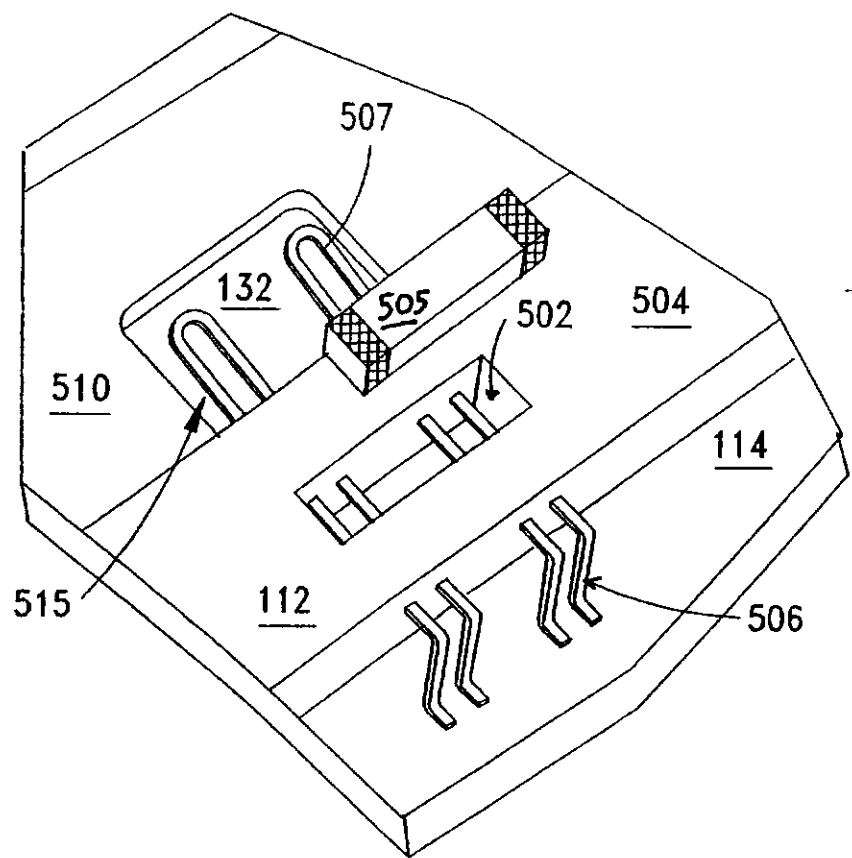
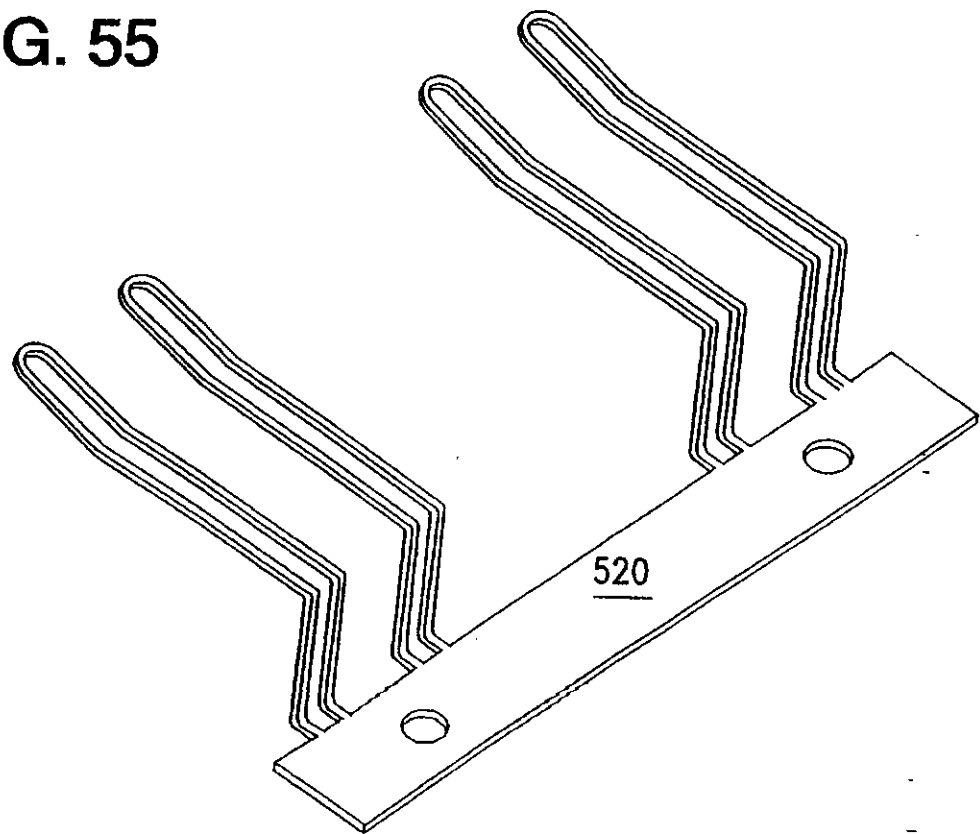


FIG. 55



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FIG. 56

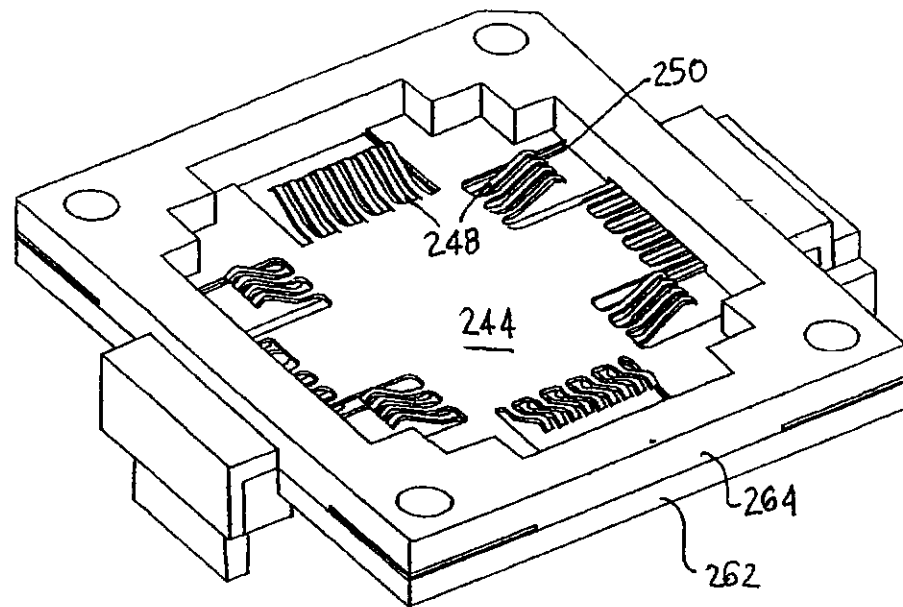
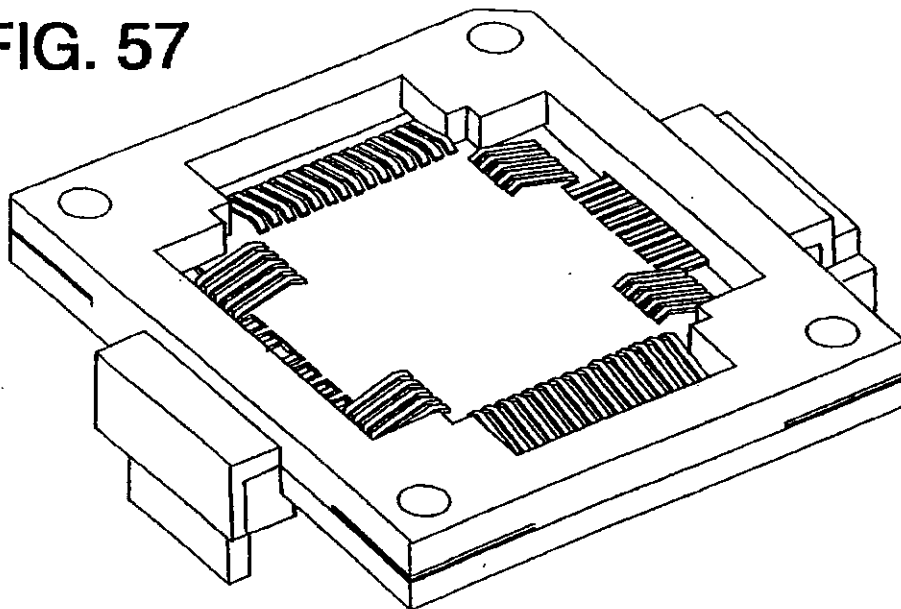


FIG. 57



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FIG. 58

