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BALANCED CAPACITANCE LEAD FRAME FOR INTEGRATED CIRCUITS

TECHNICAL FIELD OF THE INVENTION

This invention relates to integrated circuits, and more particularly relates to a lead frame having balanced capacitance for use with integrated circuitry packaging.

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BACKGROUND OF THE INVENTION

Various techniques have heretofore been used to package integrated circuits. For example, various configurations utilizing lead frames to connect integrated circuits have been developed, such as the flip chip design and the small outline J lead (SOJ) packaging techniques. In many of these prior techniques, the integrated circuit is mounted upon a pad provided by a lead frame, and wire bonds connect from the integrated circuit to conductive leads on the lead frame.

More recently, an integrated circuit packaging technique termed the lead on chip (LOC) technique has been developed. As described in the article entitled Volume Production Of Unique Plastic Surface-Mount Modules For The IBM 80-ns 1-Mbit DRAM Chip By Area Wire Bond Techniques by William C. Ward, published at the 38th ECC in 1988, this technique disposes a lead frame over the active area of an integrated circuit. Adhesive insulating tape connects the lead frame over the integrated circuit, and wire bonds connect the circuit directly to the power buses on the lead frame or jumper over the power buses to conductive leads to provide the correct signal routing. The ability to jump wires over various lead frame leads provides significant advantages by allowing alterable package I/O without chip redesign, since the wires can readily be routed over various buses or leads similar to conventional wire bonding as done on direct chip attached circuit cards.

While prior packaging techniques have worked well in practice for many designs, with the advent of more complex and smaller scale integrated circuits, it has

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become important to obtain equal loading capacitances for the input leads on the integrated circuit package. The provision of equal capacitances for various conductive leads is particularly significant for LOC applications, since the lead frame is separated from the active integrated circuit by a layer of dielectric. The requirement of equal capacitances for the conductive input leads has also become more important with the advent of large dynamic random access memory (DRAM) circuits such as the 16 meg DRAM. In such circuits, it is important that each address line has the same loading capacitance as the adjacent line in order to enhance the operational speed of the DRAM. Moreover, a need has arisen in the LOC package technique to provide additional noise shielding, which is particularly important in LOC devices because of the non-uniform metal closely adjacently disposed to the integrated circuit.

A need has thus arisen for a lead frame and integrated circuitry packaging technique which provides equal capacitances to all lead conductors associated with the integrated circuitry, while maintaining a high degree of noise shielding thereto.

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SUMMARY OF THE INVENTION

In accordance with the present invention, disadvantages and problems associated with previously developed packaging techniques have been substantially reduced or eliminated by use of the present packaging invention. An integrated circuit is encapsulated in an insulating package, with conductive leads extending from portions of the integrated circuit to the external of the package. Each of the conductive leads has substantially the identical capacitance as the remaining conductive leads.

In accordance with another aspect of the invention, a lead frame is provided for integrated circuitry which includes a plurality of elongated conductive leads extending in a side-by-side relationship. The first ends of the leads are dimensioned to be connected to an integrated circuit and the second ends of the leads are dimensioned to provide electrical connection to external circuits. The geometrical area of each of the leads are substantially identical such that the capacitance of each of the leads is substantially identical.

In accordance with yet another aspect of the invention, a lead frame is constructed by providing openings in a sheet of conductive material which define two groups of conductive leads separated by at least one power bus. Each group of the conductive leads includes a plurality of elongated leads extending in a side-by-side relationship normally to the power bus. The geometrical area of each of the leads is substantially identical such

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that the capacitance of each of the leads is substantially identical.

In accordance with a more specific aspect of the invention, each of the conductive leads has a trapezoidal configuration, the geometric area of the trapezoidal configuration of each of the leads being substantially identical to the remaining leads.

In accordance with yet another aspect of the invention, at least one power bus is associated with the integrated circuitry. Portions of the power bus are oriented adjacent ones of the conductive leads and are provided with substantially identical geometric areas as the conductive leads in order to act as dummy leads to ensure equal capacitance of the remaining leads.

In accordance with another aspect of the invention, a conductive layer is disposed adjacent an insulating layer which separates the lead frame and the integrated circuitry in order to provide noise shielding to the integrated circuitry.

In accordance with yet another aspect of the invention, a method of forming an integrated circuit package includes disposing a conductive lead frame adjacent active portions of integrated circuit. The conductive lead frame is insulated from the integrated circuit. Portions of the integrated circuit are selectively interconnected with portions of the lead frame. The lead frame is configured and oriented such that individual conductive leads have substantially identical capacitances. A conductive layer may be provided to provide noise shielding to the integrated circuit.

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BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIGURE 1 is a top view of the lead frame of the present invention;

FIGURE 2 is a perspective, exploded view of the lead frame of the invention showing the adhesive tape and integrated circuit;

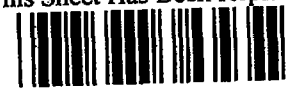
FIGURE 3 is a top view of the lead frame of the invention showing the connection of the integrated chip thereunder;

FIGURE 4 is a top view of the lead frame of the invention showing wire bonds from portions of the integrated circuit to ones of the conductive leads of the lead frame;

FIGURE 5 is a side view of the completed integrated circuit package; and

FIGURE 6 is a perspective view, partially broken away, of a completed integrated circuit package utilizing the present invention.

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DETAILED DESCRIPTION OF THE INVENTION

Referring to FIGURE 1, a lead frame 10 of the present invention comprises a metal sheet which may be formed of, for example, full hard temper CDA alloy 151 which may be approximately .008 in. in thickness and which may be spot plated in gold, silver, or the like. The metal sheet has a plurality of cutouts stamped therein to define a lead configuration. Specifically, the lead configuration comprises a pair of power buses 12 and 14 which comprise elongated parallel conductive lines suitable for receiving electrical power. A first group of conductive leads 16 is disposed generally normally to the power bus 12, with leads 16 being arranged in a side-by-side relationship. Similarly, a second group of conductive leads 18 is disposed generally normally to the power bus 14, with the leads 18 arranged in a side-by-side relationship. While it will be understood that different numbers of conductive leads may be provided in dependence upon the integrated circuitry, in the illustrated embodiment, ten conductive leads comprise the first group 16 and ten conductive leads comprise the second group 18. Conductive leads 16 and 18 are utilized to provide input and output signals to the associated integrated circuit.

End portions of power bus 12 extend normally to the center portion of the power bus 12 and are identified as dummy or false leads 20. Similarly, end portions of power bus 14 extend generally normally to the central portion of power bus 14 and are generally identified as dummy or false leads 22. Each of the power buses 12 and 14 also include center extensions 24 and 26. As will be subsequently described in greater detail, these center bus

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extensions 24 and 26 operate as dummy or false conductive leads to assist in maintaining equal capacitance of neighboring conductive leads.

An important aspect of the present invention is that each of the conductive leads 16 and 18 are formed with a substantially identical geometric configuration. In this way, each of the conductive leads 16 and 18 have substantially identical capacitances.

Cutouts in the lead frame sheet also define a first group 28 of lead extensions and a second group 30 of lead extensions. As will be subsequently described, these lead extensions 28 and 30 are partially cut or trimmed away during final assembly of the integrated circuit package. Support bars 32 and 34 are provided on opposite ends of the wire frame in order to provide added support to the encapsulated package.

Locking extensions 32a and 34a are provided to enable locking of the support bars 32 and 34 within the plastic encapsulation to ensure integrity of the package.

In order to better understand the inventive concept wherein equal capacitances are provided to each of the conductive leads, conductive lead 36 will now be described in greater detail. Lead 36 is comprised of three different sections. The first section 36a is spaced apart from and oriented normally to the central power bus 12. The second or middle portion 36b of the lead is angled away from normal to the power bus 12 and has a trapezoidal cross-sectional area. The third section 36c of the lead is disposed normally to the central power bus 12. As will be subsequently described, section 36a of the lead is used to receive wire bonding to an active portion

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of the integrated circuit located below the lead. Section 36c of the lead extends from the integrated circuit package and is used to make physical contact with exterior circuitry. Locking notches 36f are provided in the conductive lead 36 to enable secure locking of the conductive lead within the encapsulation plastic in subsequent encapsulation steps to be described.

An important aspect of the present invention is that each of the conductive leads 16 and 18 have substantially identical cross-sectional areas as lead 36. As may be seen from the drawings, each of the first sections of the leads which correspond to section 36a are rectangular and have the identical cross-sectional area. Similarly, each of the trapezoidal areas corresponding to section 36b have substantially identical cross-sectional areas. An important aspect of the invention is that each of the mid sections of the conductive leads which form the trapezoidal areas have identical length upper and lower bases which form the trapezoidal area. Specifically, the base 36d of lead 36 is identical in length as the corresponding bases for all other conductive leads on the lead frame. Similarly, the base 36e forming the lower base of the trapezoidal area has an identical length as all other corresponding bases in the remaining conductive leads. It may also be seen that the heights of the trapezoidal areas of all the conductive leads 16 and 18 are the same. Since trapezoids with equal bases and equal heights have equal areas, the present invention provides an easy technique to ensure that all mid areas of the conductive leads are equal. Similarly, it may be seen that the areas of each of the third sections 36c of the

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conductive leads are identical. Since the geometrical areas of each of the conductive leads is identical, the capacitance of the leads will be found to be substantially identical.

An important aspect of the present invention is the provision of the trapezoidal mid-sections of the conductive leads which enable the leads to diverge from normal to accommodate sufficient size external lead pads to ensure adequate electrical contact with exterior circuits. Specifically, it may be seen that the top five conductive leads forming group 16 diverge from normal in an upward angle, while the bottom five conductive leads forming group 16 diverge from normal at a downwardly oriented angle. Similarly, the first five conductive leads forming group 16 diverge from normal at an upward angle, while the bottom five leads diverge from normal at a downward angle. The unique geometry of the conductive leads enables this divergence without a change in geometrical area and resulting capacitance.

Another important aspect of the invention is the provision of the dummy or false leads 20 and 22 as well as the center bus extensions 24 and 26 which form dummy or false leads. Without these dummy or false leads, certain of the conductive leads of the invention could have differing capacitances than their neighbors, because such leads were not surrounded on both sides with identically shaped leads. With the provisions of the identically shaped dummy or false lead extensions 20-26 from the power buses 12 and 14, neighboring conductive leads may be provided with identical capacitances. For example, without dummy or false lead 20, conductive lead 36 would

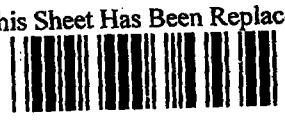
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have only its lower neighbor conductive lead closely associated therewith. However, with the provision of the upper dummy lead 20, which is provided with an identical shape to conductive lead 36, lead 36 is surrounded on both sides by identical leads.

Similarly, the center bus extensions 24 and 26 operate to provide equal capacitance to their neighbor leads. As may be seen, extensions 24 and 26 are of identical construction and each have a Y configuration. Referring specifically to extension 24, the Y configuration includes a leg 24a and 24b. It may be seen that each of the legs 24a and 24b are identical in construction and that they have substantially the same trapezoidal configuration as the mid portions of the two adjacent conductive leads. The legs 24a and 24b do not extend as far outwardly from power bus 12 as do the conductive leads, since the legs 24a and 24b will not extend outside of the hermetically sealed package. Locking notches 24c are provided in each of the legs in order to maintain the substantially identical geometric area, to ensure that the neighboring conductive leads see a substantially identical conductive mass to ensure that substantially identical capacitance is maintained in those adjacent conductive leads.

The Y shaped configuration of the extensions 24 and 26 enable equal capacitance to be provided to the conductive leads of the invention, even with the diverging orientation of the leads as previously described. In some cases, a small capacitance imbalance may be initially provided because the geometries of the legs 24a and 24b are not identical with those of the neighboring conductive

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leads. However, this imbalance may be nullified by carefully selecting the length of the legs 24a and 24b to provide the desired exact capacitance balance.

FIGURE 2 illustrates a perspective exploded view of the connection of the lead frame 10 to an integrated circuit 40. Integrated circuit 40 may comprise any suitable type of integrated circuit for use with a lead frame 10, but it has been found particularly advantageous to use the present lead frame with integrated circuits such as DRAMs. In particular, because of the extreme complexity and small dimensions associated with circuits such as the 16 meg DRAM, the present invention is particularly adaptable for use with such complex circuits.

In accordance with the invention, two pieces of double-sided adhesive 42 and 44 are disposed over the top of the integrated circuit 40 and attach the lead frame 10 over the top of the integrated circuit 40. It is this configuration which leads to the description of the lead over chip (LOC). The use of the double-sided adhesive 42 and 44 is known, and the adhesive may comprise, for example, a double-sided thermosetting epoxy adhesive coated polyimide film which also acts as an active barrier. The integrated circuit 40 and the lead frame 10 form a self supporting structure. The power buses 12 and 14 and the conductive leads 16 and 18 provide for highly efficient central distribution of voltage, ground and control signals. The power buses 12 and 14 and conductive leads 16 and 18 are laminated directly over the primary heat generating circuits of the integrated circuit, thus optimizing heat dissipation.

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When the lead frame 10 is affixed over the integrated circuit 40 in the manner shown in FIGURE 2, the resulting configuration will appear as shown in FIGURE 3, which comprises a top view of the finished subassembly. The power buses 12 and 14 comprise spaced apart parallel conductive buses which run along the middle of the integrated circuit 40. The adhesives 42 and 44 are spaced apart such that active portions of the integrated circuit 40 are exposed for bonding to the conductive leads of the invention as will be subsequently described. Again, the identical configuration of the conductive leads 16 and 18 may be seen, which provides the substantially identical capacitance provided by the invention.

Referring to FIGURES 2 and 3, another important aspect of the invention may be understood. Because of the irregularity of metal disposed over the integrated circuit 40, certain circuits within the integrated circuit 40 are subject to noise. It has been determined that the provision of a conductive layer associated with the adhesives 42 and 44 serves to substantially shield the integrated circuit from the non-uniform leads of the lead frame. In accordance with the invention, a layer of conductive metal such as copper may then be placed on the sides of the adhesives 42 and 44 away from the integrated circuit 40. Adhesive may then be deposited over the metallic layer for connection to the underside of the lead frame 10. Substantial noise shielding is thus provided by the conductive layer associated with the bonding adhesives 42 and 44.

After the lead frame 10 has been connected to the integrated circuit 40 by adhesives 42 and 44, the

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subassembly is laminated under suitable temperature and pressure conditions and is then oven cured to fully cross-link the adhesive.

FIGURE 4 illustrates the next stage of assembly of the present invention wherein high speed thermosonic gold ball wire bonding is accomplished. While it will be understood that various types of wire bonding may be utilized with the invention, bonding using 0.001 in. diameter gold wire has been successfully accomplished. As noted, the gold wire bonds selected portions of the integrated circuit 40 to selected portions of the power buses 12 and 14 and to the conductive leads 16 and 18. For example, wire lead 50 connects the integrated circuit to power bus 12, while wire lead 52 bonds the integrated circuit to one of the conductive leads 16. It will be understood that the wire bonding scheme will vary depending upon the particular configuration of the integrated circuit 40 used with the invention.

After testing of the wire bond ball connections by suitable shear and pull tests, transfer molding of the invention with a molding compound is conducted. While different molding compounds are usable with the present invention, a Novolac epoxy mold compound has been found to work well to encapsulate the entire integrated circuit device. Because of the complexity of the circuitry, low stress mold techniques are utilized. The molded device is then cured, deflashed and lead preparation is conducted on the external leads. The leads are then trimmed and formed by bending to produce the nearly finished product depicted in FIGURES 5 and 6.

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FIGURE 5 illustrates an end view of the substantially finished product wherein the integrated circuit 40 may be seen encapsulated within a plastic body 56. Conductive leads 16 and 18 are shown extending from over the integrated circuit 40 and adhesives 42 and 44 to external of the molded plastic body 56. Leads 16 and 18 are bent for suitable physical and electrical contact with external circuitry. Wire bonds 50 and 52 may be seen connecting portions of the integrated circuit 40 with the leads 16 and 18.

FIGURE 6 illustrates in perspective a partially cut away view of the finished semiconductor package. The plastic encapsulation totally surrounds the integrated circuit 40 and all portions of the adhesives 42 and 44. FIGURE 6 illustrates clearly the side-by side symmetrical relationships of the lead conductors 16 and 18. It may be seen that the geometry and shape of each of the twenty conductive leads 16 and 18 are substantially identical to one another and that the trapezoidal middle section of the conductive leads enables the leads to diverge from one another while yet maintaining identical geometry. It may also be seen how the dummy or false leads 20-22 act to balance the capacitance of the end conductive leads. FIGURE 6 further illustrates the center bus extensions 24 and 26 and shows how the geometry of the Y shaped legs of the extensions 24 and 26 operate as dummy or false leads to balance the capacitance of the diverging neighboring conductive leads.

Again, the provision of the metallic coating on the adhesive tapes 42 and 44 tends to isolate the elements on the integrated circuit 42 from electrical disturbances

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in the lead frame 10. The resultant symmetry of the present lead frame design and the addition of the dummy or false leads from the power buses improves the thermal dissipation and lowers thermal or temperature gradients of the packaging system, thus allowing a greater number of and more evenly distributed thermal paths.

An important aspect of the invention is that by balancing the capacitance in the manner described above, the equality of loading capacitance between signal leads is maintained at all lead frame heights above the surface of the integrated circuit 42. In other words, it is possible to provide the conductive leads 16 and 18 with upsteps or downsteps at any arbitrary line parallel to the edge of the integrated circuit package. In this manner, the conductive leads may be stepped up or down as needed in order to control the total loading capacitance of the package, while maintaining the equality of capacitance between the individual conductive leads. Moreover, the up or down setting of the leads enables accurate control of the thermal dissipation properties of the package and the stress distribution of the package. The provision of such up or down steps in the conductive leads while maintaining equal capacitance is not available with other designs due to the differing geometries of the neighboring leads.

When the device is fabricated to the stage indicated by FIGURE 6, additional lead finishing with eutectic lead solder dipping, singulation, marking, inspection test and burn-in are required to complete the final product for use.

While it will be understood that the actual dimensions of the lead frame 10 of the present invention

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will vary in dependence upon its intended use, it has been found that a typical width of section 36a (FIGURE 1) may be 0.015 in.while the width of the third section 36c of the conductive lead may comprise .025 in. The total length of a conductive lead 16 or 18 in the preferred embodiment may be 0.3 in. The above-noted dimensions have been found to adequately accommodate an integrated package having the dimensions 340 x 660mm.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

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CLAIMS:

1. A lead frame for integrated circuitry comprising:

a plurality of elongated conductive leads extending in a side-by-side relationship, first ends of said leads dimensioned to be connected to an integrated circuit and second ends of said leads dimensioned to provide electric connections to external circuits;

the geometrical area of each of said leads being substantially identical such that the capacitance of each of said leads is substantially identical.

2. The lead frame of Claim 1 wherein each of said conductive leads has a trapezoidal configuration, the geometric area of said trapezoidal configuration of each said lead being substantially identical.

3. The lead frame of Claim 2 wherein said trapezoidal configuration of each said lead is disposed between said first and second ends of each said lead.

4. The lead frame of Claim 1 and further comprising:

an elongated power bus having a central portion disposed normally to said conductive leads and further having end portions which extend in a side-by-side relationship to said conductive leads, said power bus end portions having substantially identical geometric areas as said conductive leads to act as false neighboring leads to maintain equal capacitance for all of said conductive leads.

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5. The lead frame of Claim 1 and further comprising:

an elongated power bus having a central portion extending normally of said conductive leads and spaced from said first ends of said leads;

an extension from said power bus extending between two groups of said leads in a side-by-side relationship to said leads;

said extension having substantially identical geometric areas as said leads to act as false neighboring leads to maintain equal capacitance for said leads.

6. The lead frame of Claim 1 wherein said conductive leads have an angled mid portion, ones of said conductive leads angled away from others of said conductive leads.

7. The lead frame of Claim 6 wherein said angled mid-portion of said conductive leads forms trapezoidal areas, said trapezoidal areas of all said conductive leads being substantially identical.

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8. A lead frame comprising:

a sheet of conductive material;

openings through said sheet to define two groups of conductive leads separated by at least one power bus;

each group of conductive leads including a plurality of elongated leads extending in a side-by-side relationship normally to said power bus; and

the geometrical area of each of said leads being substantially identical such that the capacitance of each of said leads is substantially identical.

9. The claim of Claim 8 wherein the middle portion of each of said leads has a trapezoidal configuration of identical geometric area.

10. The claim of Claim 8 wherein said power bus includes end portions oriented in a side-by-side relationship to one of said groups of conductive leads, said end portions having substantially identical geometric areas as said conductive leads.

11. The claim of Claim 8 wherein said power bus includes an extension disposed in the middle region thereof, said extension extending normally from said bus between ones of said conductive leads in a side-by-side relationship, said extension having substantially the same geometric area as said conductive leads to act as a dummy lead to insure equal capacitance of said conductive leads.

12. The claim of Claim 11 wherein said extension has a Y shaped configuration, each leg of said Y shaped configuration having the same geometric area as corresponding portions of adjacent conductive leads.

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13. A lead frame for connection to an integrated circuit comprising:

a pair of parallel elongated conductive buses;

first and second groups of conductive leads arranged on opposite sides of said power buses, each said group extending normally away from said power buses;

said conductive leads in each said group being arranged in a side-by-side relationship along the length of said power buses;

the area of each of said conductive leads being substantially identical such that the capacitance of said leads is substantially identical.

14. The apparatus of Claim 13 wherein said integrated circuit is disposed beneath and supports said lead frame, connecting wires electrically connecting areas of said integrated circuit to ones of said power buses and said conductive leads to form an active integrated circuit device.

15. The apparatus of Claim 13 wherein said integrated circuit is separated from said lead frame by a nonconductive layer.

16. The apparatus of Claim 15 wherein said nonconductive layer includes adhesive to bond said lead frame and said integrated circuit.

17. The apparatus of Claim 16 and further comprising a conductive layer over said nonconductive layer to act as a noise shield to said integrated circuit.

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18. The apparatus of Claim 17 wherein each of said conductive leads has a trapezoidal configuration, the geometric area of said trapezoidal configuration of each said lead being substantially identical.

19. The apparatus of claim 13 wherein each of said power buses includes end portions which extend generally normally to the central said power buses and which lie side-by-side with said conductive leads.

20. The apparatus of Claim 13 wherein each of said power buses includes a false lead extension which extends normally from the center of said power buses between ones of said conductive leads, said extension having a Y configuration with leg portions having substantially identical areas as corresponding portions of adjacent conductive leads.

21. The lead frame of Claim 13 wherein each of said conductive leads includes a first end portion adjacent and normal to one of said power buses; and

each of said conductive leads further including a central portion angled from normal and further including a second end portion remote from said power buses and extending normally to said power buses.

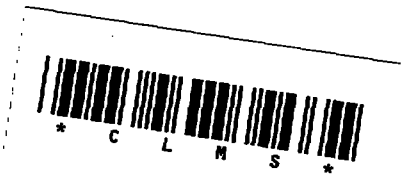
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22. The lead frame of Claim 21 wherein said central positions of said conductive leads have a trapezoidal configuration, the trapezoidal bases of each of said conductive leads being equal in length to ensure said trapezoidal configuration of each conductive lead is substantially equal in area.

23. The lead frame of Claim 21 wherein said central portions of one-half of said first and second groups of conductive leads extend at diverging angles to the remaining one-half of said conductive leads in each said group.

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24. An integrated circuit device comprising:

an integrated circuit encapsulated in an insulating package;

conductive leads extending from connections to portions of said integrated circuit to external of said package;

each of said conductive leads having substantially identical capacitance as the remaining conductive leads.

25. The integrated circuit device of Claim 24 and further comprising:

at least one power bus extending adjacent said integrated circuit and said conductive leads;

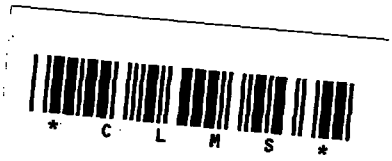
said power bus including extensions oriented adjacent said conductive leads to act as false leads to maintain equal capacitance of each of said conductive leads.

26. The integrated circuit device of Claim 24 and further comprising:

an insulating layer disposed between said integrated circuit and said conductive leads; and

a conductive layer disposed on said insulating layer to provide noise shielding to said integrated circuit.





27. An integrated circuit device comprising:

an integrated circuit;

a lead frame for being disposed adjacent an active side of said integrated circuit;

connecting wires interconnecting portions of said integrated circuit to portions of said lead frame;

said lead frame including a plurality of conductive leads arrayed in a side-by-side relationship along at least one side of said integrated circuit;

said conductive leads having substantially identical geometric areas to provide substantially identical capacitances to said integrated circuit.

28. The integrated circuit device of Claim 27 wherein said integrated circuit comprises a dynamic random access memory.

29. The integrated circuit device of Claim 27 wherein each of said conductive leads has an angled portion which defines a trapezoid, the areas of the trapezoids of said conductive leads being substantially identical.

30. The integrated circuit device of Claim 27 and further comprising at least one power bus extending substantially along the length of said integrated circuit, said power bus including false lead extensions which lie adjacent ones of said conductive leads to ensure that said conductive leads have substantially identical capacitances.

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31. The integrated circuit device of Claim 30 wherein said false lead extension comprises the end portions of said power bus.

32. The integrated circuit device of Claim 30 wherein said false lead extension comprises a centrally located extension from said power bus.

33. The integrated circuit device of Claim 32 wherein said centrally located extension has a Y configuration, each leg of said configuration having a substantially identical area as the corresponding area of a neighbor conductive lead.

34. The integrated circuit device of Claim 27 wherein ones of said conductive leads are angled away from others of said conductive leads.

35. The integrated circuit device of Claim 27 and further comprising a conductive shield formed between said integrated circuit and said lead frame to provide noise shielding.

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