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ABSTRACT

HIGHLY SELECTIVE AND COMPLETE INTERCONNECT METAL LINE AND VIA/CONTACT HOLE FILLING BY ELECTROLESS PLATING

A novel method for the activation of semiconductor substrates for highly selective electroless copper plating in multilayer interconnect metallization lines and vias/contact holes has been developed. A copper-seeded polysilicon layer is provided over the substrate to facilitate growth of copper into the vias. Subsequent rinsing and chemical-mechanical polishing processes allow removal of overgrowth of copper and the polysilicon layer to achieve overall smooth topography of the copper surface and the insulating layer surface of the substrate.

Figure 3 is to be published.