Description:

Brief description of prior art:
Lighting circuit are largest wired network in the building. Control signal can send through lighting network to control any device in the building.
To control and monitor the lights in the building is importance application of this invention. There are various method to control the lights or loads.

a. Power Line Carrier (PLC) method: Refer to **Fig 1.**
Main controller **102** and device under control **103** all are equipped with PLC modem **101.** Control signal from main controller are fed to PLC modem. Power line carrier signal then fed to a.c. supply cable to the device under control. PLC modem in the control device then recovers the control command and sends to device controller.
The drawback of this system is PLC modem **101** subject to line noise interference and expensive. Not economically when apply to control the lightings. The application normally limit to short distance control.

b. Two wire phase control (analog): Refer to **Fig 2.**
Device under control **206** are connected in series with main controller **201.** main controller **201** pulse width modulate the a.c. supply to all device **206** under control. Phase detector **205** detect the pulse width and fed this info to control the device. The depth of control is proportional to the width of the detected pulse. **203** and **204** are 50% and 90% dimming control a.c. supply waveform respectively.
Generate high harmonic content in power supply system when dimming more than 30%.
Precise light brightness control is difficult. The reason is the recover pulse width vary when line supply amplitude change. This means that same percentage dimming pulse width control from main controller might result in different light brightness when supply voltage fluctuated or the load change from resistive to inductive when light is dimmed.

c. Three wire phase control: Refer to **Fig 3.**
Control method similar to b) above except control signal are send through separate live wire. Main controller **301** pulse width modulate a.c. are fed to separate live wire **302** and connect to all device under control **303.** Because control signal are send through separate live wire. No high harmonic content generated problem in power supply as b) above.
Drawback of this system is need to run additional wire **302** to every device under control **303**. System will be costly. Recover pulse width also subject to line voltage variation as b) above.

d. Separate control wire: Refer to **Fig 4.**
Main controller **401** and device under control **404** are equip with modem **402.** Modem connect to separate pair of control wire **403**. This system offer 2 way communication between controller and device under control.
Drawback of this system is need to run separate pair control wire **403** from controller **401** to every device **404** under control. System cost very high.

e. Two wire phase control (digital): Refer to **Fig 5.**
All device under control **504** are connect in series with controller **501**. A.C. supply **502** fed to controller **501**. Controller pulse modulate output from Triac then fed the phase modulated a.c. to all device under its control **504** down stream. **503** is the pulse modulate waveform output from Triac .
Comparator **506** in device under control **504** recover modulated pulse. As shown waveform **505.**
Recovered pulse then fed to integrator circuit **507** to eliminate the narrow pulse and noise. Integrator output is the modulated pulse. In theory this method should recover all the modulated pulse perfectly. But in practice there are line voltage variation and inductive load cause pulse width vary and d.c. voltage superimpose on the recover signal before comparator. (after full wave rectifier and attenuator circuit). Thus cause modulated pulse and interference pulse width some time different very little. Integrator circuit might not be able to differentiate it and thus cause error signal received.
Drawback of the system is when line supply voltage vary +/- 15% might cause recover pulse error. When the load is inductive. After full wave rectifier there is d.c. offset voltage exist. This d.c. offset voltage is superimpose on the rectified a.c. signal. Which might cause recover pulse error. Inductive load cause

error pulse recover is more serious. This system don't have method to track the line voltage variation and inductive load cause d.c. voltage superimpose after full wave rectifier.

f. Brief description of prior art drawing:

Fig 1. Illustrates a communication in accordance Power Line Carrier (PLC) method.
Fig 2. Illustrates a communication in accordance Two Wire Phase Control (analog)
Fig 3. Illustrates a communication in accordance Three Wire Phase Control
Fig 4. Illustrates a communication in accordance Separate Control Wire
Fig 5. Illustrates a communication in accordance Two Wire Phase Control (digital)

Object of the invention:

Provide reliable and low cost control method from transmitter (or controller) to devices under control downstream. Invention keep track of line voltage variation and inductive load causes recover pulse width vary. System auto adjust and compensate the recover pulse width variation cause by line voltage variation and load change from resistive to inductive and retrieve the control command.
System provide up to 240BPS (60Hz supply) or 200BPS (50Hz supply) from controller to device under control.
When severe line distortion or noise present in the supply line. System automatically reduce the communication baud rate to 120 BPS (60 Hz supply) or 100 BPS (50 Hz supply).

Summary of the invention

System consists of transmitter (or controller) **701** and receiver **801** two portions.
In accordance to the invention. Control command from transmitter to receiver contains series of '0' and '1' is breakdown into basic 4 stage data '00' '01' '10' and '11' (**Fig 7** waveform **713** and **714**). Triac is phase modulate by 4 stage data '00', '01', '10' and '11'. This 4 stage data is converted to precise fixed time delay T0, T1 **707a**, T2 **707b** and T3 **707c** respectively by CPU **705.** Time delay of T0 for data '00' is zero. This time delay data then fed it to Triac or SCR triggering circuit **706** to pulse width modulate the Triac or SCR **712** immediately after zero crossing **704** of supply is detected.
Pulse width modulation is close to zero crossing point of the supply. Time delay data cause delay triggering of Triac or SCR **712** after zero crossing point. '00' data trigger the Triac or SCR immediately after zero crossing. '01' '10' and '11' data cause delay triggering of Traic or SCR (**refer to Fig 9**) T1 **707a** , T2 **707b** and T3 **707c** respectively. Delay triggering time will be T1, T2 and T3 respectively. Duration of T3 **707c** is longest. Pulse width modulated a.c. supply **708** only transmit to those receiver **801** and load **812** located downstream of controller. No power isolation is requiring. The format of data transmit from transmitter to receiver is 'preamble + synchronous + command'.
Receiver **801** in the control device recover the phase modulated data and fed it to comparator , anti jittering and noise filter circuit **810** then send to microprocessor **811** to process it. Transmitted data contains the pulse width of '00', '01', '10' and '11' info as preamble prior the actual control command. Microprocessor retrieves the 4 stage '00' to '11' pulse width info first and use it as reference value to retrieve and re-structure the following synchronous and control command data.
Line supply voltage normally fluctuates slowly. It might vary +/- 15% over 24 hours. In very short duration. A.C. supply voltage can consider very stable.
Data transmit from transmitter to receiver take less than 1 second. Any line voltage variation and inductive load variation in 1 second period can consider negligible. The recover pulse width of preamble, synchronous and following control command affect by supply voltage and load variation are the same.
Microprocessor can easily recover control command with the reference pulse width of '00' to '11' contain in preamble.

Brief description of the invention drawings

Fig 6. Illustrates a communication in accordance with the present invention.
Fig 7. Illustrates the transmitter and respective point waveform
Fig 8. Illustrates the receiver and respective point waveform
Fig 9. Illustrate relationship of waveform from transmitter to receiver
Fig 10 Illustrate with fix pulse width modulation the relation of line voltage vary cause recover pulse width Change.

Detail description of the invention

Fig 6 shown the system diagram of the invention. System consists of transmitter or controller **701** and Triac or SCR **712.** Receiver **801** and Load **812.**

1. Transmitter

Refer to **Fig 7** the system block diagram of transmitter or controller **701.** Microprocessor **705** in transmitter **701** re-arrange the command signal (series of '0' or '1')data bit **713** according to '00' '01' '10 and '11' pattern **714.** CPU then convert '00' '01' '10' and '11' data to fixed time delay pulse**707.** For data '00' Triac was trigger without time delay (T0 is zero) after zero crossing is detected. . For data '01' triggering delay pulse is T1 **707a.** and for data '10' and '11'delay triggering time will be T2 **707b** and T3 **707c** respectively. T3 is longest time delay to trigger Triac or SCR. T2 is second longest, T1 is shortest and T0 trigger Triac or SCR immediately. Microprocessor send out precisely time delay triggering pulse **707** to triggering device **706** immediately after zero crossing of line voltage **710** which is detected by zero crossing detector **704.** Precisely time delay pulse from trigger circuit **706** then fed to trigger Triac or SCR **712.** Delay triggering of Triac or SCR after zero crossing pulse detected is depends on whether the command data is '00', '01', '10' or '11'. A.C. supply (as shown waveform **708)** after Triac or SCR is send to downstream devices **801, 812.** Control command are send from controller to downstream device **801 812.** The duration of transmission is less than 1 second. The format of data transmit from transmitter to receiver is 'preamble + synchronous + command'. The transmission baud rate is 240 BPS (for 60 Hz supply) or 200 BPS (for 50 Hz supply).
Waveform **709** shown the load is resistive. **710** is the waveform shown the load is inductive.

2. Receiver and load under control.

Refer to **Fig 8** the system block diagram of the receiver **801** and load **812.**
A.C. output from transmitter or controller as shown waveform **802** are fed to receiver **801** and load **812.** The output of full wave rectifier **806** as shown in waveform **803** then fed to zener diode **808** and to attenuator **807.** The function of the zener diode **808** are use to offset the floating voltage after rectifier cause by inductive load. Attenuator output then fed to comparator and filtering circuit **810** and compares it with fixed reference voltage **815.** Diode **809** protect the comparator when the attenuator **803** output to comparator **810** exceeds the supply voltage Vcc **813. 804** is the output waveform of comparator and filtering circuit **810.**
The recover pulse width at comparator and filtering circuit **810** output is proportional to data '00' to '11'. Comparator and filtering circuit **810** output then fed to CPU circuit **811.** CPU first retrieve the '00' to '11' information contained in the preamble and use it as reference pulse width of '00' to '11' signal.
Pulse width of preamble data recover by receiver will be T4 **804a,** T5 **804b,** T6 **804c** and T7 **804d.** Which represent the data bits '00' '01' '10' and '11' respectively.
Receiver CPU **811** compares the following synchronous and command data pulse width with T4 **804a,** T5 **804b,** T6 **804c** and T7 **804d** and retrieve as below method.
If the recover pulse width less than T4 + (T5 – T4)/2 then the received data is "00".
If pulse width less than T5 + ((T6 – T5)/2 and more then T4 + (T5 – T4)/2 then the received data is "01".
If pulse width less than T6 + (T7 – T6)/2 and more then T5 + (T6 –T5)/2 then the received data is "10".
If pulse width more than T6 + (T7 – T6)/2 then the received data is "11".
CPU **811** then re-structure the retrieve '00' to '11' data back to actual control command format. CPU **811** then control the load **812** according to the control command instruction. E.g. to switch on or switch off the light or dim the lights to the percentage specify in the control command.

Fig 9 shown the waveform of the invention.

711 is the incoming a.c supply waveform to transmitter (or controller) **701.**
707 is the transmitter signal output from zero crossing detector **704** to transmitter CPU circuit **705.**
710 is the transmitter CPU **705** output of time delay pulse width which is proportional to control data '00' to '11'. The delay triggering pulse T0 (equal zero delay time) to T3 then send to Triac or SCR triggering circuit **706** of transmitter **701** immediately after zero crossing of supply voltage is detected . The amount of delay triggering of Triac or SCR is depends on the modulating data is '00', '01' '10' or '11'.
708 and **802** are pulse modulated output waveform of supply from transmitter or controller to receiver **801** and load **812.**
803 is the waveform of receiver **801** rectifier **806** output.
815 is the comparator **810** reference voltage.
804 is the waveform of receiver comparator and filtering circuit **810** output to receiver CPU circuit **811.** T4 **804a** (data 00), T5 **804b** (data 01), T6 **804c** (data 10) and T7 **804d** (data 11)

Fig 10 shows how the line supply voltage vary cause receiver recover pulse width change

In most of the time the loads under control are not pure resistive and a.c. supply might fluctuate between +/- 15% of standard supply voltage. This variation will affect the receiver recover pulse width.

1004 is the waveform of standard supply voltage from transmitter **701** to receiver **801. 1004a** is the receiver **801** rectifier output waveform. **815** is the reference voltage of comparator **811. 1004b** is the recover pulse output of comparator and filtering circuit **810** to CPU circuit **811.**

1001 is the waveform shows that the supply had increased. **1001a** is the receiver **801** rectifier output waveform. **1001b** is the recover pulse output of comparator and filtering circuit **810** to CPU circuit **811**.

As shown in **Fig 10** both **1001** and **1004** are different supply voltage with same pulse width modulation. Supply voltage **1001** is higher than **1004. 1001b** and **1004b** are recovering pulse of **1001** and **1004** respectively. Pulse width of **1004b** is wider than **1001b.** This shows that when the supply voltage increased the recover pulse width of comparator output reduced and vice versa.

Tracking of line supply voltage and load variation

In order to keep track of supply voltage variation and load change from resistive to inductive cause recover pulse width change (refer to **Fig 10**) and ensure that the receiver circuit recover the correct '00' to '11' data. The invention method is send the standard '00' to '11' pulse prior the control command as preamble.

The recover preamble pulse width of '00' to '11' changes when line voltage and load vary. The following synchronous and control command pulse width also shift same amount. This means that the pulse width of preamble and control command is varying in same proportion as line voltage or load vary.

Standard pulse width of '00' to '11' is sending prior the control command as preamble. CPU first extracts out the standard pulse width of '00' to '11' from preamble and stored it then compare it with following received synchronous and control command pulse width. Since the reference pulse width are vary same amount as synchronous and control command data when supply or load change.

CPU should be able to extract out the '00' to '11' data regardless of line voltage and load variation.

Format of signal from transmitter send to Receiver:

1. Transmitter or controller sends out: Preamble + Synchronous + Commands data.
   a. Preamble signal: Repeat '00' + '01' + '10' +'11' data stream.

      This data stream are use to track the line supply voltage variation. Line supply voltage is fluctuation slowly. It might vary +/- 15% over 24 hours. But in very short duration (few seconds) supply voltage can consider very stable.

      Minimum 2 times of 00' to '11' data streams are send out. This is for receiver **801** CPU **811** to record down the pulse width of '00','01', '10' and '11'. This info will be temporary stored and use as reference to extract the following synchronous and control command.

      The detected pulse width varies when the line supply voltage fluctuated. The reference pulse width are vary same amount as synchronous and control command when supply voltage or load change.

      In-order to extract out correct '00' to '11' data (line voltage and inductive load affects the recover pulse width). Preamble signal is very importance. It enables correct control command received and recovers when line voltage or inductive cause received pulse width change.

      Standard transmission baud rate is 240BPS (60 Hz supply) or 200BPS (50Hz supply). When the recover control command in the receiver affected by

      High noise interference or harmonic present in the power line might affect the recover pulse width. The result will cause CPU difficult to extract and recover data '00' to '11'. System will automatically reduce the transmission baud rate to 120 BPS (60 Hz supply) or 100 BPS (50 Hz supply).

      Pulse width of preamble data recover by receiver is T4, T5, T6 and T7. Which represent the data bit '00' '01' '10' and '11' respectively.

      Local receiver **606** near to transmitter detect the recover preamble pulse width of '00' (T4), '01' (T5), '10' (T6) and '11' (T7) too close to differentiate when severe noise present on supply line or incoming supply line have high harmonic content. This might cause error in the receiving control data. Local receiver **606** then sends out alert signal to transmitter **701**. Transmitter **701** received the alert signal from local receiver **606**. Transmitter will reduce the transmission baud rate to 120 BPS (60 Hz supply) or 100 BPS (50 Hz supply). Preamble signal send out from transmitter will contain delay time T0 and T3 only. Thus Triac will be trigger by time delay T0 and T3 only. Delay time T0 represent bit '0' and delay time T3 represent bit '1' of control command. When CPU **705** in the receiver **701** detected the preamble data contain only 2 stage time delay data represent data '00' and '11'. '01' and '10' data are

absent. CPU **705** will assume that the control command baud rate have reduced from to 240 BPS to 120BPS (or 200 BPS to 100BPS). Pulse width of recover data '00' will treat as data bit '0' and pulse width of '11' will treat as data bit '1'. CPU **705** then re-construct back the command data at reduce baud rate.

b. Synchronous signal: minimum 2 times '00' + '11' data.
   This is to inform CPU **705** the starting bit of the retrieved control command.

c. Control command: Control command consists of:
   Devices address: Every device under control have unique address and group address.
   Operation command: Like switch on or switch off the device and other functions.
   Operand: Instruct the device to perform specific operation. (E.g. dim the lights to 20% of full brightness etc).

Claims:

1. Splitting the series of '0' and '1' bits control command into series of '00' '01' '10' and '11' as 4 basic elements. Convert this basic element to fixed time delay duration and fed it to Triac or SCR triggering circuit and trigger the Triac or SCR when zero crossing of supply voltage is detected.
2. 4 basic fixed time delay triggering of Traic or SCR after zero crossing represent data bits '00' '01' '10; and '11'. This information is sending as preamble signal in series with synchronous and control command to receivers connected in down streams of transmitter (or controller).
3. Receiver retrieves the pulse width of preamble signal and uses it as reference pulse width of '00' '01' '10' and '11' data. The reference pulse width of '00' to '11' are stored in CPU and be use as reference pulse width of '00' '01' '10' and '11'.
4. CPU use reference pulse width of '00' '01' '10' and '11' info and compare it with the synchronous and control command pulse width after the preamble. CPU converts the synchronous and command pulse back to basic '00' '01' '10' and '11' basic data. CPU then uses these basic data to re-constructs back the synchronous data and control command. Synchronous data are use to indicate the starting of control command.
5. 4 basic fixed time delay triggering of Traic or SCR represent the data '00', '01', '10', and '11' are send as preamble of the control command. This information are use to keep track the supply voltage and load variation cause the receiver recover pulse width vary. The receiver recovering pulse width of preamble and control command are shifted same amount as supply voltage and load vary. CPU can successfully separate and retrieve the control command with the '00' to '11' reference pulse width contained in preamble.
6. Method of reduce baud rate transmission when local receiver **606** near to transmitter detected the severe interference cause the pulse width of recovering '00' '01' '10' and '11' data too close differentiate and might cause error in receiving control command. Receiver **606** will send out alert signal to transmitter. Transmitter then automatically reduces the transmission baud rate from 240 BPS to 120BPS in 60 Hz supply system (or 200 BPS to 100BPS in 50 Hz supply system).
7. Splitting the series of '0' and '1' bits control command into series of '000' '001' '010' to '111' as 8 basic elements (same method include split the command to '0000' to '1111' as 16 basic element or higher than 16 elements as '00000' to '11111' etc). Convert this basic element to fixed time delay duration and fed it to Triac or SCR triggering circuit and trigger the Triac or SCR when zero crossing of supply voltage is detected.
   Method of retrieving and re-structure back the control command same as 2) to 6) above.