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Tichester Court, Austin, TX 78729 (US). **OVERKAMP, Gregory, A.**; P.O. Box 163442, Austin, TX 78716 (US).

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(74) Agent: **HARRIS, Scott, C.**; Fish & Richardson P.C., Suite 500, 4350 La Jolla Village Drive, San Diego, CA 92122 (US).

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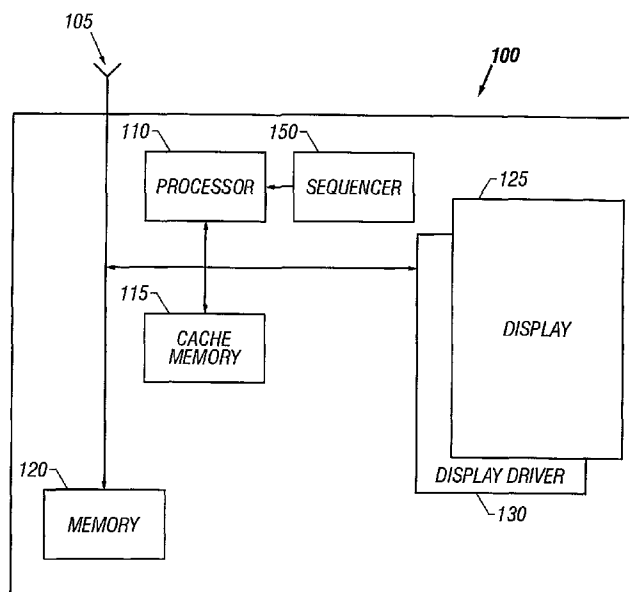
(71) Applicants: **INTEL CORPORATION** [US/US]; 2200 Mission College Boulevard, Santa Clara, CA 95052 (US). **ANALOG DEVICES, INC.** [US/US]; One Technology Way, P.O. Box 9106, Norwood, MA 02062 (US).

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(72) Inventors: **SINGH, Ravi, P.**; 12349 Metric Boulevard, #829, Austin, TX 78758 (US). **ROTH, Charles, P.**; 13305

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(54) Title: INSTRUCTION ADDRESS GENERATION AND TRACKING IN A PIPELINED PROCESSOR



(57) Abstract: In an embodiment, an address pipeline corresponding to an instruction pipeline in a processor, for example, a digital signal processor (DSP), may generate and track the instruction address of each instruction at each stage. The address pipeline may include program count (PC) generation logic to automatically calculate the PC of the next instruction based on the width of the current instruction for sequential program flow. The address pipeline may also track valid bits associated with each instruction and store the address of the oldest valid instruction for return to the original program flow after a disruptive event.

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