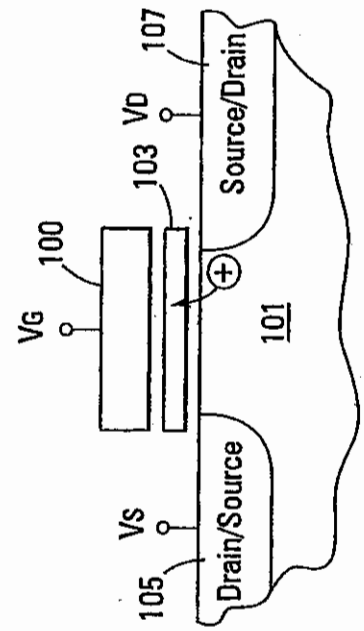

VG
100
103
VD
107
Source/Drain
101
Drain/Source
105
Vs

Fig. 2

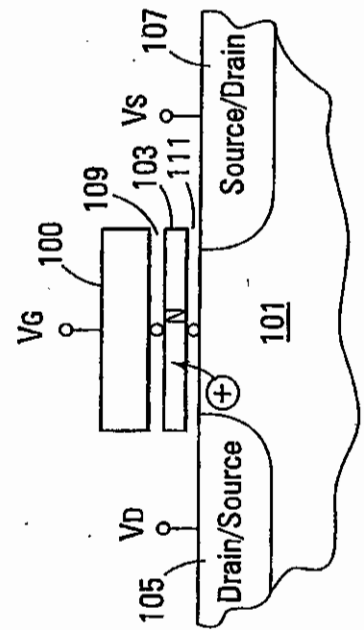

VG
100
109
103
111
Vs
107
Source/Drain
101
Drain/Source
105
VD

Fig. 1

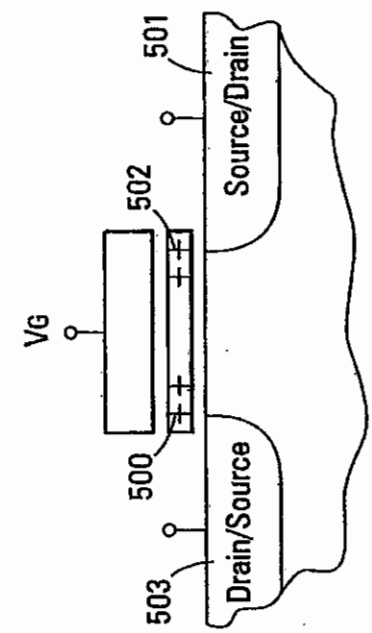


Fig. 5

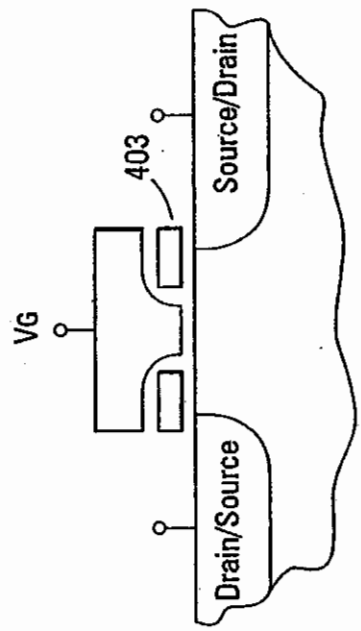


Fig. 4

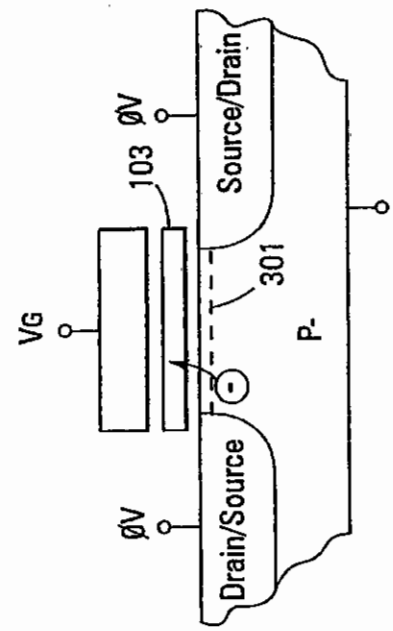


Fig. 3

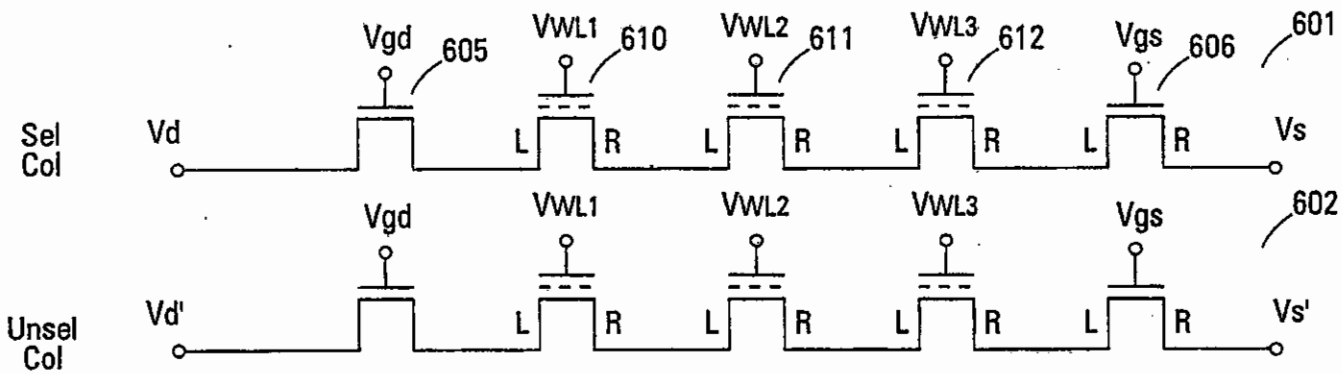


Fig. 6

OPERATION	Vd	Vd'	Vgd	VWL1	VWL2	VWL3	Vgs	Vs	Vs'
Erase (option 1)	gnd	gnd	+VH/2	+VH	+VH	+VH	+VH/2	gnd	gnd
Erase (option 2)	O/C	O/C	O/C	+VH	+VH	+VH	O/C	O/C	O/C
pgm VWL2 (L)	+VDP	gnd	Vx1	Vx2	-VH	Vx2	Vx1	gnd	gnd
pgm VWL2 (R)	gnd	gnd	Vx1	Vx2	-VH	Vx2	Vx1	+VDP	gnd
Read VWL2 (L)	gnd	gnd	Vy1	Vy2	VR	Vy2	Vy1	+VDR	gnd
Read VWL2 (R)	Vdr	gnd	Vy1	Vy2	VR	Vy2	Vy1	gnd	gnd

Fig. 7

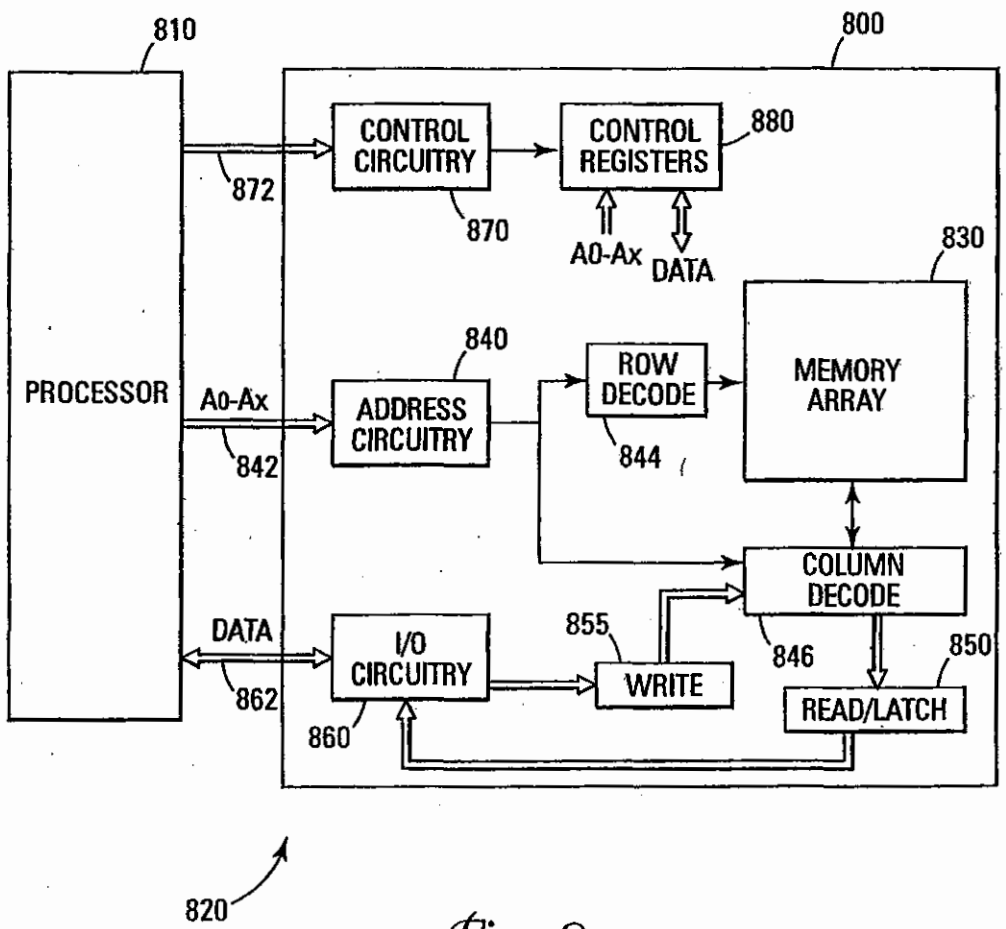

810
800
PROCESSOR
CONTROL CIRCUITRY
CONTROL REGISTERS
880
872
870
A0-Ax
DATA
830
840
A0-Ax
ADDRESS CIRCUITRY
ROW DECODE
MEMORY ARRAY
842
844
COLUMN DECODE
DATA
I/O CIRCUITRY
855
WRITE
846
850
READ/LATCH
862
860
820

Fig. 8