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International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 13/00, 13/40 — A1

(11) International Publication Number: WO 96/22571

(43) International Publication Date: 25 July 1996 (25.07.96)

(21) International Application Number: PCT/US96/00506

(22) International Filing Date: 16 January 1996 (16.01.96)

(30) Priority Data:
08/375,972 20 January 1995 (20.01.95) US

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(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AZ, BY, KG, KZ, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published

With international search report.

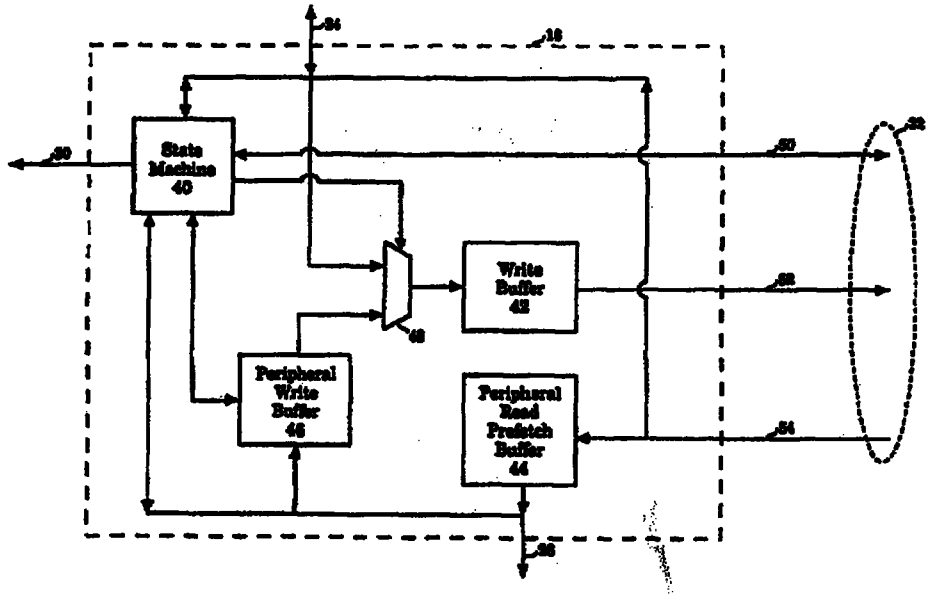
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

SG 9700807-2

RTMP's copy + IPER + annexes

Claim 1 to 14 cancelled
New claim 15 to 22.

(54) Title: BUS BRIDGE CIRCUIT AND METHOD USING SNOOP AHEAD OPERATIONS



(57) Abstract

An integrated bus bridge and memory controller circuit (16) enables access to a shared memory (18) with high bandwidth data streaming. The bus bridge and memory controller circuit (16) performs a series of snoop ahead transactions over the processor bus (24) during access transactions to the shared memory (18) that originate over the peripheral bus (26) and thereby enables high bandwidth data streaming on the peripheral bus (26). The bus bridge and memory controller circuit (16) may be used in a computer system (10) having a processor (12) and a cache memory (14) coupled to the processor bus (24), and a set of bus agents (20, 22) coupled to the peripheral bus (26). The circuit (16) may include a write buffer (42) for merging write data received over the buses, a peripheral write buffer (46) that stores a snoop done flag, and a peripheral read prefetch buffer (44).