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DISPLAY APPARATUS

BACKGROUND OF THE INVENTION

This invention relates generally to a display apparatus which includes a display panel, a video driver and a timing generator and specifically to a driving control technique for a display apparatus which adopts a plural pixel simultaneous sampling system, and more specifically to a technique for removing noise included in a video signal to be supplied from a video driver to a display panel.

A plural pixel simultaneous sampling system is effective as a driving system for a display panel represented by a liquid crystal display panel of the active matrix type and is disclosed, for example, in Japanese Patent Laid-Open No. Hei 4-116687. According to the plural pixel simultaneous driving system, a color display panel includes a plurality of signal lines which are disposed in parallel to each other in a vertical direction and wherein each successive three signal lines make up a set for the colors of red (R), green (G) and blue (B). Further, the color display panel includes a plurality of gate lines arranged in parallel to each other in a horizontal

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direction. Furthermore, the color display panel includes pixel electrodes individually connected to intersecting points of the signal lines and the gate lines via respective switching elements. The pixel electrodes are arranged at a predetermined arrangement pitch in a matrix. In addition, the color display panel includes a plurality of horizontal switches individually provided corresponding to the signal lines. Further, the color display panel includes three video lines connected for the individual colors to the signal lines via the horizontal switches and accepts video signals of R, G and B supplied thereto from a video driver. In the plural pixel simultaneous sampling system of the construction described above, a horizontal driving circuit for simultaneously controlling the horizontal switches in units of a set for the colors R, G and B and performs RGB three pixel simultaneous sampling driving. In this instance, a sample and hold unit for relatively providing delay amounts corresponding to the arrangement pitch of the pixels to the video signals of R, G and B supplied to the three video lines is provided in the video driver. By relatively providing the delay amounts corresponding to the arrangement pitch of the pixels to the video signals of R, G and B and controlling

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opening and closing operations of the horizontal switches simultaneously in units of a set for R, G and B, the number of stages of horizontal driving circuits (for example, shift registers) for driving the horizontal switches is reduced to achieve simplification in construction and also to reduce the power dissipation while a good color display image is obtained. Since the horizontal switches for R, G and B are constructed so that the opening and closing operations thereof are simultaneously controlled by a selection pulse outputted from a shift register, the number of stages of the shift registers is reduced to one third. Further, also the frequency of a horizontal clock signal to be supplied from a timing generator is reduced to one third.

In a display apparatus which adopts the plural pixel simultaneous sampling system, video signals to be inputted to a display panel of the active matrix type are produced by a video driver built in a sample and hold unit. However, an ordinary sample and hold unit produces, at timings at which the on-off operation is changed over alternately, noise originating from sample and hold leakage. Since the noise is supplied in a superposed condition on the video signals to the display panel, the

display apparatus has a subject to be solved in that a display defect in the form of a vertical stripe appears on the screen and deteriorates the picture quality remarkably.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a display apparatus of a plural pixel simultaneous driving system wherein sample and hold noise included in a video signal is removed before the video signal is supplied to a display panel.

In order to attain the object described above, according to an aspect of the present invention, there is provided a display apparatus which comprises a display panel including pixels arranged at intersecting points between gate lines and signal lines which extend perpendicularly to each other, and a driving circuit for distributing a plurality of video signals for individual sets each including a predetermined number of ones of the signal lines to drive a plurality of ones of the pixels at a time, a video driver for relatively delaying a plurality of original video signals in accordance with an arrangement pitch of the pixels to obtain the plurality of video signals and supplying the plurality of video signals to the

display panel, and a timing generator for supplying a timing signal to the display panel and the video driver to synchronously control the plural pixel simultaneous driving of the driving circuit and the delaying processing of the video driver, the video driver including a first sample and hold means for repetitively sampling and holding the original video signals inputted thereto from the outside in response to the timing signal inputted thereto from the timing generator, a second sample and hold means for repetitively sampling and holding a predetermined reference signal in response to the timing signal, and a differential means for differentially processing the original video signals after sampled and held and the reference signal after the sampled and held to produce video signals from which noise originating from the sampling and holding has been removed. Preferably, the second sample and hold means repetitively samples and holds the reference signal of a fixed voltage and intentionally adds noise originating from the sampling and holding.

In a display apparatus which adopts the plural pixel simultaneous driving system, sample and hold noises produced by RGB video drivers make a cause of a vertical stripe or a like display defect on the display screen.

Therefore, in the present invention, sample and hold noise produced by a video driver is intentionally produced separately from a processing system for an actual video signal, and they are differentially processed (subtraction processed) with each other to erase the noise from the output video signal. In particular, separately from the processing system for an actual video signal, a processing system for a reference signal (dummy signal) is provided, and sample and hold noise of the same timing is produced artificially by the processing system for the reference signal. By differentially processing the outputs of the two signal processing systems, the sample and hold noises included in both of them cancel each other. Consequently, since the video signal to be supplied from the video driver to the display panel does not include any sample and hold noise, a display defect such as a vertical stripe can be suppressed. Accordingly, the display apparatus is advantageous in that it provides an improved picture quality.

According to another aspect of the present invention, the display apparatus is driven by a driving method which comprises the steps of repetitively sampling and holding, by means of said video driver, the original

video signals inputted from the outside in response to the timing signal inputted from said timing generator, repetitively sampling and holding a predetermined reference signal simultaneously in response to the timing signal, and differentially processing the original video signals after sampled and held and the reference signal after sampled and held to produce a video signal from which noise originating from the sampling and holding has been removed.

Preferably, the reference signal of a fixed voltage is repetitively sampled and held to intentionally add noise originating from the sampling and holding.

According to a further aspect of the present invention, there is provided a video signal processing circuit for delaying an input video signal supplied thereto from the outside in response to a timing signal supplied thereto from the outside to produce an output video signal, which comprises a first sample and hold means for repetitively sampling and holding the input video signal in response to the timing signal, a second sample and hold means for repetitively sampling and holding a predetermined reference signal in response to the timing signal, and a differential means for differentially processing the input video signal and the reference signal after sampled and

held to produce an output video signal from which sample and hold noise synchronized with the timing signal has been removed.

The above and other objects, features and advantages of the present invention will become apparent from the following description and the appended claims, taken in conjunction with the accompanying drawings in which like parts or elements are denoted by like reference characters.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing a basic construction of a video signal processing circuit to which the present invention is applied;

FIG. 2 is a waveform diagram illustrating operation of the video signal processing circuit shown in FIG. 1;

FIG. 3 is a block diagram showing a general construction of a display apparatus to which the present invention is applied;

FIG. 4 is a block diagram showing an example of a construction of a video driver incorporated in the display apparatus shown in FIG. 3;

FIG. 5 is a waveform diagram illustrating timing signals supplied from a timing generator incorporated in the display apparatus shown in FIG. 3;

FIG. 6 is a block diagram showing an example of a detailed construction of a display panel incorporated in the display apparatus shown in FIG. 3;

FIG. 7 is a waveform diagram illustrating description of operation of the display panel shown in FIG. 6;

FIG. 8 is a circuit diagram showing an example of a construction of a first sample and hold circuit included in the video signal processing circuit shown in FIG. 1;

FIG. 9 is a waveform diagram illustrating operation of the first sample and hold circuit shown in FIG. 8;

FIG. 10 is a circuit diagram showing an example of a detailed construction of the video signal processing circuit shown in FIG. 1;

FIG. 11 is a graph illustrating a relationship between an input video signal to the video driver shown in FIG. 4 and a noise included in an output video signal.

FIG. 12 is a schematic view illustrating simulation conditions in the graph shown in FIG. 11;

FIG. 13 is a graph illustrating a linearity between the input video signal and the output video signal of the video driver shown in FIG. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring first to FIG. 1, there is shown in block diagram a basic construction of a video signal processing circuit to which the present invention is applied. The video signal processing circuit operates in response to a timing signal (latch signal) PS/H supplied thereto from an external timing signal source 1 and delays an input video signal (original video signal) V_{sigin} supplied similarly from an external video signal source 2 to produce an output video signal VS/H. The video signal processing circuit includes a first sample and hold circuit 3, a second sample and hold circuit 4, and a differential circuit 5. The first sample and hold circuit 3 repetitively samples and holds the input video signal V_{sigin} in response to the timing signal PS/H. The second sample and hold circuit 4 repetitively samples and holds a predetermined reference signal V_{ref} in response to the timing signal PS/H. It is to be noted that, in the circuit arrangement shown in FIG. 1, a signal of a fixed voltage supplied from a reference

signal source 6 is used as the reference signal V_{ref} . The differential circuit 5 differentially processes an input video signal $V_{sigS/H}$ after sampled and held and a reference signal $V_{refS/H}$ after sampled and held to produce an output video signal $V_{S/H}$ from which sample and hold noise synchronized with the timing signal PS/H has been removed. In other words, $V_{S/H} = V_{sigS/H} - V_{refS/H}$. It is to be noted that the differential circuit 5 is formed of an input transistor T_r , an output transistor T_r , a load resistor R and so forth. The video signal processing circuit having the construction described above is incorporated as a sample and hold unit S/H into, for example, a video driver.

Referring now to FIG. 2, operation of the video signal processing circuit (sample and hold unit S/H) shown in FIG. 1 is illustrated. The first sample and hold circuit 3 samples and holds the input video signal V_{sign} to produce the video signal $V_{sigS/H}$. A noise $\Delta V_{S/H}$ synchronized with the latch signal PS/H is superposed with the video signal $V_{sigS/H}$. Meanwhile, the second sample and hold circuit 4 samples and holds the reference signal V_{ref} to produce the reference signal $V_{refS/H}$. Also the reference signal $V_{refS/H}$ includes a noise $\Delta V_{S/H}$ of an

equal amount superposed with the reference signal V_{ref} . The differential circuit 5 thus performs differential processing between the video signal $V_{sigS/H}$ and the reference signal $V_{refS/H}$ to form an output video signal $V_{S/H}$ from which the noise $\Delta V_{S/H}$ has been removed.

FIG. 3 shows in block diagram a basic construction of a display apparatus to which the present invention is applied. Referring to FIG. 3, the display apparatus shown includes a display panel 11, a video driver 12, and a timing generator 13. The display panel 11 includes pixels arranged at intersecting points between gate lines and signal lines which extend perpendicularly to each other, and a horizontal driving circuit for distributing a plurality of video signals V_{sigout} (in the present example, three video signals separated to systems of the three primary RGB colors) for individual sets each including a predetermined number of (three in the present arrangement) ones of the signal lines to drive a plurality of ones of the pixels at a time. It is to be noted that the horizontal driving circuit operates in response to a pair of horizontal clock signals $HCK1$ and $HCK2$ and successively transfers a predetermined horizontal start signal HST to perform three pixel simultaneous driving described above.

Further, the display panel 11 has, in addition to the horizontal driving circuit, a built-in vertical driving circuit and line sequentially scans the gate lines. The vertical driving circuit operates in response to a pair of vertical clock signals VCK1 and VCK2 and successively transfers a vertical start signal VST to line sequentially select the gate lines. The video driver 12 relatively delays a plurality of original video signals Vsign (in the present example, video signals of the three systems of VR, VG and VB) in accordance with an arrangement pitch of the pixels and supplies video signals Vsigout of the three RGB systems described above to the display panel 11. The timing generator 13 supplies timing signals such as the horizontal start signal HST and the horizontal clock signals HCK1 and HCK2 to the horizontal driving circuit of the display panel 11 to control the three pixel simultaneous driving described above. Further, the timing generator 13 supplies timing signals such as the vertical start signal VST and the vertical clock signals VCK1 and VCK2 to the vertical driving circuit of the display panel 11 to control the line sequential scanning of the gate lines. Furthermore, the timing generator 13 supplies timing signals (latch signals) such as timing signals

PS/H1, PS/H2, PS/H3 and PS/H4 to the video driver 12 to control operation of the video driver 12. Consequently, the timing generator 13 can synchronously control the three pixel simultaneous driving of the display panel 11 and the delaying processing (sample and hold processing) of the video driver 12.

FIG. 4 shows in block diagram an example of a detailed construction of the video driver 12 shown in FIG. 3. As described hereinabove, the video driver 12 relatively delays the original video signals V_{signin} of the three VR, VG and VB systems in accordance with the arrangement pitch of the pixels to adjust the supply timings of the video signals V_{sigout} of the three RGB systems to the display panel 11. In the present arrangement, the video driver 12 has an analog construction and includes sample and hold units S/H which perform delaying processing of the original video signals V_{signin}. In particular, the video driver 12 includes three front stage sample and hold units S/H1, S/H2 and S/H3 corresponding to the original video signals V_{signin} of the three VR, VG and VB systems. The video driver 12 further includes three rear stage sample and hold units S/H4 individually connected to the front stage sample and hold

units S/H1, S/H2 and S/H3. A delay channel corresponding to the VR system is formed of a set of the front stage sample and hold unit S/H1 and a corresponding one of the rear stage sample and hold units S/H4; another delay channel corresponding to the VG system is formed of a set of the front stage sample and hold unit S/H2 and a corresponding one of the rear stage sample and hold units S/H4; and a further delay channel corresponding to the VB system is formed of a set of the front stage sample and hold unit S/H3 and a corresponding one of the rear stage sample and hold units S/H4. The front stage sample and hold units S/H1, S/H2 and S/H3 are controlled in synchronism with each other. It is to be noted that an amplifier AMP is connected to the output stage of each one of the delay channels. In the present example, the original video signals V_{sign} of the three VR, VG and VB systems are distributed to the three delay channels, and the video signals V_{sigout} of the relatively delayed three RGB systems are outputted. Here, at least the three rear stage sample and hold units S/H4 have the video signal processing circuit construction shown in FIG. 1 and remove, from the output video signals V_{sigout} of the three RGB systems, noise originating from the sampling and holding.

It is to be noted that naturally the video signal processing circuit construction shown in FIG. 1 may be adopted also for the front stage sample and hold units S/H1, S/H2 and S/H3.

FIG. 5 shows waveforms of various timing signals supplied from the timing generator 13 shown in FIG. 3. As described hereinabove, the timing generator 13 operates in response to a synchronizing signal inputted thereto from the outside and supplies the horizontal start signal HST, the horizontal clock signals HCK1, HCK2 and so forth to the display panel 11 to control driving of the display panel 11. Though not shown, the timing generator 13 additionally supplies the vertical start signal VST and the vertical clock signals VCK1 and VCK2 to the display panel 11. Further, the timing generator 13 supplies a plurality of latch signals PS/H1, PS/H2, PS/H3 and PS/H4 to the sample and hold units of the video driver 12. The processing timings of the sample and hold units included in the delay channels of the three systems are defined by those latch signals. In particular, the first front stage sample and hold unit S/H1 is first caused to intermittently operate in response to the latch signal PS/H1. Then, the second front stage sample and hold unit S/H2 is caused to intermittently

operate in response to the latch signal PS/H2 while the third front stage sample and hold unit S/H3 is caused to continuously operate in response to the latch signal PS/H3. Further, after the latch signal PS/H2 is outputted, the latch signal PS/H4 is outputted so that the three rear stage sample and hold units S/H4 are caused to intermittently operate all at once. In particular, the potentials of the original video signals V_{sign} held by the front stage sample and hold units S/H1, S/H2 and S/H3 are re-sampled at a timing at which the rear stage sample and hold units S/H4 are turned on, and are supplied to the display panel 11 side. The display panel 11 can simultaneously select the video signals of the three systems by horizontal switches. Naturally, the front stage sample and hold units S/H1, S/H2 and S/H3 have phases shifted relative to each other. Accordingly, time information included in the video signals is not lost. In this manner, when plural pixel simultaneous driving is performed in the display panel, in order that time information included in the video signals may not be lost, the original video signals V_{sign} are first sampled by the front stage sample and hold units S/H1, S/H2 and S/H3 having phases displaced from each other, and then sampled

by the sample and hold units S/H4 at the rear stage so that they may be selected simultaneously at a suitable timing in the display panel.

Here, at least the rear stage sample and hold units S/H4 have the video signal processing circuit construction shown in FIG. 1 as described above and each produces a video signal VS/H from which noise originating from sampling and holding has been removed. The waveform of the video signal VS/H when it is assumed that no noise removal is performed is indicated at the lowest stage in FIG. 5. If no countermeasure is taken, then at a timing at which the latch signal PS/H4 falls, a noise $\Delta VS/H$ which originates from sample and hold leakage is superposed as an offset to the original video signal V_{sign}. In particular, within a sampling time within which the latch signal PS/H4 is in an on state, the video signal VS/H exhibits a potential equal to that of the input video signal V_{sign}, but within a holding time within which the latch signal PS/H4 is in an off state, the output video signal VS/H is equal to V_{sign} + $\Delta VS/H$. The video signal VS/H is amplified by the succeeding amplifier AMP, and a final output video signal V_{sigout} is supplied to the display panel side. Since such noise $\Delta VS/H$ makes a cause by which

a vertical stripe appears on the display screen, in the present invention, the video signal processing circuit construction shown in FIG. 1 is adopted for the rear stage sample and hold units S/H4 to remove the noise $\Delta V_{S/H}$ in advance.

FIG. 6 shows an example of a detailed construction of the display panel 11 shown in FIG. 3. The display panel 11 includes a pixel array section and a peripheral driving circuit section. The pixel array section includes liquid crystal pixels PXL arranged at individual intersecting points between gate lines X and signal lines Y which extend perpendicularly to each other. Each of the pixels PXL is driven by a switching element formed of a thin film transistor TFT. The gate electrode of the thin film transistor TFT is connected to a corresponding gate line X, the source electrode is connected to a corresponding signal line Y, and the drain electrode is connected to a pixel electrode of a corresponding liquid crystal pixel PXL. Further, though not shown, an opposing electrode is disposed in an opposing relationship to each pixel electrode with a predetermined gap left therebetween, and liquid crystal is enclosed in the gap. Meanwhile, the peripheral driving circuit section is divided into a

vertical driving circuit 21 and a horizontal driving circuit 22. The vertical driving circuit 21 is connected to the gate lines X and line sequentially selects the pixels PXL of one line. In particular, the vertical driving circuit 21 includes a shift register, and it successively transfers the vertical start signal VST in response to the vertical clock signals VCK1 and VCK2 and outputs a gate pulse to each gate line X. On the other hand, the horizontal driving circuit 22 samples the video signals Vsigout of the three RGB systems at a time and distributes them all at once to a predetermined number of (three in the present example) ones of the signal lines Y. In particular, a plurality of horizontal switches HSW are interposed between the horizontal driving circuit 22 and the signal lines Y. Each of the horizontal switches HSW is connected commonly to three signal lines Y. The video signals Vsigout of the three RGB systems are sampled at a time at the three corresponding signal lines Y via the individual horizontal switches HSW. The horizontal driving circuit 22 successively transfers the horizontal start signal HST in response to the horizontal clock signals HCK1 and HCK2 supplied thereto from the timing generator 13 and outputs selection pulses PHSW1, PHSW2, PHSW3, ... In

response to the selection pulses PHSW, the corresponding horizontal switches HSW are controlled to be opened or closed so that simultaneous sampling described above is performed.

FIG. 7 illustrates in timing chart the relationship between each of the video signals Vsigout inputted to the display panel 11 and the selection pulses PHSW. As described hereinabove, noise has been removed from the video signal Vsigout, and there is no problem if the selection pulses PHSW have a dispersion from one another. Here, in order to facilitate understanding of the invention, a condition wherein noise is contained in the video signal Vsigout is illustrated in FIG. 7. Here, the sampling timing in the display panel is the point of time of a falling edge of each of the selection pulses PHSW. Since the phases of the selection pulses PHSW have a little dispersion from each other, the potentials of the video signal Vsigout sampled are different among different sets of three signal lines, and they appear as a vertical stripe on the screen. For example, those signal lines Y sampled in response to the selection pulses PHSW1 and PHSW3 are held at a signal level to be used for actual writing, but those signal lines Y sampled in response to the selection

pulses PHSW2 and PHSW4 exhibit a little higher signal level. This appears as a vertical stripe and deteriorates the picture quality significantly. For example, with a display panel of a normally white mode, signal lines which sample noise will have a tinge of black. Therefore, in the present invention, sample and hold noise included in the video signal Vsigout is removed on the video driver side in advance so that, even if the selection pulses PHSW exhibit some dispersion on the display panel side, no vertical stripe may appear.

FIG. 8 shows in circuit diagram an example of a detailed construction of the first sample and hold circuit 3 included in the video signal processing circuit (sample and hold unit S/H) shown in FIG. 1. Referring to FIG. 8, the first sample and hold circuit 3 operates in response to the latch signal PS/H inputted thereto from the timing signal source 1 such as a timing generator and repetitively samples and holds the video signal Vsigin inputted thereto from the video signal source 2 such as a video decoder. The input video signal VsigS/H after sampled and held is taken out via a load resistor r and a load capacitor C . As seen from FIG. 8, the first sample and hold circuit 3 is formed of six transistors Q1 to Q6.

Operation of the first sample and hold circuit 3 shown in FIG. 8 will be described in detail with reference to FIG. 9. When the latch signal PS/H is at the high level, the transistor Q2 to whose base terminal a predetermined bias voltage V_{bias} is applied exhibits an off state while current I_1 flows through a system of the transistor Q1. Consequently, the input video signal $V_{sigS/H}$ exhibits a potential equal to that of the input video signal V_{sigin} . However, when the latch signal PS/H falls from the high level to the low level, the timings at which currents flowing through individual nodes are cut are different. In particular, currents I_3 and I_4 fall first, and then, currents I_5 and I_6 fall. Consequently, the difference I_7 ($I_6 - I_4$) between the currents I_6 and I_4 does not flow between the collector and the emitter of the transistor Q4, but flows to the output terminal side. In particular, at this point of time, since the transistor Q4 is in an off state, the residual current I_7 ($I_6 - I_4$) misses its escape and appears at the output terminal. Consequently, the video signal $V_{sigS/H}$ exhibits different values upon sampling and upon holding, and this makes a noise $\Delta V_{S/H}$. Therefore, according to the present invention, the second sample and hold circuit 4 is provided

in addition to the first sample and hold circuit 3, and a predetermined reference signal is repetitively sampled and held in response to the same latch signal PS/H to intentionally produce a noise $\Delta V_{S/H}$ of an equal amount. Then, the video signal $V_{sigS/H}$ after sampled and held and the reference signal after sampled and held similarly are differentially processed to remove the noise $\Delta V_{S/H}$ originating from the sampling and holding. It is to be noted that, as a result of the differential processing, a DC level is added to the sample and hold video signal $V_{S/H}$. However, the DC component is clamped in the video driver, and the DC offset does not matter at all.

FIG. 10 shows in circuit diagram an example of a detailed construction of the video signal processing circuit (sample and hold unit) shown in FIG. 1. The video signal processing circuit shown is applied to a set of the front stage sample and hold unit S/H1 and the corresponding rear stage sample and hold unit S/H4 constructing a channel of the R system included in the video driver 12 shown in FIG. 4. Here, the front stage sample and hold unit S/H1 has an ordinary construction, and the rear stage sample and hold unit S/H4 has a noise removing function in accordance with the present invention. As shown in FIG. 10, the front

stage sample and hold unit S/H1 and the rear stage sample and hold unit S/H4 are connected to each other with an emitter follower 31 interposed therebetween. The front stage sample and hold unit S/H1 has a construction similar to that of the first sample and hold circuit 3 shown in FIG. 8. In other words, the front stage sample and hold unit S/H1 of the ordinary structure is formed only of the first sample and hold circuit shown in FIG. 8 and does not have a removing function for sample and hold noise at all. However, naturally the front stage sample and hold unit S/H1 may alternatively have a sample and hold function built therein. In contrast, the rear stage sample and hold unit S/H4 is formed of a first sample and hold circuit 3, a second sample and hold circuit 4 and a differential circuit 5. The first sample and hold circuit 3 and the second sample and hold circuit 4 have a basically same construction. The first sample and hold circuit 3 repetitively samples and holds an input video signal supplied thereto from the front stage sample and hold unit S/H1 in response to a latch signal PS/H4. Also the second sample and hold circuit 4 operates in response to the same latch signal PS/H4 and repetitively samples and holds a predetermined reference signal Vref. The differential

circuit 5 differentially processes the video signal $V_{sigS/H}$ after sampled and held and the reference signal $V_{refS/H}$ after sampled and held to produce an output video signal $V_{S/H}$ from which sample and hold noise synchronized with the latch signal $PS/H4$ has been removed.

FIG. 11 illustrates in graph a result of a simulation wherein sample and hold noise is compared in magnitude between an arrangement of the related art and the arrangement of the present invention. Referring to FIG. 11, the axis of abscissa represents the input video signal V_{sin} in units of V , and the axis of ordinate represents the magnitude of the noise $\Delta V_{S/H}$ in units of mV . The input video signal V_{sin} is varied stepwise for the individual three RGB systems to individually detect the noises $\Delta V_{S/H}$ by simulation. As apparently seen from the graph, comparing with the related art arrangement, the noise $\Delta V_{S/H}$ can be reduced to approximately one fourth to one fifth with the arrangement of the present invention.

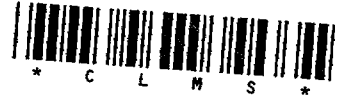
FIG. 12 illustrates conditions of the simulation illustrated in FIG. 11. While the related art arrangement employs, for the rear stage sample and hold units $S/H4$, a sample and hold unit having no noise removing function, the arrangement of the present invention employs, for the rear

stage sample and hold units S/H4, a sample and hold unit which has an additional noise removing function. In the simulation, noises $\Delta V_{S/H}$ included in the output video signals $V_{S/H}$ outputted for the individual three RGB systems were detected. In this instance, the on times of the latch signals PS/H were set to 22 nsec, and the off times were set to 44 nsec. Further, the rising time and the falling time of pulses forming the latch signals PS/H were set to 5 nsec. In addition, the potential level of the reference signal V_{ref} was set to 2.5 V. Further, the potential level of the bias voltage V_{bias} was set to 1.6 V. The result of the simulation of the noises $\Delta V_{S/H}$ conducted under the conditions described above is the graph of FIG. 11.

FIG. 13 illustrates in graph a result of a simulation of the relationship between the input video signal V_{sigin} and the output video signal $V_{S/H}$. As seen from FIG. 13, a sufficient linearity is maintained between the input video signal V_{sigin} and the output video signal $V_{S/H}$, and it can be seen that the removing processing of sample and hold noise according to the present invention does not have any bad influence at all.

Having now fully described the invention, it will be apparent to one of ordinary skill in the art that many

changes and modifications can be made thereto without departing from the spirit and scope of the invention as set forth herein.



WHAT IS CLAIMED IS:

1. A display apparatus, comprising:

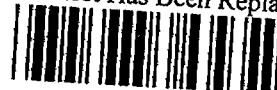
a display panel including pixels arranged at intersecting points between gate lines and signal lines which extend perpendicularly to each other, and a driving circuit for distributing a plurality of video signals for individual sets each including a predetermined number of ones of said signal lines to drive a plurality of ones of said pixels at a time;

a video driver for relatively delaying a plurality of original video signals in accordance with an arrangement pitch of said pixels to obtain the plurality of video signals and supplying the plurality of video signals to said display panel; and

a timing generator for supplying a timing signal to said display panel and said video driver to synchronously control the plural pixel simultaneous driving of said driving circuit and the delaying processing of said video driver;

said video driver including a first sample and hold means for repetitively sampling and holding the original video signals inputted thereto from the outside in response to the timing signal inputted thereto from said

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timing generator, a second sample and hold means for repetitively sampling and holding a predetermined reference signal in response to the timing signal, and a differential means for differentially processing the original video signals after sampled and held and the reference signal after the sampled and held to produce video signals from which noise originating from the sampling and holding has been removed.

2. A display apparatus according to claim 1, wherein said second sample and hold means repetitively samples and holds the reference signal of a fixed voltage and intentionally adds noise originating from the sampling and holding.

3. A video signal processing circuit for delaying an input video signal supplied thereto from the outside in response to a timing signal supplied thereto from the outside to produce an output video signal, comprising:

a first sample and hold means for repetitively sampling and holding the input video signal in response to the timing signal;

a second sample and hold means for repetitively sampling and holding a predetermined reference signal in response to the timing signal; and

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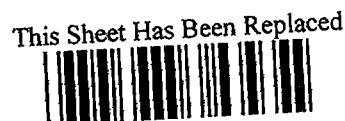




a differential means for differentially processing the input video signal and the reference signal after sampled and held to produce an output video signal from which sample and hold noise synchronized with the timing signal has been removed.

4. A driving method for a display apparatus which includes a display panel including pixels arranged at intersecting points between gate lines and signal lines which extend perpendicularly to each other and a driving circuit for distributing a plurality of video signals for individual sets each including a predetermined number of ones of said signal lines to drive a plurality of ones of said pixels at a time, a video driver for relatively delaying a plurality of video signals in accordance with an arrangement pitch of said pixels to obtain the plurality of video signals and supplying the plurality of video signals to said display panel, and a timing generator for supplying a timing signal to said display panel and said video driver to synchronously control the plural pixel simultaneous driving of said driving circuit and the delaying processing of said video driver, said driving method comprising the steps of:

repetitively sampling and holding, by means of





said video driver, the original video signals inputted from the outside in response to the timing signal inputted from said timing generator;

repetitively sampling and holding a predetermined reference signal simultaneously in response to the timing signal; and

differentially processing the original video signals after sampled and held and the reference signal after sampled and held to produce a video signal from which noise originating from the sampling and holding has been removed.

5. A driving method for a display apparatus according to claim 4, wherein the reference signal of a fixed voltage is repetitively sampled and held to intentionally add noise originating from the sampling and holding.

This Sheet Has Been Replaced

