MASK MATERIAL CONVERSION

Background of the Invention

Field of the Invention

This invention relates generally to integrated circuit fabrication and, more particularly, to masking techniques.

Description of the Related Art

As a consequence of many factors, including demand for increased portability, computing power, memory capacity and energy efficiency in modern electronics, integrated circuits are continuously being reduced in size. To facilitate this size reduction, the sizes of the constituent features, such as electrical devices and interconnect line widths, that form the integrated circuits are also constantly being decreased.

The trend of decreasing feature size is evident, for example, in memory circuits or devices such as dynamic random access memories (DRAMs), static random access memories (SRAMs), ferroelectric (FE) memories, etc. To take one example, DRAM typically comprises millions of identical circuit elements, known as memory cells. In its most general form, a memory cell typically consists of two electrical devices: a storage capacitor and an access field effect transistor. Each memory cell is an addressable location that can store one bit (binary digit) of data. A bit can be written to a cell through the transistor and read by sensing charge on the storage electrode from the reference electrode side. By decreasing the sizes of constituent electrical devices and the conducting lines that access them, the sizes of the memory devices incorporating these features can be decreased. Additionally, storage capacities can be increased by fitting more memory cells into the memory devices.

The continual reduction in feature sizes places ever greater demands on techniques used to form the features. For example, photolithography is commonly used to pattern features, such as conductive lines, on a substrate. The concept of pitch can be used to describe the size of these features. Pitch is defined as the distance between an identical point in two neighboring features. These features are typically defined by spaces between adjacent features, which are typically filled by a material, such as an insulator or conductor. As a result, pitch can be viewed as the sum of the width of a feature and of the width of the space separating that feature from a neighboring feature. Due to factors such as optics and light or radiation wavelength, however, photolithography techniques each have a minimum pitch below which a particular

photolithographic technique cannot reliably form features. Thus, the minimum pitch of a photolithographic technique can limit feature size reduction.

"Pitch doubling" is one method proposed for extending the capabilities of photolithographic techniques beyond their minimum pitch. Such a method is illustrated in Figures 1A-1F and described in U.S. Patent No. 5,328,810, issued to Lowrey *et al.* With reference to Figure 1A, photolithography is first used to form a pattern of lines 10 in a photoresist layer overlying a layer 20 of an expendable material and a substrate 30. As shown in Figure 1B, the pattern is then transferred by an etch step (preferably anisotropic) to the layer 20, forming placeholders, or mandrels, 40. The photoresist lines 10 can be stripped and the mandrels 40 can be isotropically etched to increase the distance between neighboring mandrels 40, as shown in Figure 1C. A layer 50 of material is subsequently deposited over the mandrels 40, as shown in Figure 1D. Spacers 60, *i.e.*, material extending or originally formed extending from sidewalls of another material, are then formed on the sides of the mandrels 40 by preferentially etching the spacer material from the horizontal surfaces 70 and 80 in a directional spacer etch, as shown in Figure 1E. The remaining mandrels 40 are then removed, leaving behind only the spacers 60, which together act as an etch mask for patterning underlying layers, as shown in Figure 1F. Thus, where a given pitch formerly included a pattern defining one feature and one space, the same width now includes two features and two spaces defined by the spacers 60. As a result, the smallest feature size possible with a photolithographic technique is effectively decreased.

It will be appreciated that while the pitch is actually halved in the example above, this reduction in pitch is conventionally referred to as pitch "doubling," or, more generally, pitch "multiplication." That is, conventionally "multiplication" of pitch by a certain factor actually involves reducing the pitch by that factor. The conventional terminology is retained herein.

The critical dimension of a feature is the feature's minimum dimension. For features formed using the spacers 60, the critical dimension typically corresponds to the width of the spacers. The width of the spacers, in turn, is typically dependent upon a thickness 90 (see Figures 1D and 1E) of the layer 50. Thus, the layer 50 is typically formed to a thickness 90 corresponding to the desired critical dimension.

The quality and uniformity of the spacers 60 directly affect the quality of the integrated circuits partially defined in the substrate 30 using the spacers as a mask. Where the desired spacers 60 are relatively wide compared to the mandrels 40 and/or the space separating the spacers 60, however, it has been observed that the resulting spacers 60 and the etch mask resulting from the spacers 60 can have poor uniformity. This poor uniformity, in turn, can cause poorly defined and non-uniform features to be formed in the substrate. As a result, the electrical performance of integrated circuits formed in the substrate may be degraded or the integrated circuits may be unusable.

Accordingly, there is a need for methods of forming etch masks having highly uniform and well-defined patterns, especially in conjunction with spacers formed in pitch multiplication.

Summary of the Invention

According to one aspect of the invention, a method is provided for fabricating an integrated circuit. The method comprises providing a substrate having an overlying mask layer. The mask layer comprises mask material and openings which form a pattern. The mask material is oxidized and the pattern is subsequently transferred to the substrate.

According to another aspect of the invention, a process is provided for forming an integrated circuit. The process comprises providing a pattern comprising a plurality of mask lines in a mask layer overlying a substrate. The mask lines comprise a precursor material. The mask lines are grown to a desired width by chemically reacting the precursor material to form a chemical compound occupying a larger volume than the precursor material.

According to another aspect of the invention, a process is provided for forming an integrated circuit. The process comprises providing a patterned mask layer overlying a substrate. The mask layer comprises a precursor material which is chemically reacted to form an etch stop material. The pattern in the mask layer is subsequently transferred to an underlying layer.

According to yet another aspect of the invention, a method of semiconductor processing is provided. The method comprises providing a substrate. A temporary layer overlies the substrate and a photodefinable layer overlies the temporary layer. A pattern is formed in the photodefinable layer and transferred to the temporary layer to form a plurality of placeholders in the temporary layer. A blanket layer of spacer material is deposited over the plurality of placeholders. The spacer material is selectively removed from horizontal surfaces. The placeholders are selectively removed relative to the spacer material. The spacer material is expanded to a desired size.

According to another aspect of the invention, a process is provided for forming a memory device. The process comprises forming a plurality of mask lines by pitch multiplication. Neighboring mask lines are separated from one another by an open space and the open space between neighboring mask lines is narrowed.

According to yet another aspect of the invention, a method is provided for semiconductor processing. The method comprises forming a plurality of mask lines by pitch multiplication. A volume of material forming the mask lines is expanded to a desired width by converting the material to an other material.

Brief Description of the Drawings

The invention will be better understood from the Detailed Description of the Preferred Embodiments and from the appended drawings, which are meant to illustrate and not to limit the invention, and wherein:

Figures 1A-1F are schematic, cross-sectional side views of mask lines, formed in accordance with a prior art pitch multiplication method;

Figure 2 is a schematic, cross-sectional side view of a partially formed memory device, in accordance with preferred embodiments of the invention;

Figure 3 is a schematic, cross-sectional side view of the partially formed memory device of Figure 2 after forming lines in a photo-definable layer, in accordance with preferred embodiments of the invention;

Figure 4 is a schematic, cross-sectional side view of the partially formed memory device of Figure 3 after widening spaces between photoresist lines, in accordance with preferred embodiments of the invention;

Figure 5 is a schematic, cross-sectional side view of the partially formed memory device of Figure 6 after etching through a hard mask layer, in accordance with preferred embodiments of the invention;

Figure 6 is a schematic, cross-sectional side view of the partially formed memory device of Figure 5 after transferring a pattern from the photoresist and hard mask layers to a temporary layer, in accordance with preferred embodiments of the invention;

Figure 7 is a schematic, cross-sectional side view of the partially formed memory device of Figure 6 after depositing a blanket layer of a spacer material, in accordance with preferred embodiments of the invention;

Figure 8 is a schematic, cross-sectional side view of the partially formed memory device of Figure 7 after a spacer etch, in accordance with preferred embodiments of the invention;

Figure 9 is a schematic, cross-sectional side view of the partially formed memory device of Figure 8 after being coated with a removable material, in accordance with preferred embodiments of the invention;

Figure 10 is a schematic, cross-sectional side view of the partially formed memory device of Figure 9 after etching the photoresist and hard mask layers, in accordance with preferred embodiments of the invention;

Figure 11 is a schematic, cross-sectional side view of the partially formed memory device of Figure 10 after removing the photoresist and temporary layers, in accordance with preferred embodiments of the invention;

Figure 12 is a schematic, cross-sectional side view of the partially formed memory device of Figure 11 after enlarging the spacers to a desired width, in accordance with preferred embodiments of the invention;

Figure 13 is a schematic, cross-sectional side view of the partially formed memory device of Figure 12 after transferring the spacer pattern to an underlying hard mask layer, in accordance with preferred embodiments of the invention;

Figure 14 is a schematic, cross-sectional side view of the partially formed memory device of Figure 13 after removing the spacers, in accordance with preferred embodiments of the invention;

Figure 15 is a schematic, cross-sectional side view of the partially formed memory device of Figure 1 having an additional masking layer, in accordance with preferred embodiments of the invention;

Figure 16 is a schematic, cross-sectional side view of the partially formed memory device of Figure 15 after forming spacers, in accordance with preferred embodiments of the invention;

Figure 17 is a schematic, cross-sectional side view of the partially formed memory device of Figure 16 after expanding spacers, in accordance with preferred embodiments of the invention;

Figure 18 is a schematic, cross-sectional side view of the partially formed memory device of Figure 17 after etching through a hard mask layer, in accordance with preferred embodiments of the invention;

Figure 19 is a schematic, cross-sectional side view of the partially formed memory device of Figure 18 after transferring the spacer pattern to the additional masking layer, in accordance with preferred embodiments of the invention;

Figure 20 is a schematic, cross-sectional side view of the partially formed memory device of Figure 6 after depositing a blanket layer of a spacer material, in accordance with other preferred embodiments of the invention;

Figure 21 is a schematic, cross-sectional side view of the partially formed memory device of Figure 20 after enlarging the blanket layer to a desired thickness, in accordance with other preferred embodiments of the invention; and

Figure 22 is a schematic, cross-sectional side view of the partially formed memory device of Figure 21 after removing the hard mask and temporary layers, in accordance with other preferred embodiments of the invention.

Detailed Description of the Preferred Embodiments

It has been found that the poor quality of some spacer patterns is due to difficulties depositing conformal layers of spacer material and/or etching this material to form spacers. Because spacers are typically formed out of the vertically extending parts of blanket layers of

spacer material over a complex mask topography, the conformality of the layers will affect the uniformity, *e.g.*, the widths, the heights and the physical placement, of the spacers formed from the layers. It will be appreciated that the more conformal a layer is, the more closely it replicates the shape of the surface on which it is deposited.

As critical dimensions continue to decrease, however, the aspect ratios of the spaces, or openings, between mandrels continue to increase. This is partly due to the desire to pack features more closely together by reducing the widths of the spaces between mandrels. In addition, in common methods of transferring patterns, both the spacers and an underlying layer are exposed to an etchant, which preferentially etches away the substrate material. The etchants, however, also wear away the spacers, albeit at a slower rate. Thus, even as critical dimensions decrease, the vertical heights of the spacers must remain at a level that allow a pattern transfer to be completed before the spacers are completely worn away by etchants.

Accordingly, deposition of highly conformal layers of spacer material can be increasingly difficult, due in part to increasingly limited diffusion of precursor gases into the bottom portions of the spaces between mandrels. This diffusion becomes increasingly more limited during the course of a deposition, as sidewalls fill in with spacer material, thereby further increasing the aspect ratios of the space between the sidewalls. For this reason, relatively thin layers are more easily and reliably deposited than relatively thick layers. As a result of poor conformality of relatively thick deposited layers, the uniformity of spacers formed from the layers can be also be poor.

In addition, just as it may be difficult for precursors to reach the bottoms of high aspect ratio spaces, the aspect ratios of some spaces can also limit the amount of etchant that penetrates to the bottoms of those spaces. Consequently, when etching laterally extending parts of the layer of spacer material to define individual spacers, some spacer material may undesirably remain at the bottoms of these spaces, causing the formation of spacers having bottom surfaces with widths different from expected widths. Thus, difficulties in depositing and also etching layers of spacer materials make precise control over the widths of the spacers difficult.

Advantageously, preferred embodiments of the invention allow for more precise control over the widths and uniformity of features formed using a mask pattern. In the preferred embodiments, the mask pattern is formed with a material that can itself be increased to a desired size or critical dimension by a subsequent process, such as oxidation. The mask pattern is then subjected to the expansion process to increase the widths of mask features to a desired width. The now-enlarged mask features can then be used to form a pattern in an underlying layer. As used herein, it will be appreciated that a "feature" refers to any volume or opening formed in a material, *e.g.*, in a mask layer or in the substrate, and having discrete boundaries.

Preferably, the pattern subjected to the enlargement process is a pattern of spacers formed by pitch multiplication. The spacers preferably comprise silicon, *e.g.*, polysilicon or amorphous silicon. The enlargement process can be any process that causes the spacers to expand. Where the spacers comprise silicon, the expansion process preferably comprises oxidation of the spacers to form silicon oxide. Moreover, the spacers are oxidized until they grow to a desired width. After growing to the desired width, the spacers can be used to pattern features in underlying layers. Optionally, the spacers can be trimmed to a desired critical dimension after being oxidized.

Advantageously, by growing the spacers to a desired width after they are formed, a thinner layer of spacer material can be deposited. By depositing thinner layers than would otherwise be required for a desired critical dimension, the conformality of the layers is less dependent upon the limitations of the deposition and/or etching process. As a result, the process window for forming spacers of a given critical dimension is widened.

In addition, as noted above, a spacer is typically formed to a particular height that is dictated in part by the requirements of a particular semiconductor process to be performed through the mask (*e.g.*, etching, implantation, doping, oxidation, etc.) and particular materials of the underlying substrate that are to be exposed to the process. For example, spacers are typically formed to a height that accounts for the removal of some material during subsequent etching of an underlying layer. Advantageously, because spacers typically grow both laterally and vertically during, *e.g.*, oxidation, the resulting taller spacers are less likely to be etched away when transferring the spacer pattern to an underlying layer. Also, because the initial height of the spacer formed by a spacer etch is dependent on the height of a mandrel, the mandrel's height can be less than the height that would be required if the spacers were not later enlarged. Consequently, because the height of the mandrels can be reduced, the aspect ratio of the spaces between the mandrels is also reduced, thereby further easing the requirements for the spacer material deposition and further increasing the process window.

It will be appreciated that silicon nitrides and silicon oxides are particularly suitable as spacer materials for mask formation, due in part to the availability of selective etch chemistries relative to a variety of other materials, including metals, oxides and silicon-containing substrates. Advantageously, the conversion of the silicon spacer into a silicon oxide allows preferred embodiments of the invention to be easily inserted into various process flows, especially for pitch multiplication, without needing to substantially alter the process flow. In addition, partial conversion of silicon spacers to silicon oxide still allows selective etch chemistries that will attack, *e.g.*, a carbon mask material without attacking either silicon oxide or residual silicon.

Reference will now be made to the Figures, wherein like numerals refer to like parts throughout. It will be appreciated that Figures 2-22 are not necessarily drawn to scale.

It will be also appreciated that, while the preferred embodiments will find application in any context in which it may be desirable to increase the size of the individual parts constituting a mask pattern after those parts are formed, in particularly advantageous embodiments the mask pattern comprises spacers formed by pitch multiplication. Thus, the pitch multiplied features preferably have a pitch below the minimum pitch of the photolithographic technique used for patterning the mandrels used to form the spacers. In addition, while the preferred embodiments can be used to form any integrated circuit, they are particularly advantageously applied to form devices having arrays of electrical devices, including logic or gate arrays and volatile and non-volatile memory devices such as DRAM, ROM or flash memory.

With reference to Figure 2, a partially formed integrated circuit 100 is provided. A substrate 110 is provided below various masking layers 120-150. The layers 120-150 will be etched to form a mask for patterning the substrate 110 to form various features, as discussed below.

It will be appreciated that the "substrate" can include a layer of a single material, a plurality of layers of different materials, a layer or layers having regions of different materials or structures in them, etc. These materials can include semiconductors, insulators, conductors, or combinations thereof. For example, the substrate can comprise doped polysilicon, an electrical device active area, a silicide, or a metal layer, such as a tungsten, aluminum or copper layer, or a combination thereof. Thus, the mask features discussed below can directly correspond to the desired placement of conductive features, such as interconnects, in the substrate. In other embodiments, the substrate can be an insulator and the location of mask features can correspond to the desired location of insulators.

The materials for the layers 120-150 overlying the substrate 110 are preferably chosen based upon consideration of the chemistry and process conditions for the various pattern forming and pattern transferring steps discussed herein. Because the layers between a topmost photodefinable layer 120 and the substrate 110 will function to transfer a pattern derived from the photodefinable layer 120 to the substrate 110, the layers between the photodefinable layer 120 and the substrate 110 are preferably chosen so that they can be selectively etched relative to other exposed materials. It will be appreciated that a material is considered selectively, or preferentially, etched when the etch rate for that material is at least about 5 times greater, preferably about 10 times greater and more preferably about 20 times greater than that for surrounding materials.

In the illustrated embodiment, the photodefinable layer 120 overlies a first hard mask, or etch stop, layer 130, which overlies a temporary layer 140, which overlies a second hard mask, or etch stop, layer 150, which overlies the substrate 110 to be patterned, *e.g.*, by etching through the second hard mask layer 150.

The photodefinable layer 120 is preferably formed of a photoresist, including any photoresist known in the art. For example, the photoresist can be any photoresist compatible with 157 nm, 193 nm or 248 nm wavelength sytems, 193 nm wavelength immersion systems or electron beam systems. Examples of preferred photoresist materials include argon fluoride (ArF) sensitive photoresist, *i.e.*, photoresist suitable for use with an ArF light source, and krypton fluoride (KrF) sensitive photoresist, *i.e.*, photoresist suitable for use with a KrF light source. ArF photoresists are preferably used with photolithography systems utilizing relatively short wavelength light, *e.g.*, 193 nm. KrF photoresists are preferably used with longer wavelength photolithography systems, such as 248 nm systems.

The material for the first hard mask layer 130 preferably comprises an inorganic material, and exemplary materials include silicon oxide (SiO_2), silicon or a dielectric anti-reflective coating (DARC), such as a silicon-rich silicon oxynitride. In the illustrated embodiment, the first hard mask layer 130 is a dielectric anti-reflective coating (DARC). The temporary layer 140 is preferably formed of amorphous carbon, which offers very high etch selectivity relative to the preferred hard mask materials. More preferably, the amorphous carbon is a form of amorphous carbon that is highly transparent to light and which offers further improvements in alignment. Deposition techniques for forming a highly transparent carbon can be found in A. Helmbold, D. Meissner, Thin Solid Films, 283 (1996) 196-203.

Because the preferred chemistries for etching photoresist also typically etch significant amounts of amorphous carbon and because chemistries are available for etching amorphous carbon with excellent selectivity relative to a variety of non-photoresist materials, the hard mask layer 130, selected from such materials, preferably separates the layers 120 and 140. As noted above, the first hard mask layer 130 preferably comprises silicon oxide, silicon or a DARC, which can be preferentially removed relative to amorphous carbon.

In addition, using DARCs for the first hard mask layer 130 can be particularly advantageous for forming patterns having pitches near the resolution limits of a photolithographic technique. The DARCs can enhance resolution by minimizing light reflections, which can decrease the precision with which photolithography can define the edges of a pattern. Optionally, a bottom anti-reflective coating (BARC) (not shown) can similarly be used in addition to the first hard mask layer 130 to control light reflections.

The second hard mask layer 150 preferably comprises a dielectric anti-reflective coating (DARC) (*e.g.*, a silicon oxynitride), silicon or aluminum oxide (Al_2O_3). In addition, a bottom anti-reflective coating (BARC) (not shown) can optionally be used to control light reflections. In the illustrated embodiment, the second hard mask layer 150 comprises Al_2O_3.

In addition to selecting appropriate materials for the various layers, the thicknesses of the layers 120-150 are preferably chosen depending upon compatibility with the etch chemistries and

process conditions described herein. For example, when transferring a pattern from an overlying layer to an underlying layer by selectively etching the underlying layer, materials from both layers are removed to some degree. Thus, the upper layer is preferably thick enough so that it is not worn away over the course of the pattern transfer.

In the illustrated embodiment, the photodefinable layer 120 is preferably between about 100 nm and about 300 nm thick and, more preferably, between about 150 nm and about 250 nm thick. The first hard mask layer 130 is preferably between about 10 nm and about 500 nm thick and, more preferably, between about 15 nm and about 300 nm thick. The temporary layer 140 is preferably between about 100 nm and about 300 nm thick and, more preferably, between about 100 nm and about 200 nm thick. The second hard mask layer 150 is preferably between about 10 nm and about 50 nm thick and, more preferably, between about 10 nm and about 30 nm thick.

It will be appreciated that the various layers discussed herein can be formed by various methods known to those of skill in the art. For example, various vapor deposition processes, such as chemical vapor deposition, can be used to form hard mask layers. Spin-on-coating processes can be used to form photodefinable layers. In addition, amorphous carbon layers can be formed by chemical vapor deposition using a hydrocarbon compound, or mixtures of such compounds, as carbon precursors. Exemplary precursors include propylene, propyne, propane, butane, butylene, butadiene and acetelyne. A suitable method for forming amorphous carbon layers is described in U.S. Patent No. 6,573,030 B1, issued to Fairbairn *et al.* on June 3, 2003.

In a first phase of methods in accordance with the preferred embodiments and with reference to Figures 3-11, a pattern of spacers is formed by pitch multiplication.

With reference to Figure 3, a pattern comprising spaces or trenches 122 delimited by photodefinable material features 124 is formed in the photodefinable layer 120. The trenches 122 can be formed by, *e.g.*, photolithography, in which the layer 120 is exposed to radiation through a reticle and then developed. After being developed, the remaining photodefinable material, photoresist in the illustrated embodiment, forms features such as the illustrated lines 124 (shown in cross-section only).

The pitch of the resulting lines 124 and spaces 122 is equal to the sum of the width of a line 124 and the width of a neighboring space 122. To minimize the critical dimensions of features formed using this pattern of lines 124 and spaces 122, the pitch is preferably at or near the limits of the photolithographic technique used to pattern the photodefinable layer 120. Thus, the pitch may be at the minimum pitch of the photolithographic technique and the spacer pattern discussed below can advantageously have a pitch below the minimum pitch of the photolithographic technique.

As shown in Figure 4, the spaces 122 can optionally be widened by etching the photoresist lines 124, to form modified spaces 122a and lines 124a. The photoresist lines 124 are

preferably etched using an isotropic etch, such as a sulfur oxide plasma, *e.g.*, a plasma comprising SO_2, O_2, N_2 and Ar. The extent of the etch is preferably selected so that the widths of the spaces 122a and the lines 124a are substantially equal to the desired spacing between the later-formed spacers, as will be appreciated from the discussion of Figures 8-10 below. Advantageously, this etch allows the lines 124a to be narrower than would be possible with using the photolithographic technique used to pattern the photodefinable layer 120. In addition, the etch can smooth the edges of the lines 124a, thus improving the uniformity of those lines 124a.

The pattern in the (modified) photodefinable layer 120 is preferably transferred to the temporary layer 140 to allow for deposition of a layer 170 of spacer material (Figure 7). Thus, the temporary layer 140 is preferably formed of a material that can withstand the process conditions for spacer material deposition, discussed below. In other embodiments where the deposition of spacer material is compatible with the photodefinable layer 120, the temporary layer 140 can be omitted and the spacer material can be deposited directly on the photo-defined features 124 or the modified photodefined features 124a of the photodefinable layer 120 itself.

In the illustrated embodiment, in addition to having higher heat resistance than photoresist, the material forming the temporary layer 140 is preferably selected such that it can be selectively removed relative to the material for the spacers 175 (Figures 8) and the underlying etch stop layer 150. As noted above, the layer 140 is preferably formed of amorphous carbon.

The pattern in the photodefinable layer 120 is preferably first transferred to the hard mask layer 130, as shown in Figure 5. This transfer is preferably accomplished using an anisotropic etch, such as an etch using a fluorocarbon plasma, although a wet (isotropic) etch may also be suitable if the hard mask layer 130 is thin. Preferred fluorocarbon plasma etch chemistries include CF_4, CFH_3, CF_2H_2 and CF_3H.

The pattern in the photodefinable layer 120 is then transferred to the temporary layer 140, as shown in Figure 6, preferably using a SO_2-containing plasma, *e.g.*, a plasma containing SO_2, O_2 and Ar. Advantageously, the SO_2-containing plasma can etch carbon of the preferred temporary layer 140 at a rate greater than 20 times and, more preferably, greater than 40 times the rate that the hard mask layer 130 is etched. A suitable SO_2-containing plasma is described in U.S. Patent Application No. 10/931,772 of Abatchev *et al.*, filed August 31, 2004, entitled Critical Dimension Control. It will be appreciated that the SO_2-containing plasma can simultaneously etch the temporary layer 140 and also remove the photodefinable layer 120. The resulting lines 124b constitute the placeholders or mandrels with which a pattern of spacers 175 (Figure 8) will be formed.

Next, as shown in Figure 7, a layer 170 of spacer material is preferably blanket deposited conformally over exposed surfaces, including the hard mask layer 130, the hard mask 150 and the sidewalls of the temporary layer 140. Optionally, the hard mask layer 130 can be removed before

depositing the layer 170. The spacer material can be any material that can act as a mask for transferring a pattern to the underlying substrate 110, or that otherwise can allow processing of underlying structures through the mask being formed. The spacer material preferably: 1) can be deposited with good step coverage; 2) can be deposited at a temperature compatible with the temporary layer 140; 3) can be further processed to enlarge its dimensions; and 4) can be selectively etched relative to the temporary layer 140 and any layer underlying the temporary layer 140 after being enlarged. Preferred materials include polysilicon and amorphous silicon. The layer 170 is preferably deposited to a thickness of between about 20 nm to about 60 nm and, more preferably, about 20 nm to about 50 nm. Preferably, the step coverage is about 80 % or greater and, more preferably, about 90 % or greater.

As shown in Figure 8, the spacer layer 170 is then subjected to an anisotropic etch to remove spacer material from horizontal surfaces 180 of the partially formed integrated circuit 100. Such an etch, also known as a spacer etch, can be performed using HBr/Cl plasma. The etch can include a physical component and preferably also includes a chemical component, *e.g.*, a reactive ion etch (RIE), such as a Cl_2, HBr etch. Such an etch can be performed, for example, using a LAM TCP9400 flowing about 0-50 sccm Cl_2 and about 0-200 sccm HBr at about 7-60 mTorr pressure with about 300-1000 W top power and about 50-250 W bottom power.

The hard mask layer 130 (if still present) and the temporary layer 140 are next removed to leave free standing spacers 175 (Figure 11). Because the spacers 175 may be thin and because the hard mask layer 130 may be formed of a material similar to the spacers 175, a space-fill layer 155 may be formed over and around the spacers 175 to help maintain the structural integrity of the spacers 175 and to aid in etching the layers 130 and 140, as shown in Figure 9. Preferably, the layer 155 comprises photoresist, which can be deposited in a spin-on process. In other embodiments, *e.g.*, where the spacers 175 are sufficiently wide and where adequate etch chemistries are available, the layers 130 and 140 may be removed without deposition of the layer 155.

With reference to Figure 10, the hard mask layer 130, along with a top portion of the space-fill layer 155, is removed, for example, by planarization. Preferred chemistries for etching the layers 130 and 155 include a two step etch: first using CF_4/He plasma until the layer 130 (Figure 9) is removed and then using an O_2 plasma to remove the temporary layer 140, along with a remaining portion of the space-fill layer 155. The resulting structure is shown in Figure 11. Alternatively, to remove the layer 130 in the first part of the etch, the layers 130 and 155 can be subjected to chemical mechanical polishing.

Thus, a pattern of freestanding spacers 175 is formed. Preferred chemistries for etching the layers 140 and 155 include a sulfur oxide plasma etch. Advantageously, silicon is more readily etched, either isotropically and anisotropically, than materials, such as silicon nitrides or

silicon oxides, that are typically used for spacers. In some embodiments, the critical dimension of the spacers 175 is adjusted after the spacer etch by trimming the spacers 175.

Thus, pitch multiplication has been accomplished. In the illustrated embodiment, the pitch of the spacers 175 is roughly half that of the photoresist lines 124 (Figure 3) originally formed by photolithography. Advantageously, spacers 175 having a pitch of about 100 nm or less can be formed. It will be appreciated that because the spacers 175 are formed on the sidewalls of the features or lines 124b, the spacers 175 generally follow the outline of the pattern of features or lines 124 originally formed in the photodefinable layer 120.

Next, in a second phase of methods according to the preferred embodiments, the spacers 175 are enlarged so that their widths correspond to the desired critical dimensions of features that are to be formed in the substrate 110. Preferably, this enlargement is accomplished by reacting the spacers 175 to form a new compound or alloy occupying more space. In the illustrated embodiment having spacers formed of silicon, the enlargement process preferably comprises oxidation of the spacers. It will be appreciated that the spacers 175 grow upon being oxidized, as shown in Figure 12. The size of the spacers 175a will vary depending upon the extent to which the spacers 175 are oxidized. Thus, the duration and degree of the oxidation is preferably chosen so that the spacers 175 reach a desired width 95. The oxidation of the spacers 175 can be accomplished by any oxidation process known in the art, including thermal oxidation, oxidation using oxygen radicals or plasma, etc. In other embodiments, the spacers 175 can be enlarged by being nitrided by any nitridation process known in the art. Thus, a pattern of spacers 175a having desired widths 95 can be formed.

It will be appreciated that the spacers 175 can be formed of any material that can be expanded, can be conformally deposited and for which suitable etch chemistries are available. For example, the spacers 175 can be formed using titanium and can be enlarged by oxidation or nitridation to form TiO_2 or TiN_2. Other examples of materials include tantalum (which can be expanded by oxidation or nitridation to form tantalum oxide or tantanlum nitride) and tungsten (which can be expanded by oxidation or nitridation to form tungsten oxide or tungsten nitride).

Preferably, the extent of the enlargement is chosen such that the spacers 175 are enlarged to a width substantially equal to the desired critical dimension of the features, such as interconnects, word lines, bit lines, transistor rows, or gaps between damascene lines, which will be patterned in the substrate 110 using the pattern formed by the spacers 175a. For example, the spacers 175a can be oxidized to a greater or less extent, depending upon whether the desired critical dimensions are only slightly or more substantially greater than the dimensions of the non-oxidized spacers 175. Thus, process conditions, such as duration, chemical reactivity, temperature, etc., are chosen to achieve the desired degree of spacer expansion.

It will be appreciated that growth of the spacers 175 will also narrow the space separating those spacers 175. Preferably, the spacers 175 are positioned to account for this narrowing. In addition, the critical dimension of the spacers 175a can adjusted after the expansion by trimming the spacers 175a, *e.g.*, with an isotropic etch.

It will also be appreciated that the spacers 175a themselves may be used directly as a hard mask to pattern an underlying substrate 110. Preferably, however, the pattern of the spacers 175a is transferred to one or more underlying layers which offer better etch selectivity to the substrate 110 than the spacers 175a. With reference to Figure 13, the pattern made out by the spacers 175a can be transferred to the second hard mask layer 150. Preferably, the second hard mask layer 150 is etched using a BCl_3/Cl_2 plasma etch.

With reference to Figure 14, the spacers 175a can optionally be removed before patterning the substrate 110. The spacers 175a can be removed using a wet etch process. Advantageously, by removing the spacers 175a, the aspect ratio of the mask overlying the substrate 110 is reduced, thereby allowing etchants other processing chemicals to more easily reach the substrate and, so, improving the formation of vertical sidewalls or otherwise clearly delineating and completing processing.

In other embodiments, as shown in Figure 15, an additional mask layer 160 can be utilized to pattern difficult to pattern substrates 110. Such substrates can include, for example, multiple layers, which require multiple successive etches to pattern. Due to the availability of chemistries that allow very selective removal of amorphous carbon relative to many silicon-containing substrate materials, the additional mask layer 160 is preferably formed of amorphous carbon.

It will be appreciated that the steps discussed above may be applied to form spacers 175a overlying the additional mask layer 160. With reference to Figure 16, a pattern of spacers 175 is formed. As shown in Figure 17, the spacers 175 are then expanded, by, *e.g.*, oxidation, to a desired width, as discussed above. The pattern of spacers 175a can then be transferred to the second hard mask layer 150, preferably using a BCl_3/Cl_2 plasma etch, as shown in Figure 18. The pattern is then transferred to the additional mask layer 160, preferably by anisotropically etching the additional mask layer 160, as shown in Figure 19. Preferably, the anisotropic etch is comprises exposing the additional mask layer 160 to a SO_2-containing plasma. In other embodiments, it will be appreciated that the spacers 175 may be removed before etching the layer 150 or before etching the substrate 110, as discussed above with respect to Figure 14.

The substrate 110 can then be processed through the mask layers 160 and 150 and the spacers 175a to define various features, *e.g.*, transistors, capacitors and/or interconnects. Where the substrate 110 comprises layers of different materials, a succession of different chemistries, preferably dry-etch chemistries, can be used to successively etch through the different layers. It

will be appreciated that, depending upon the chemistry or chemistries used, the spacers 175a and the hard mask layer 150 may be etched. Amorphous carbon of the additional mask layer 160, however, advantageously offers excellent resistance to conventional etch chemistries, especially those used for etching silicon-containing materials. Accordingly, the additional mask layer 160 can effectively be used as a mask for etching through a plurality of substrate layers, or for forming high aspect ratio trenches. The additional mask layer 160 can later be removed for further processing of the substrate 110.

It will be appreciated that, in any of the steps described herein, transferring a pattern from a first level to a second level involves forming features in the second level that generally correspond to features on the first level. For example, the path of lines in the second level will generally follow the path of lines on the first level and the location of other features on the second level will correspond to the location of similar features on the first level. The precise shapes and sizes of features can vary from the first level to the second level, however. For example, depending upon etch chemistries and conditions, the sizes of and relative spacings between the features forming the transferred pattern can be enlarged or diminished relative to the pattern on the first level, while still resembling the same initial "pattern." Thus, the transferred pattern is still considered to be the same pattern as the initial pattern. In contrast, forming spacers around mask features can change the pattern.

It will be appreciated that formation of contacts according to the preferred embodiments offers numerous advantages. For example, because thinner layers are more easily conformally deposited than thicker layers, the layers of spacer material from which spacers are formed can be deposited with improved conformality. As a result, spacers can be formed from these layers with improved uniformity. Moreover, the relative thinness of these layers reduces the aspect ratios of trenches lined with the blanket layer of spacer material, thereby allowing etchants to more easily penetrate to the bottom of the trenches and, thus, facilitating the spacer etch.

It will also be appreciated that various modifications of the illustrated embodiments are possible. For example, the pitch of the spacers 175 or 175a can be more than doubled. Further pitch multiplication can be accomplished by forming additional spacers around the spacers 175 or 175a, then removing the spacers 175 or 175a, then forming spacers around the spacers that were formerly around the spacers the 175 or 175a, and so on. An exemplary method for further pitch multiplication is discussed in U.S. Patent No. 5,328,810 to Lowrey *et al.*

In addition, various other patterns, for patterning features of different sizes, can be overlaid or formed adjacent to the spacers 175 or 175a. For example, an additional photodefinable layer can be formed overlying the spacers 175 or 175a and then patterned to form the other patterns. Methods for forming such patterns are disclosed in U.S. Patent Application

No. 10/931,771 of Tran *et al.*, filed August 31, 2004, entitled Methods for Increasing Photo-Alignment Margins.

Moreover, while all the spacers 175 can be oxidized to have a similar width, in other embodiments, only some of the spacers 175 may be oxidized. For example, some spacers 175 can be protected from oxidation by depositing and patterning a protective layer (for which selective etch chemistries are available) and then oxidizing exposed spacers.

In addition, depending upon the material being converted and the extent of the conversion process, the oxidation or subsequent chemical conversion process may not appreciably increase the size of the spacers 175. In such case, the processes disclosed herein can nevertheless be applied to convert the spacers 175 to a material for which highly selective etch chemistries are available. As such, the conversion process can advantageously convert the spacers 175 to a better etch stop for subsequent etch steps. For example, a mask precursor material can be converted to a silicon or metal oxide or nitride, which can advantageously provide good etch selectivity to surrounding, *i.e.*, underlying, materials.

With reference to Figures 20-22, where the spacers 175 are enlarged, it will be appreciated that the spacers 175 or the layer 170 can be enlarged, *e.g.*, by oxidation, at any point after deposition of the spacer material and before forming the free-standing spacers 175. For example, after depositing a blanket layer of spacer material 170 (Figure 20), the entire blanket layer 170 can be expanded, as shown in Figure 21 to form an expanded blanket layer 170a. As noted above, the expansion process, including process conditions (*e.g.*, duration, chemical reactivity, temperature, etc.), is preferably chosen such that the blanket layer 170 expands to a desired thickness corresponding to a desired critical dimension, taking into account any horizontal shrinkage during the subsequent spacer etch. Thus, the expansion process may leave the layer 170 only partially oxidized. As shown in Figure 22, after a spacer etch, the mandrels 124b are then removed to leave the free-standing spacers 175a. Advantageously, because the spacers 175a are thicker than the spacers 175, a protective space-fill layer 155 (Figure 9) may not necessary and the mandrels 124b can be etched using an anisotropic etch, *e.g.*, using a fluorocarbon plasma.

In other embodiments, the spacers 175 can be expanded after the spacer etch and before etching the mandrels (*e.g.*, the spacers 175 in the Figure 8 can be expanded). Advantageously, because the spacers 175 are allowed to grow laterally in only one direction, this type of expansion allows the distance between individual pairs of spacers 175 to be maintained constant, while reducing the distance between the constituent spacers of a pair of spacers 175. As noted above, however, the expansion step is preferably performed after forming the spacers 175 as freestanding structures, to facilitate etching of the layer 170.

Also, while "processing" through the various mask layers preferably involve etching an underlying layer, processing through the mask layers can involve subjecting layers underlying the mask layers to any semiconductor fabrication process. For example, processing can involve doping, oxidation, nitridation or depositing materials through the mask layers and onto underlying layers.

Accordingly, it will be appreciated by those skilled in the art that various other omissions, additions and modifications may be made to the methods and structures described above without departing from the scope of the invention. All such modifications and changes are intended to fall within the scope of the invention, as defined by the appended claims.

WE CLAIM:

1. A method for fabricating an integrated circuit, comprising:

providing a substrate having an overlying mask layer, the mask layer comprising mask material and openings, the mask material and openings forming a pattern;

oxidizing the mask material; and

transferring the pattern to the substrate after oxidizing the mask material.

2. The method of Claim 1, wherein transferring the oxidized mask pattern comprises etching the semiconductor substrate through the openings in the mask layer.

3. The method of Claim 1, wherein the mask layer comprises polysilicon or amorphous silicon.

4. The method of Claim 3, wherein oxidizing the mask layer comprises forming silicon oxide.

5. The method of Claim 3, wherein oxidizing the mask layer comprises partially oxidizing the mask layer.

6. The method of Claim 1, wherein oxidizing the mask layer comprises enlarging the mask material to a desired width corresponding to a desired critical dimension of a feature in the integrated circuit.

7. The method of Claim 6, wherein the desired critical dimension is a width of conductive interconnects in the integrated circuit.

8. The process of Claim 1, wherein the substrate comprises a plurality of layers of different materials.

9. The method of Claim 8, wherein transferring the pattern to the semiconductor substrate comprises employing a different etch chemistry for each of the plurality of layers.

10. The method of Claim 1, wherein the substrate is an insulator.

11. The method of Claim 10, wherein transferring the pattern to the semiconductor substrate defines conductive lines of an array of a memory device.

12. The method of Claim 1, wherein providing a substrate comprises forming a pattern of spacers by pitch multiplication, wherein the mask material comprises the spacers.

13. A process for forming an integrated circuit, comprising:

providing a pattern comprising a plurality of mask lines in a mask layer overlying a substrate, the mask lines comprising a precursor material; and

growing the mask lines to a desired width by chemically reacting the precursor material to form a chemical compound occupying a larger volume than the precursor material.

14. The process of Claim 13, wherein growing the mask lines comprises performing a thermal oxidation.

15. The process of Claim 13, wherein the plurality of mask lines is formed by pitch multiplication.

16. The process of Claim 13, wherein the mask lines comprise silicon.

17. The process of Claim 13, wherein an amorphous carbon is disposed between the mask layer and the substrate.

18. The process of Claim 13, further comprising transferring the pattern to a hard mask layer between the mask layer and the substrate after growing the mask lines.

19. The process of Claim 18, wherein the hard mask layer comprises aluminum oxide.

20. The process of Claim 19, wherein transferring the pattern to a hard mask layer comprises etching the hard mask layer with BCl_3/Cl_2 plasma.

21. The process of Claim 18, further comprising selectively removing the mask layer relative to the hard mask layer after transferring the pattern to a hard mask layer.

22. The process of Claim 18, further comprising transferring the pattern to an additional mask layer between the hard mask layer and the substrate after transferring the pattern to a hard mask layer.

23. The process of Claim 22, wherein the additional mask layer comprises amorphous carbon.

24. The process of Claim 13, wherein the desired width corresponds to a critical dimension of conductive lines to be formed in the substrate.

25. A process for forming an integrated circuit, comprising:

providing a patterned mask layer overlying a substrate, the mask layer comprising a precursor material;

chemically reacting the precursor material to form an etch stop material; and

subsequently transferring the pattern in the mask layer to an underlying layer.

26. The process of Claim 25, wherein chemically converting enlarges a volume of the precursor material.

27. The process of Claim 26, wherein chemically converting comprises performing a thermal oxidation.

28. The process of Claim 25, wherein the patterned mask layer comprises a plurality of mask lines formed by pitch multiplication.

29. The process of Claim 25, wherein the precursor material is selected from the group consisting of silicon, titanium, tantalum and tungsten.

30. The process of Claim 29, wherein the etch stop material comprises an oxide or a nitride.

31. The process of Claim 25, wherein an amorphous carbon is disposed between the mask layer and the substrate and wherein subsequently transferring comprises transferring the pattern to the amorphous carbon layer.

32. The process of Claim 25, wherein transferring the pattern to the amorphous carbon layer comprises performing a SO_2 plasma etch.

33. A method of semiconductor processing, comprising:

providing a substrate, wherein a temporary layer overlies the substrate and a photodefinable layer overlies the temporary layer;

forming a pattern in the photodefinable layer;

transferring the pattern to the temporary layer to form a plurality of placeholders in the temporary layer;

depositing a blanket layer of spacer material over the plurality of placeholders;

selectively removing the spacer material from horizontal surfaces;

selectively removing the placeholders relative to the spacer material; and

expanding the spacer material to a desired size.

34. The method of Claim 33, wherein selectively removing the placeholders forms a pattern of free-standing spacers and wherein expanding the spacer material is performed after selectively removing the placeholders.

35. The method of Claim 33, wherein expanding the spacer material is performed before selectively removing the spacer material from horizontal surfaces.

36. The method of Claim 33, wherein expanding the spacer material is performed after selectively removing the spacer material from horizontal surfaces and before selectively removing the placeholders.

37. The method of Claim 33, wherein the temporary layer comprises amorphous carbon.

38. The method of Claim 37, wherein the photodefinable layer comprises photoresist.

39. The method of Claim 38, wherein forming a pattern in the photodefinable layer comprises performing photolithography and subsequently isotropically etching the photodefinable layer.

40. The method of Claim 38, wherein a hard mask layer separates the temporary layer and the photodefinable layer.

41. The method of Claim 40, wherein the hard mask layer comprises a dielectric antireflective coating.

42. The method of Claim 41, wherein the dielectric antireflective coating comprises silicon oxynitride.

43. The method of Claim 41, wherein selectively removing the placeholders comprises:

depositing a filler material over and around the spacer material;

simultaneously etching the filler material and the hard mask layer; and

subsequently simultaneously etching the filler material and the temporary layer.

44. The method of Claim 43, wherein depositing a filler material comprises depositing photoresist.

45. The method of Claim 44, wherein depositing photoresist comprises performing a spin-on process.

46. The method of Claim 43, wherein simultaneously etching the filler material and the hard mask layer comprises performing a CF_4/He plasma etch.

47. The method of Claim 43, wherein subsequently simultaneously etching the filler material and the temporary layer comprises performing an O_2 plasma etch.

48. The method of Claim 33, wherein depositing a blanket layer of spacer material comprises depositing a layer of silicon by chemical vapor deposition.

49. The method of Claim 48, wherein expanding the spacer material comprises forming silicon oxide.

50. The method of Claim 48, wherein selectively removing the spacer material from horizontal surfaces comprises anisotropically etching the silicon layer.

51. The method of Claim 50, wherein anisotropically etching the silicon layer comprises etching the silicon layer with HBr/Cl_2 plasma.

52. A process for forming a memory device, comprising:

forming a plurality of mask lines by pitch multiplication, wherein neighboring mask lines are separated from one another by an open space; and

narrowing the open space between neighboring mask lines.

53. The process of Claim 52, wherein the mask lines comprise polysilicon or amorphous silicon.

54. The process of Claim 52, wherein narrowing the open space comprises reacting the mask lines to form a different chemical compound or alloy.

55. The process of Claim 54, wherein reacting the mask lines comprises expanding the mask lines by oxidation.

56. The process of Claim 55, wherein reacting the mask lines comprises completely oxidizing the mask lines.

57. The process of Claim 52, further comprising transferring a pattern formed by the mask lines to an underlying layer.

58. The process of Claim 57, wherein the underlying layer comprises amorphous carbon.

59. The process of Claim 58, wherein transferring the pattern to the amorphous carbon layer comprises transferring the pattern to a hard mask layer and then transferring the pattern from the hard mask layer to the amorphous carbon layer.

60. The process of Claim 59, wherein transferring the pattern to a hard mask layer comprises etching the hard mask layer with a BCl_3/Cl_2 plasma.

61. The process of Claim 59, wherein transferring the pattern from the hard mask layer to the amorphous carbon layer comprises exposing the amorphous carbon layer to SO_2-containing plasma.

62. A method for semiconductor processing, comprising:

forming a plurality of mask lines by pitch multiplication; and

expanding a volume of material forming the mask lines to a desired width by converting the material to an other material.

63. The method of Claim 62, wherein expanding a volume of material forming the mask lines comprises expanding a blanket layer of spacer material during forming a plurality of mask lines pitch multiplication.

64. The method of Claim 63, wherein comprising:

forming a plurality of mandrels;

depositing the blanket layer of the spacer material;

expanding the spacer material; and

etching horizontal surfaces to form spacers from the blanket layer of spacer material after expanding the spacer material, wherein the spacers form the mask lines.

65. The method of Claim 63, wherein forming a plurality of mask lines comprises:

forming a plurality of mandrels;

depositing the blanket layer of the spacer material;

etching horizontal surfaces to form spacers from the blanket layer of spacer material, wherein the spacers form the mask lines;

expanding the spacer material after etching horizontal surfaces; and

subsequently preferentially removing the mandrels relative to the spacer material after expanding.

66. The method of Claim 62, wherein expanding a volume of material forming the mask lines comprises expanding a pattern of spacers after pitch multiplication.

67. The method of Claim 62, wherein converting the material to an other material comprises oxidizing the material forming the mask lines.

68. The method of Claim 62, wherein converting the material to an other material comprises nitriding the material forming the mask lines.

69. The method of Claim 62, further comprising exposing an underlying layer to reactants through openings between the mask lines.

70. The method of Claim 69, wherein the reactants are etchants.

71. The method of Claim 70, wherein exposing an underlying layer comprises etching amorphous carbon.

72. The method of Claim 70, wherein exposing an underlying layer comprises etching a conductive substrate.

73. The method of Claim 62, further comprising trimming the mask lines after expanding a volume of material forming the mask lines.

74. The method of Claim 62, wherein the mask lines comprise polysilicon or amorphous silicon.

75. The method of Claim 62, wherein the desired width is a critical dimension of conductive interconnect lines in an integrated circuit.