WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor package, the method comprising:

preparing a panel package, the panel package including a redistribution substrate, a connection substrate on the redistribution substrate, a plurality of lower semiconductor chips on the redistribution substrate, and a lower molding layer covering the lower semiconductor chips and the connection substrate;

sawing the panel package to form a plurality of strip packages separated from each other, each of the strip packages including a sawed portion of the redistribution substrate, at least two of the lower semiconductor chips, and a sawed portion of the connection substrate;

providing a plurality of upper semiconductor chips on one of the strip packages and electrically connecting the upper semiconductor chips to the sawed portion of the connection substrate of the one of the strip packages; and

forming an upper molding layer on the one of the strip packages to cover the upper semiconductor chips; and

sawing the one of the strip packages and the upper molding layer to form a plurality of separated packages after the forming the upper molding layer.

2. The method of claim 1, wherein the electrically connecting the upper semiconductor chips to the sawed portion of the connection substrate comprises forming a plurality of first connection terminals that are directly coupled to chip pads of the upper semiconductor chips and to upper pads of the connection substrate

of the one of the strip packages.

3. The method of claim 1 or claim 2, wherein the preparing the panel package comprises:

providing the connection substrate on a temporary substrate, the connection substrate having a plurality of holes;

providing the lower semiconductor chips on the temporary substrate, the lower semiconductor chips being disposed in the holes of the connection substrate;

forming the lower molding layer on the temporary substrate to cover the lower semiconductor chips and the connection substrate; and

removing the temporary substrate to expose bottom surfaces of the lower semiconductor chips and a bottom surface of the connection substrate.

4. The method of claim 3, wherein the preparing the panel package further comprises forming the redistribution substrate on the bottom surfaces of the lower semiconductor chips and the bottom surface of the connection substrate exposed by the removing the temporary substrate.

5. The method of claim 3 or claim 4, wherein the upper molding layer directly contacts the lower molding layer.

6. The method of any one of claims 1 to 5, wherein the connection substrate comprises:

a plurality of base layers;

a connection line pattern between the base layers;

a plurality of vias penetrating the base layers and coupled to the connection line pattern;

an upper pad exposed on a top surface of the connection substrate and coupled to at least one of the vias; and

a lower pad exposed on a bottom surface of the connection substrate and coupled to another one of the vias.

7. The method of claim 6, wherein the upper pad is not vertically aligned with the lower pad.

8. The method of any one of claims 1 to 7, wherein the preparing the panel package comprises:

forming a plurality of first connectors between the redistribution substrate and the lower semiconductor chips; and

forming a plurality of second connectors between the redistribution substrate and the connection substrate,

wherein the first connectors include solder balls, bumps, or pillars, and

wherein the second connectors include solder balls, bumps, or pillars.

9. A method of fabricating a semiconductor package, the method comprising:

preparing a panel package;

preparing a plurality of strip packages, by sawing the panel package to

form the plurality of strip packages separated from each other, each of the strip packages including a redistribution substrate, a connection substrate on the redistribution substrate, a plurality of lower semiconductor chips mounted on the redistribution substrate, and a lower molding layer covering the lower semiconductor chips;

placing a plurality of upper semiconductor chips on one of the strip packages, at least two of the upper semiconductor chips being laterally spaced apart from each other; and

forming a plurality of connection terminals directly connected to the upper semiconductor chips and the connection substrate,

forming an upper molding layer on the one of the strip packages to cover the upper semiconductor chips after the forming the plurality of connection terminals; and

sawing the one of the strip packages and the upper molding layer to provide separate packages after the forming the upper molding layer.

10. The method of claim 9, wherein the connection substrate includes a plurality of upper pads directly coupled to the connection terminals,

wherein the preparing the plurality of strip packages includes forming a plurality of openings in the lower molding layer to expose the upper pads.

11. The method of claim 10, wherein the forming the openings is performed by a laser drilling process,

wherein widths of the openings are equal to or less than widths of the

upper pads.

12. The method of claim 10, wherein the forming the openings includes performing a photolithography process on the lower molding layer.

13. The method of any one of claims 10 to 12, wherein one of the openings exposes two or more of the upper pads.

14. The method of any one of claims 9 to 13, wherein the upper molding layer directly physically contacts a top surface of the lower molding layer.

15. The method of any one of claims 9 to 14, wherein each of the separated packages includes at least one of the lower semiconductor chips and at least one of the upper semiconductor chips.

16. The method of claim 15, further comprising forming a shield layer on at least one of the separated packages to cover the lower molding layer.

17. A method of fabricating a semiconductor package, the method comprising:

forming a first preliminary package;

forming a plurality of second preliminary packages, by performing a first sawing process on the first preliminary package to form the plurality of second preliminary packages separated from each other;

mounting a plurality of upper semiconductor chips on one of the second preliminary packages, at least two of the upper semiconductor chips being laterally spaced apart from each other; and

performing a second sawing process on the one of the second preliminary packages to provide separate packages,

wherein forming the first preliminary package comprises:

providing a connection substrate on a temporary substrate,

providing a plurality of lower semiconductor chips on the temporary substrate,

forming a lower molding layer on the temporary substrate to cover the lower semiconductor chips and the connection substrate,

removing the temporary substrate to expose bottom surfaces of the lower semiconductor chips and a bottom surface of the connection substrate, and

forming a redistribution substrate on the bottom surfaces of the lower semiconductor chips and the bottom surface of the connection substrate exposed by the removing the temporary substrate,

wherein the method further comprises:

forming an upper molding layer on the one of the second preliminary packages to cover the upper semiconductor chips, and

wherein the performing the second sawing process comprises:

sawing the one of the second preliminary packages and the upper molding layer to provide the separate packages after the forming the upper molding layer.

18. The method of claim 17, wherein the forming the plurality of second preliminary packages includes performing the first sawing process on the first preliminary package including the redistribution substrate and the connection substrate.

19. The method of claim 18, wherein the second sawing process is performed after the first sawing process.