SYSTEMS AND DEVICES INCLUDING FIN TRANSISTORS AND METHODS OF USING, MAKING, AND OPERATING THE SAME

Field of Invention

[0001] Embodiments of the present invention relate generally to electronic devices and, more specifically, in certain embodiments, to fin transistors.

Description of Related Art

[0002] Fin field-effect transistors (finFETs) are often built around a fin (e.g., a tall, thin semiconductive member) extending generally perpendicularly from a substrate. Typically, a gate traverses the fin by conformally running up one side of the fin, over the top, and down the other side of the fin. In some instances, the gate is disposed against the sides of the fin and does not extend over the top. Generally, a source and a drain are located on opposite sides of the gate near the ends of the fin. In operation, a current through the fin between the source and drain is controlled by selectively energizing the gate.

[0003] Some finFETs include gates formed with a sidewall-spacer process. In some versions of this process, the gates are formed by covering a fin with a conformal, conductive film and, then, anisotropically etching the conductive film. During the etch, the conductive material is removed faster from the horizontal surfaces than from the vertical surfaces. As a result, a portion of the conductive material remains against the vertical sidewalls of the fins.

An advantage of this process is that relatively narrow gates can be formed relative to gates patterned with photolithography, which is often subject to alignment and resolution constraints.

[0004] Although forming gates with a sidewall-spacer process avoids some process issues, it can introduce other failure mechanisms. Often the sidewalls of the fins are angled rather than vertical because the fins were formed with an etch step that was less than perfectly anisotropic. These angled sidewalls can narrow, and in some cases close, the process window for the sidewall spacer process. The angles place the bases of adjacent fins closer to one another, and when the conformal film is deposited in this narrower gap, the portions of the film covering the adjacent sidewalls can join, creating a film with a larger vertical thickens in the gap. The film can become so thick in the gap that the sidewall-spacer etch does not remove all of the conductive film between adjacent gates. The resulting conductive residue forms stringers that short adjacent finFETs and lower yields.

BRIEF DESCRIPTION OF DRAWINGS

[0005] FIGS. 1-22 are cross-sectional views of a substrate during sequential stages of a manufacturing process in accordance with an embodiment of the present technique.

DETAILED DESCRIPTION

[0006] The problems discussed above may be mitigated by some of the subsequently described embodiments. Among these embodiments is an example of a manufacturing process

that forms insulating fins between adjacent gates. As explained below, in some embodiments, both insulating fins and semiconductor fins are formed by a single etch that defines furrows between the insulating fins and semiconductor fins. The furrows, in turn, may define the shape and position of gates formed in the furrows. Because the gates are formed in furrows separated by insulating fins, in some embodiments, the gates are believed to be more reliably isolated from one another than gates formed with conventional techniques. This manufacturing process and some of its variants are described below with reference to FIGS. 1-22.

[0007] As illustrated by FIG. 1, the manufacturing process begins with providing a substrate 102. The substrate 102 may include semiconductive materials such as single-crystal or poly-crystalline silicon, gallium arsenide, indium phosphide, or other materials with semiconductor properties. Alternately, or additionally, the substrate 102 may include a non-semiconductor body on which an electronic device may be constructed, structures such as a plastic or ceramic work surface, for example. The term "substrate" encompasses bodies in a variety of stages of manufacture, including an unprocessed whole wafer, a partially-processed whole wafer, a fully-processed whole wafer, a portion of a diced wafer, or a portion of a diced wafer in a packaged electronic device.

[0008] In this embodiment, the substrate 102 includes an upper doped region 104 and a lower doped region 106. The upper doped region 104 and the lower doped region 106 may be differently doped. For example, the upper doped region 104 may include an n+ material and

the lower doped region 106 may include a p- material. The depth of the upper doped region 104 may be generally uniform over a substantial portion of the substrate 102, such as throughout a substantial portion of an array area of a memory device, for example. The upper doped region 104 and the lower doped region 106 may be doped by implanting or diffusing dopant materials. Alternatively, or additionally, one or both of these regions 104 or 106 may be doped during growth or deposition of all or part of the substrate 102, such as during epitaxial deposition of a semiconductive material or during growth of a semiconductive ingot from which wafers are cut. As explained below, the upper doped region 104 may provide material used to form a source and a drain of a transistor, and the lower doped region 106 may provide material used to form a channel of the transistor.

[0009] Deep isolation trenches 108 and shallow trenches 110 may be formed in the substrate 102. These trenches 108 and 110 may generally extend in the Y direction, as indicated in FIG. 1. One or more shallow trenches 110 may be interposed between pairs of the deep isolation trenches 108. In some embodiments, the shallow trenches 110 may be deeper than the upper doped region 104 to separate subsequently-formed sources and drains. Additionally, the deep isolation trenches 108 may be deeper than the shallow trenches 110 to isolate subsequently-formed transistors.

[0010] The deep isolation trenches 108 and the shallow trenches 110 may define several dimensions of the substrate 102. The shallow trenches 110 have a width 112 less than F, where

F is the resolution of the equipment with which the deep isolation trenches are patterned. Similarly, the deep isolation trenches 108 may have a width 114 less than F, and the deep isolation trenches 108 may be spaced away from the shallow trenches 110 by a width 116 that is less than F. In some embodiments, one or more or all of these widths 112, 114, and 116 is less than or generally equal to 3/4 F, 1/2 F, or 1/4 F. The trenches 108 and 110 repeat with a period of 118, which in some embodiments is less than or generally equal to 4 F, 2 F, or 1 F. In other embodiments, the pattern may be interrupted with other structures or variation in the pattern. The deep isolation trenches 108 and/or shallow trenches 110 may have a generally rectangular or trapezoidal cross-section, and, in some embodiments, their cross-section may be generally uniform through some distance in the Y direction, for example through a distance larger than one, two, five, or more transistor lengths.

[0011] A variety of process flows may be used to form the deep isolation trenches 108 and the shallow trenches 110. In some embodiments, they are formed sequentially, each with a double-pitched mask. In one example of such a process, the deep isolation trenches 108 are formed first by masking off the areas between every other pair of deep isolation trenches 108 and, then, forming a poly-silicon sidewall spacer on the sides of the mask, over the areas corresponding to each of the deep isolation trenches 108. Then the mask may be removed and a hard mask material, such as oxide, may be deposited over the remaining poly-silicon sidewall spacers, and the hard mask material may be etched back or planarized with chemical mechanical planarization (CMP) to expose the poly-silicon. Next, the poly-silicon may be

selectively etched to form openings in the oxide hard mask through which the deep isolation trenches 108 may be etched. The shallow trenches 110 may be formed with a similar flow, except with the initial mask shifted by some distance, e.g., the width 116, and with a shallower etch. In other embodiments, these structures 108 and 110, like many others discussed herein, may be formed with process flows.

[0012] The deep isolation trenches 108 and shallow trenches 110 may be partially or entirely filled with various dielectric materials, such as high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), or spun-on-glass (SOG), for instance, to electrically isolate features. Additionally, the deep isolation trenches 108 or the shallow trenches 110 may include various liner materials, such as silicon nitride for example, to relieve film stresses, improve adhesion, or function as a barrier material. In some embodiments, prior to being filled, the bottom of the deep isolation trenches 108 is implanted with dopants selected to further isolate the transistors.

[0013] Next, in this embodiment, three-different films are formed on the substrate 102, as illustrated by FIG. 2. The first illustrated film is a lower stop region 120. In this embodiment, the lower stop region 120 is a layer of oxide that is either grown or deposited, depending in part on whether the bulk semiconductor material of the substrate 102 readily forms a native oxide, as occurs with materials like silicon. For example, the lower stop region 120 may be grown on silicon by reacting the surface of the silicon portion of the substrate 102

with oxygen in a furnace, or the lower stop region 120 may be deposited with chemical-vapor deposition (CVD) on substrates with a variety of types of semiconductor materials, including both silicon and compound semiconductors. The lower stop region 120 may be between 20 and 200 Å thick, e.g., generally near 80 Å thick.

[0014] The lower stop region 120 may be made of a different material from the next region: an upper stop region 122. In this embodiment, the upper stop region 122 is made of nitride deposited with CVD. The upper stop region 122 may be between 30 and 300 Å thick, e.g., generally near 100 Å thick. As explained below, in some embodiments, the transition between the upper stop region 122 and the lower stop region 120 may reduce over etching by signaling the appropriate time to stop etching or by slowing the etch rate before the upper doped region 104 is penetrated.

[0015] Next in the illustrated embodiment, a sacrificial mask region 124 is formed, as illustrated by FIG. 2. The sacrificial mask region 124 may be made of poly-silicon deposited with a CVD system, and it may have a thickness between 500 and 5000 Å, e.g., generally near 1500 Å thick. The thickness of the sacrificial mask region 124 may be selected based on a desired semiconductor-fin height. As explained below, in this embodiment, the sacrificial mask region 124 forms a hard mask for the etch step that defines the semiconductor fins. A portion of the hard mask is consumed during the fin etch, so the longer the semiconductor fins, and the deeper the fin etch, the thicker the sacrificial mask region 124 may be.

[0016] After forming the films illustrated by FIG. 2, the substrate 102 is patterned, as illustrated by FIGS. 3 and 4. FIG. 3 illustrates a precursor-fin mask 126, and FIG. 4 illustrates precursor fins 128 formed by etching regions exposed by the precursor-fin mask 126. The precursor-fin mask 126 may be made of photoresist, or the mask 126 may be a hard mask formed by depositing and patterning a masking material. The precursor-fin mask 126 may be patterned with a variety of lithography systems, such as a photolithography system, a nano-imprint system, an electron-beam system, or other appropriate patterning device. The illustrated precursor-fin mask 126 includes a series of masked regions 130 and exposed regions 132, both generally extending in the X direction. Both the masked regions 130 and the exposed regions 132 may have a width generally equal to 1 F, and it follows that the precursor-fin mask 126 may have a period 134 near 2 F.

[0017] In certain embodiments, the precursor-fin mask 126 has a relatively large alignment margin compared to some conventional processes. In this embodiment, many of the existing structures on the substrate 102, such as the deep isolation trenches 108 and the shallow trenches 110 are generally uniform in the Y direction. As a result, in this embodiment, the mask 126 can be shifted slightly, or misaligned, along the Y direction without significantly affecting the ultimate shape of the transistors. Similarly, because the mask 126 is generally uniform in the X direction, some misalignment of the trenches 108 and 110 in the X direction may be acceptable in some embodiments.

[0018] After forming the precursor-fin mask 126, the precursor-fins 128 may be etched, as illustrated by FIG. 4. In some embodiments, this etch may be a generally anisotropic dry etch. The precursor fins 128 may have dimensions that are generally complementary to the dimensions of the precursor-fin mask 126. The etch may form voids that generally extend along the Z axis a distance 136 into the substrate 102. The distance 136 may be selected so that bottoms 138 of the voids are substantially deeper than the shallow trenches 110, but not as deep as the deep isolation trenches 108.

[0019] Next, as illustrated by FIGS. 5 and 6, the sacrificial-masking-region portion 124 of the precursor fins 128 may be undercut. The substrate 102 may be placed in a wet-etch bath that is selective to the material from which the sacrificial masking region 124 is made, e.g., a wet etch that preferentially etches poly-silicon but removes the other materials on the substrate 102 at a substantially slower rate. Because wet etches are generally isotropic, and because the top and bottom of the sacrificial masking region 124 is covered by other regions 126 and 122, the wet etch may primarily remove material from the vertical surfaces of the sacrificial masking region 124, in the X and the Y directions, thereby narrowing its width 140. In some embodiments, the width 140 may be generally equal to or less than 1/4 F, 1/2 F, 3/4 F or 1 F. The sacrificial masking region 124 may be undercut by a distance 141 that is generally equal to or greater than 3/8 F, 1/4 F, 1/8 F, or some other distance. In some embodiments, the distance 141 may be generally equal to or greater than 15 nm. As described below, the narrower sacrificial masking region 124 may define narrower semiconductor fins. In some embodiments,

the sacrificial masking region 124 may be undercut during the etch that forms the precursor fins 128.

[0020] Next, the precursor-fin mask 126 is removed, as illustrated by FIG. 7. The precursor-fin mask 126 may be removed with a wet etch that is selective to the precursor-fin mask 126, or the precursor-fin mask 126 may be removed by reacting the precursor-fin mask 126 with oxygen in a furnace or a plasma etch chamber.

[0021] As illustrated by FIG. 8, a liner 142 may be formed on the substrate 102. In this embodiment, the liner 142 is a generally conformal nitride film deposited with chemical-vapor deposition or other type of deposition. In some embodiments, the liner 142 is made of the same material as the upper stop region 122 or other suitable material, for example. The liner 142 may have a thickness 144 that is generally equal to or less than the width 142 of the undercut of the sacrificial masking region 124 (FIG. 6). The illustrated liner 142 includes shoulders 143 that define a compound curve with two generally 90-degree changes in direction. As explained below, in some embodiments, these shoulders 143 protect the portion of the liner 142 below the shoulder 143 when etching the portion of the liner 142 above the shoulder 143. Thus, the shoulder 143 functions in some embodiments as a stop region.

[0022] Next, an inter-gate dielectric 146 is formed, as illustrated by FIG. 9. In this embodiment, the inter-gate dielectric 146 is a spun-on dielectric (SOD) applied with an overburden 148. In other embodiments, it may be a different material applied with a different

process, e.g., CVD or ALD. The spun-on dielectric may be a spun-on glass, such as oxide, and in some embodiments, the spun-on dielectric may be densified by placing the substrate 102 in a furnace to drive volatile compounds from the spun-on dielectric. In some embodiments, the liner 142 may protect other portions of the substrate 102 from film stresses developed during densification.

[0023] After forming the inter-gate dielectric 146, the substrate 102 may be generally planarized with chemical-mechanical planarization (CMP), as illustrated by FIG. 10. The CMP process may remove the overburden 148, a top portion of the liner 142, and stop on or near the sacrificial-masking region 124. The transition between the inter-gate dielectric 146 and the liner 142 may produce a detectable phenomenon, such as a change in optical properties of the substrate (e.g., color), chemical properties (e.g., waste slurry pH), or mechanical properties (e.g., sliding friction) that triggers an end to the CMP process. The transition between the liner 142 and the sacrificial masking region 124 may also produce similar detectable phenomena for end-pointing the process. In some embodiments, the CMP process stops on or near the liner 142 and does not expose the sacrificial masking region 124.

[0024] Next, the portion of the liner 142 above the shoulder 143 is removed, as illustrated by FIGS. 11 and 12. The liner 142 may be removed with a dry etch that is generally selective to the liner 142 so that the liner 142 is etched without removing a substantial portion of either the sacrificial-masking region 124 or the inter-gate dielectric 146. In this embodiment,

the etch stops on or near the shoulder 143, and a substantial portion or all of the liner 142 below the shoulder 143 remains in place. In some embodiments, the etch may penetrate into the upper stop region 122 and stop on the lower stop region 120. Removing the upper portion of the liner 142 opens gaps 150 between alternating members of the sacrificial masking region 124 and the inter-gate electric 146. In this embodiment, the gaps 150 expose the sidewalls of the inter-gate dielectric 146 for the next process step.

[0025] After forming the gaps 150, they may be widened, as illustrated by FIGS. 13 and 14. In this embodiment, the gaps 150 are widened by wet etching the substrate 102. The etchant penetrates the gaps 150 and reacts with the sidewalls of the inter-gate dielectric 146. The wet etch may be generally isotropic and generally selective to the inter-gate dielectric 146 so that relatively little of the sacrificial masking region 124 is removed. In some embodiments, the wet etch undercuts a portion of the upper stopping region 122 under the sacrificial masking region 124. The gaps 150 may be widened to a width 152, and the inter-gate dielectric 146 may be narrowed to a width 156. In some embodiments, both the width 156 and the width 152 may be less than F, e.g., generally equal to or less than 3/4 F, 1/2 F, or 1/4 F. As explained below, the width 152 may generally define the width of the gates for each of the transistors.

[0026] Next in the presently described embodiment, the substrate 102 is anisotropically etched, as illustrated by FIGS. 15 and 16. In this embodiment, the anisotropic etch preferentially removes material in the Z direction and is generally not selective to many or all

of the exposed materials of the substrate 102. For example, the etch may generally etch the inter-gate dielectric 146, the sacrificial masking region 124, the upper doped region 104, and the lower doped region 106 at generally the same rate. This etch may be the type of etch known in the art as an "alligator etch."

[0027] As illustrated by FIGS. 15 and 16, the presently described etch changes a number of features of the substrate 102. A substantial portion or all of the sacrificial masking region 124 may be removed, and furrows 158 may be opened in both the upper doped region 104 and the lower doped region 106. The illustrated furrows 158 may also consume a portion of the liner 142. The furrows 158 may have a depth 160 below the top of the upper doped region 104 that is deeper than the shallow trenches 110, but not as deep as either the deep isolation trenches 108 or the bottom 138 of the space between the precursor fins 128 (FIG. 4). The sidewalls of the furrows 158 may be generally parallel to the Z direction, or they may be sloped or curved. The etch may also reduce the thickness of the inter-gate dielectric 146 and generally define insulating fins 154. The insulating fins 154 may have a base 155 that defines a bottom portion of the furrows 158. As explained below, the insulating fins 154 may separate gates of adjacent rows of transistors.

[0028] At this stage, the substrate 102 may generally define the dimensions of semiconductor fins 162. To illustrate these dimensions, FIG. 17 depicts the upper doped region 104 and the lower doped region 106 of the substrate 102 with the other features removed. As

illustrated, the substrate 102 includes a plurality of semiconductor fins 162. The illustrated fins 162 are arranged in rows 164 generally extending in the X direction, and columns 166 generally extending in the Y direction. In this embodiment, each of the semiconductor fins 162 is isolated both from other semiconductor fins 162 in the same row 164 by a deep trench 168 and from other semiconductor fins 162 in the same column 166 by an intermediate trench 170. The intermediate trenches 170 may include a wider-upper portion 172 and a narrower-lower portion 174. Each of the illustrated semiconductor fins 162 includes a generally U-shaped distal portion with two legs 176 and 178 separated by a shallow trench 180. As explained below, each of these legs 176 and 178 may form either a source or a drain of a transistor.

[0029] The next step in the presently described embodiment is illustrated by FIG. 18. After forming the gaps 158, a gate dielectric 182 may be formed. In some embodiments, the gate dielectric 182 may be deposited with chemical vapor deposition or atomic layer deposition, or in other embodiments, the gate dielectric 182 may be grown by, for example, exposing the substrate 102 to oxygen in a furnace. The illustrated gate dielectric 182 is grown, and as such, it is generally disposed on the exposed portions of both the upper doped region 104 and the lower doped region 106. The gate dielectric 182 may be made of a variety of dielectric materials, such as oxide, oxynitride, or high-dielectric constant materials like hafnium dioxide, zirconium dioxide, and titanium dioxide.

[0030] Next, a gate material 184 may be formed on the substrate 102, as depicted by FIG. 19. The illustrated gate material 184 is a conductive material, such as titanium nitride deposited with a sputter process, but in other embodiments, the gate material 184 may include other conductive films, such as doped polysilicon or various metals. In this embodiment, the gate material 184 is deposited with an overburden 185 to planarize the substrate 102 and substantially or entirely fill the furrows 158.

[0031] In the illustrated embodiment, the gate material 184 is then etched back to form isolated gates 186 and 188 on either side of the rows 164 of semiconductor fins 162, as illustrated by FIG. 20. The gate material 184 may be recessed below the top of the isolating fins 154, but not so deep that the tops of the gates 186 and 188 are below the bottom of the upper doped region 104. That is, the gates 186 and 188 may at least partially overlap the upper doped region 104.

[0032] In some embodiments, the gates 186 in 188 are isolated from one another by the insulating fins 154 even when the sidewalls of the semiconductor fins 162 are sloped. In this embodiment, the gates 186 and 188 are defined in the furrows 158 with an etch back process rather than with a sidewall spacer process. As a result, in some embodiments, sloped fin sidewalls do not necessarily narrow the process window.

[0033] Next, the remainder of the sacrificial masking region 124, the upper stop region 122, and the lower stop region 120 may be removed to expose terminals of the transistors 190,

as illustrated by FIGS. 21 and 22. Each of the illustrated transistors 190 includes a source 192, a drain 194, and a channel illustrated by arrow 196, depicting current flow from the source 192 to the drain 194. The transistors 190 may consume an area generally equal to or less than 4 F^2, including the gates 186 and 188 and isolation associated with each transistor 190.

[0034] To turn on the transistors 190, a voltage may be asserted on the gates 186 and 188, and a voltage between the source 192 and drain 194 may drive current 196 through the channel. The illustrated transistors 190 may be referred to as dual-gate transistors or multi-gate transistors, as they have a gate adjacent each side wall. The gates 186 and 188 may be energized according to a variety of patterns: both gates 186 and 188 may be energized generally simultaneously; one gate 186 or 188 may be energized, but not the other; or the gates 186 and 188 may be energized independent of one another. In some embodiments, the gates 186 and 188 may partially or entirely circumscribe the rows 164, e.g., the gates 186 and 188 may connect at one or both ends of the rows 164.

[0035] A variety of devices may be connected to the transistors 190. For example, the transistors 190 may connect to other transistors 190 to form a processor, an application specific integrated circuit (ASIC), or static random access memory (SRAM), or the transistors 190 may connect to a device primarily configured to store data, such as a capacitor, phase change memory, ferroelectric memory, or a programmable-metallization cell.

[0036] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

1. A device, comprising:

fin field-effect transistors disposed in rows, wherein each of the fin field-effect transistors comprises a semiconductor fin comprising a generally U-shaped distal portion with two legs comprising a source and a drain of each of the fin field-effect transistors, wherein the two legs define a gap therebetween, wherein the two legs and the gap are aligned such that a drive current generated between the source and the drain flows in a direction parallel to alignment of the rows;

an insulator disposed solely in the gap of the semiconductor fin of each of the fin field-effect transistors; and

insulating fins each disposed in a second gap defined between the fin field-effect transistors disposed in the rows.

2. A device, comprising:

fin field-effect transistors disposed in rows, wherein each of the fin field-effect transistors comprises a semiconductor fin comprising a generally U-shaped distal portion with two legs comprising a source and a drain of each of the fin field-effect transistors, wherein the two legs define a gap therebetween;

an insulator disposed solely in the gap of the semiconductor fin of each of the fin field-effect transistors; and

insulating fins each disposed in a second gap defined between the fin field-effect transistors disposed in the rows, wherein the insulating fins at least partially define furrows in which gates of each of the fin-field effect transistors are disposed.

3. The device of claim 2, wherein at least a portion of the insulating fins is disposed under the gates.

4. The device of claim 2, wherein each row comprises at least two of the fin field-effect transistors.

5. The device of claim 2, wherein the fin field-effect transistors comprise dual-gate fin field-effect transistors.

6. A device, comprising:

a plurality of rows of transistors, each transistor comprising:

a semiconductor fin, comprising a generally U-shaped distal portion with two legs comprising a source and a drain, wherein the two legs define a gap therebetween, wherein the two legs and the gap are aligned such that a drive current generated between the source and the drain flows in a direction parallel to alignment of the rows; and

a gate, at least part of which is disposed adjacent the semiconductor fin;

an insulator disposed solely in the gap of the semiconductor fin of each transistor; and

insulating fins each disposed in a second gap defined between each transistor of a pair of rows of transistors among the plurality of rows of transistors.

7. A device, comprising:

a plurality of rows of transistors, each transistor comprising:

a semiconductor fin, comprising a generally U-shaped distal portion with two legs comprising a source and a drain, wherein the two legs define a gap therebetween; and

a gate, at least part of which is disposed adjacent the semiconductor fin;

an insulator disposed solely in the gap of the semiconductor fin of each transistor; and

insulating fins each disposed in a second gap defined between each transistor of a pair of rows of transistors among the plurality of rows of transistors, wherein the insulating fins are disposed at a height greater than a height of the semiconductor fin.

8. The device of claim 7, wherein each insulating fin among the insulating fins comprises a base, and wherein the base is disposed at least partially under at least one of gates.

9. The device of claim 7, wherein the insulating fins extend along at least a substantial portion of a length of the plurality of rows of transistors.

10. The device of claim 7, wherein each insulating fin among the insulating fins comprises a liner disposed between itself and a substrate.

11. The device of claim 7, wherein each row of transistors among the plurality of rows of transistors comprises a pair of gates disposed on opposite sides of the row of transistors.

12. A device, comprising:

a first transistor of a first row of transistors and a second transistor of a second row of transistors each of the first and second transistors comprising:

a semiconductor fin having a width and having a length greater than the width and having a height extending generally perpendicularly from a substrate; and

a pair of gates formed on either side of the semiconductor fin and extending generally parallel to the semiconductor fin;

an insulator disposed solely in a gap defined by a source and a drain of the semiconductor fin of each of the first transistor and the second transistor, wherein the source, the drain, and the gap are aligned such that a drive current generated between the source and the drain flows in a direction parallel to alignment of the first row and the second row; and

an insulating fin disposed in a second gap defined between the first transistor and the second transistor and extending generally parallel to the semiconductor fin of each of the first and second transistors.

13. A device, comprising:

a first transistor of a first row of transistors and a second transistor of a second row of transistors each of the first and second transistors comprising:

a semiconductor fin having a width and having a length greater than the width and having a height extending generally perpendicularly from a substrate; and

a pair of gates formed on either side of the semiconductor fin and extending generally parallel to the semiconductor fin;

an insulator disposed solely in a gap defined by a source and a drain of the semiconductor fin of each of the first transistor and the second transistor; and

an insulating fin disposed in a second gap defined between the first transistor and the second transistor and extending generally parallel to the semiconductor fin of each of the first and second transistors, wherein the insulating fin, the semiconductor fin of the first transistor, and the semiconductor fin of the second transistor define a pair of furrows on either side of the insulating fin, wherein a gate among the pair of gates of the first transistor is disposed in a furrow among the pair of furrows and a gate among the pair of gates of the second transistor is disposed in the other furrow among the pair of furrows.

14. The device of claim 13, wherein the semiconductor fin comprises a pair of legs separated by a trench as the source and the drain.

15. The device of claim 13, comprising a liner disposed at least partially under the insulating fin.

16. The device of claim 13, wherein the first transistor and the second transistor each comprises

an upper doped region and a lower doped region, wherein the upper doped region is doped different from the lower doped region.

17. A device, comprising:

a semiconductor fin having a width and having a length greater than the width and having a height extending generally perpendicularly from a substrate, wherein the semiconductor fin comprises a source and a drain of a transistor;

an insulator disposed solely in a gap defined by the source and the drain of the transistor;

a gate comprising a first side formed on a first side of the semiconductor fin and extending generally parallel to the semiconductor fin; and

an insulating fin directly contacting a second side of the gate opposite the first side of the gate, wherein the insulating fin and the second side of the gate extend generally parallel to the semiconductor fin, and a liner disposed at least partially under the insulating fin.

18. The device of claim 17, wherein the semiconductor fin comprises a pair of legs separated by a trench.

19. The device of claim 17, wherein the pair of legs comprises the source and the drain of the transistor.

20. The device of claim 17, comprising an upper doped region and a lower doped region of the transistor, wherein the upper doped region is doped different from the lower doped region.

21. The device of claim 17, wherein the insulating fin is disposed at a height greater than the height of the semiconductor fin.