INTEGRATED CIRCUIT SYSTEM WITH SUB-GEOMETRY REMOVAL AND METHOD OF MANUFACTURE THEREOF

CROSS-REFERENCE TO RELATED APPLICATION

[0001] This application claims the benefit of U.S. Provisional Patent Application serial number 61/073,362 filed June 16, 2008, and the subject matter thereof is incorporated herein by reference thereto.

TECHNICAL FIELD

[0002] The present invention relates generally to an integrated circuit system, and more particularly to an integrated circuit system for removing sub-geometries and singularities from photomask data and the integrated circuits produced therefrom.

BACKGROUND ART

[0003] Integrated circuits find application in many of today's consumer electronics, such as cell phones, video cameras, portable music players, printers, computers, etc. Integrated circuits may include a combination of active devices, passive devices and their interconnections.

[0004] Integrated circuit fabrication typically requires a multitude of photomasks, wherein each photomask defines a specific design level that serves a particular purpose. The photomask may contain a series of shapes indicating the regions that are to be processed by the particular manufacturing step that uses the photomask. The combination of all of the shapes in the photomask set, when processed in order, forms the circuitry of the integrated circuit product.

[0005] Generally, an integrated circuit layout consists of two categories of data: design layers (designed by a layout designer) and non-design layers (layers generated with Boolean algorithms and typically done by a foundry). These design and non-design layers can be formed by Boolean algorithms ranging from the simple to the complicated, which can require special sizing.

[0006] Unfortunately, complicated Boolean algorithms can produce singularities and sub-geometry features, such as slit and slot features, within the mask level data. The singularities and sub-geometries represent unintentional features that have a size that is below the minimum feature size of the integrated circuit technology. An example of this may be an inadvertent joining of two rectangles, in a 90 nm technology, that has a cross-section of less than 2 nm. The resolution of the 90nm technology might not be able to reliably support the cross-section size which can lead to manufacturing problems, lower wafer yields, and increased costs.

[0007] Some of these sub-geometries can be removed at the layout data level by the application of a size up/size down cleaning rule, wherein some of the polygons are sized up to remove the sub-geometry feature formed between them, and then re-sized down to obtain a resultant dimension that does not impact device performance. If the sub-geometries are not addressed unexpected or parasitic devices could be formed that can damage an operating electronic device.

[0008] However, a simple sizing rule does not work for all structures and some sub-geometries and singularities may remain. As a result, a mask writing tool may not be able to resolve the pattern and/or the sub-geometries left behind and the mask inspection tool will find the mask difficult to inspect. Additionally, a lithographer might see sub-geometries printed on the wafer, which can increase the likelihood or chance of resist lifting that can adversely affect wafer yield and device performance.

[0009] Thus, a need still remains for an integrated circuit system with sub-geometry removal. In view of the continuing trend to increase the electronic content in personal devices, it is increasingly critical that answers be found to these problems. In view of the ever-increasing commercial competitive pressures, along with growing consumer expectations and the diminishing opportunities for meaningful product differentiation in the marketplace, it is critical that answers be found for these problems. Additionally, the need to reduce costs, improve efficiencies and performance, and meet competitive pressures adds an even greater urgency to the critical necessity for finding answers to these problems.

[0010] Solutions to these problems have been long sought but prior developments have not taught or suggested any solutions and, thus, solutions to these problems have long eluded those skilled in the art.

DISCLOSURE OF THE INVENTION

[0011] The present invention provides a method of manufacture of an integrated circuit system including: forming reticle data; detecting a sub-geometry, a singularity, or a combination thereof in the reticle data; applying a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data; and fabricating an integrated circuit from the reticle data.

[0012] The present invention provides an integrated circuit system comprising: reticle data on a photomask; a sub-geometry, a singularity, or a combination thereof detected in the reticle data; a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data; and an integrated circuit fabricated from the reticle data.

[0013] Certain embodiments of the invention have other steps or elements in addition to or in place of those mentioned above. The steps or element will become apparent to those skilled in the art from a reading of the following detailed description when taken with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is an isometric view of the basic elements of a photolithography system used to pattern an integrated circuit system in accordance with an embodiment of the present invention.

[0015] FIG. 2 is a plan view of a unit cell in accordance with an embodiment of the present invention.

[0016] FIG. 3 is a pictorial representation section of a reticle data having a sub-geometry.

[0017] FIG. 4 is a view of a reticle data employing the unit cell to remove the sub-geometry in accordance with an embodiment of the present invention.

[0018] FIG. 5 is a view of a reticle data after merging a unit cell as new data in accordance with an embodiment of the present invention.

[0019] FIG. 6 is a view of a reticle data employing a unit cell in accordance with an embodiment of the present invention.

[0020] FIG. 7 is a flow chart of an exemplary process for removal of the sub-geometries by adding a unit cell to the reticle data, in accordance with an embodiment of the present invention.

[0021] FIG. 8 is a view of a reticle data having a singularity formed between two or more of the rectangular shapes within a reticle system in accordance with an embodiment of the present invention.

[0022] FIG. 9 is a view of a reticle data including a patching cell and/or method between two or more of the rectangular shapes within a reticle system in accordance with an embodiment of the present invention.

[0023] FIG. 10 is a view of a reticle data after merging the patch cell as new data in accordance with an embodiment of the present invention.

[0024] FIG. 11 is a flow chart of an exemplary process for removal of the singularity by adding the patch cell to the reticle system in accordance with an embodiment of the present invention.

[0025] FIG. 12 is a flow chart of a method of manufacture of an integrated circuit system in an embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0026] The following embodiments are described in sufficient detail to enable those skilled in the art to make and use the invention. It is to be understood that other embodiments would be evident based on the present disclosure, and that system, process, or mechanical changes may be made without departing from the scope of the present invention.

[0027] In the following description, numerous specific details are given to provide a thorough understanding of the invention. However, it will be apparent that the invention may be practiced without these specific details. In order to avoid obscuring the present invention, some well-known circuits, system configurations, and process steps are not disclosed in detail.

[0028] The drawings showing embodiments of the system are semi-diagrammatic and not to scale and, particularly, some of the dimensions are for the clarity of presentation and are shown exaggerated in the drawing FIGs. Similarly, although the views in the drawings for ease of description generally show similar orientations, this depiction in the FIGs. is arbitrary for the most part. Generally, the invention can be operated in any orientation.

[0029] Where multiple embodiments are disclosed and described, having some features in common, for clarity and ease of illustration, description, and comprehension thereof, similar and like features one to another will ordinarily be described with similar reference numerals.

[0030] For expository purposes, the term "horizontal" as used herein is defined as a plane parallel to the plane or surface of the semiconductor wafer, regardless of its orientation. The term "vertical" refers to a direction perpendicular to the horizontal as just defined. Terms, such as "above", "below", "bottom", "top", "side" (as in "sidewall"), "higher", "lower", "upper", "over", and "under", are defined with respect to the horizontal plane, as shown in the figures. The term "on" means that there is direct contact among elements.

[0031] The term "processing" as used herein includes deposition of material or photoresist, patterning, exposure, development, etching, cleaning, and/or removal of the material or photoresist as required in forming a described structure.

[0032] Referring now to FIG. 1, therein is shown an isometric view of the basic elements of a photolithography system 100 used to pattern an integrated circuit system 102 in accordance with an embodiment of the present invention. The isometric view of the basic elements of the photolithography system 100 depicts a radiation source 104, such as an Argon Fluoride (ArF) excimer laser light source, providing radiation beams 106 having a wavelength of 193 nm or less.

[0033] A condenser 108, such as a focusing lens system, may receive the radiation beams 106 and converge the radiation beams 106 on a reticle system 110. The reticle system 110 may be a group of photomasks, such as fused silica blanks of amorphous quartz, having a thin patterned opaque metal layer such as chromium deposited on one surface of the blank. The pattern formed in the opaque metal layer may be the complex geometric shapes associated with patterning a single manufacturing process step for an integrated circuit (not shown).

[0034] A set of projection optics 112, may collect the radiation beams 106 that are passed through the reticle system 110 which now depicts the pattern provided by the reticle system 110. This pattern may represent a single pattern associated with the manufacturing step being performed on the integrated circuit system 102. Many such iterative steps go into the manufacturing of the integrated circuit system 102.

[0035] A stepper 114, such as an x-y orientation stepping platform, may be used to relocate the integrated circuit system 102 for exposure of single image of a component layer of the integrated circuit (not shown). A photoresist material 116, such as a super fine pattern forming material, is applied on a substrate 118. The substrate 118 may be a semiconductor wafer having an integrated circuit 120 fabricated thereon.

[0036] The integrated circuit 120 may reflect the contents of the reticule system 110 and be free of layer singularities and sub-geometries. The integrated circuit 120 may be singulated from the substrate 118 by being diced.

[0037] Referring now to FIG. 2, therein is shown a plan view of a unit cell 200 in accordance with an embodiment of the present invention. The plan view of the unit cell 200 depicts a generalized form of the unit cell 200, such as a complex geometric shape.

[0038] In some embodiments, the size and/or dimensions of the unit cell 200 can be illustrated by one or more measurements or sections. By way of example, in one embodiment, a tab measurement 202 can be of a fixed dimension, such as 50 nanometers, while a horizontal measurement 204 and a vertical measurement 206 can depend on the distance between adjacent geometries (not shown) that form a sub-geometry (not shown).

[0039] In other embodiments, the tab measurement 202 may need to satisfy a minimum dimension rule to ensure that the unit cell 200 can be resolved when patterning the substrate 118, of FIG. 1, with the reticle system 110, of FIG. 1. However, it is to be understood that the size and/or dimensions of the tab measurement 202, the horizontal measurement 204, and the vertical measurement 206 can be modified to meet the design requirements of the technology node of the integrated circuit system 102, of FIG. 1. The technology node may be designated by the minimum dimension of a feature, including technology nodes such as 135 nm, 90 nm, 65 nm, or 50 nm.

[0040] In some embodiments, the unit cell 200 can be described as "Z" shaped because of two projections that extend from opposite ends and corners of a central geometry. It is understood that the unit cell 200 may be inverted or rotated in order to remove the sub-geometry between the adjacent shapes.

[0041] Referring now to FIG. 3, therein is shown a pictorial representation section of a reticle data 300 having a sub-geometry 302. The pictorial representation section of the reticle data 300 depicts the sub-geometry 302 formed between a first shape 304 and a second shape 306 as generated in the reticle system 110.

[0042] The sub-geometry 302 would cause a mask rules check (MRC) violation because it violates a minimum size requirement for the example technology node. The relationship of the second shape 306 to a third shape 308 has sufficient spacing to not create an additional MRC violation.

[0043] The sub-geometry 302 has a width 310 and a height 312. One or both of these dimensions may create a shape in the reticle data 300 that could cause a manufacturing

problem. In order to correct the MRC violation additional geometries may be added to the reticle data 300.

[0044] This example is intended to demonstrate how the MRC violation may occur in the generation of the reticle data 300. It is understood that other configurations could cause MRC violations and the present example is intended to show how any of the currently irresolvable violations may be resolved by the current invention.

[0045] Referring now to FIG. 4, therein is shown a view of a reticle data 400 employing the unit cell 200 to remove the sub-geometry 302 in accordance with an embodiment of the present invention. In some embodiments, the vertices of the first shape 304 and the second shape 306 can be used to indicate where the sub-geometry feature is located within a coordinate system, such as a Cartesian coordinate system, of a layout.

[0046] In other embodiments, the unit cell 200 can be generated from the data of the first shape 304 and the second shape 306. Data of the first shape 304 and the second shape 306 may include, but is not limited to, one or more variables, such as the width 310, of FIG. 3, and the height 312, of FIG. 3, which can be determined by calculating the dimensions of the first shape 304 and the second shape 306 and their relative position.

[0047] The reticle system 110 may employ one or more of the unit cell 200 between one or more of the first shape 304 and the second shape 306. In the above example the spacing of the third shape 308 is in compliance with the MRC, but if an MRC violation had been detected between the second shape 306 and the third shape 308, the unit cell 200 would be applied to resolve the MRC violation.

[0048] It is understood that while the general characteristics of the unit cell 200 remains constant, the actual size may differ for each of the unit cells 200 applied. The size of the unit cell 200 may vary in the width 310, of FIG. 3, and the height 312, of FIG. 3, as described above.

[0049] The unit cell 200 can help to remove the sub-geometries 302 that may be unresolved within the reticle data 400. It is also to be understood that the reticle data 400 may include any structure formed on or over any layer of the integrated circuit system 102, of FIG. 1.

[0050] The reticle data 400 can represent the original data formed by the layout data level of electronic design automaton software or it may be generated by Boolean combinations of the layout data. The Boolean combinations of the layout data may be generated by the manufacturing software for photomask generation.

[0051] Referring now to FIG. 5, therein is shown a view of a reticle data 500 after merging a unit cell as new data in accordance with an embodiment of the present invention. The view of the reticle data 500 depicts the reticle system 110 after merging the unit cell 200, of FIG. 4, as a new shape 502 in accordance with an embodiment of the present invention.

[0052] The unit cell 200 when plotted as part of the new shape 502 and formed on the reticle system 110 removes the sub-geometry 302, of FIG. 3, at the layout data level, the reticle system 110 level, and/or the integrated circuit system 102, of FIG. 1.

[0053] It has been discovered that the incorporation of the unit cell 200 during the generation of the reticle data 500 may prevent MRC violations and improve the manufacturing yield of the integrated circuit system 102, of FIG. 1.

[0054] Referring now to FIG. 6, therein is shown a view of a reticle data 600 employing a unit cell in accordance with an embodiment of the present invention. The view of the reticle data 600 depicts a first rectangle shape 602 adjacent to a second rectangle shape 604.

[0055] The unit cell 200 is placed between the first rectangle shape 602 and the second rectangle shape 604.

[0056] Each of the first rectangle shape 602, the second rectangle shape 604, and the unit cell 200 can be formed over and/or within a medium 606, such as a quartz or glass substrate having clear and opaque regions representing the reticle data 600. It is to be understood that the medium 606 can represent a layout data level, the reticle system 110, of FIG. 1, and/or the integrated circuit system 102, of FIG. 1.

[0057] By way of example, and for ease of discussion, the unit cell 200 can be divided into two sections, a first region 608 and a second region 610, based upon their functionality. In some embodiments, the first region 608 can be used to fill the gap, distance, or space between one or more of the first rectangle shape 602 and the second rectangle shape 604, thereby helping to remove the sub-geometries 302, of FIG. 3.

[0058] The second region 610 can be employed to improve the resolution of the connection region, when the overlapping region of the first rectangle shape 602 and the second rectangle shape 604 is too short. It is understood that the system and method described herein can be used in a multitude of applications including removing the sub-geometry 302 that may exist adjacent the first rectangle shape 602 or between two or more of the first rectangle shape 602 and the second rectangle shape 604, regardless of the function of the affected layer.

[0059] Referring now to FIG. 7, therein is shown a flow chart of an exemplary process 700 for removal of the sub-geometries by adding a unit cell to the reticle data, in accordance with

an embodiment of the present invention. The flow chart of the exemplary process 700 depicts a combine data 702.

[0060] The combine data 702 may produce manufacturing layer layout information, used to fabricate the integrated circuit system 102, of FIG. 1, by performing a Boolean operation on one or more layout design layers. Since the Boolean operation may produce the sub-geometry 302, of FIG. 3, a check dimensions 704 must verify all spacing.

[0061] The check dimensions 704 may perform a MRC on all of the shapes of the combine data 702 in order to identify the sub-geometry 302. The coordinates of all of the shapes in the combine data 702 may be identified and separation distances calculated in order to identify the sub-geometry 302.

[0062] If one or more of the sub-geometry 302 is identified by the check dimensions 704, an insert unit cell 706 will place and adjust the unit cell 200, of FIG. 2. The adjustment of the unit cell 200 may include matching the width 310, of FIG. 3, and the height 312, of FIG. 3, to the sub-geometry 302 identified by the check dimensions 704.

[0063] A merge data 708 may perform an additional Boolean operation, such as an "OR" operation to merge the unit cell 200 into the new shape 502, of FIG. 5, created by the merge data 708. The resulting geometry of the new shape 502 may have the sub-geometry 302 removed.

[0064] Referring now to FIG. 8, therein is shown a view of a reticle data 800 having a singularity 802 formed between two or more rectangular shapes 804 within a reticle system 110 in accordance with an embodiment of the present invention. The view of the reticle data 800 depicts two of the rectangular shapes 804 meeting at a corner in a diagonal joining.

[0065] The singularity 802 may be detected when two shapes in the reticle data 800 meet in a single point as depicted in FIG. 8. The single point of contact may include a slight overlap of the rectangular shapes 804 wherein the cross-section of the slight overlap does not meet the minimum dimension of the MRC.

[0066] In an embodiment, a script, such as a series of instructions generated from a scripting language, can be used to determine the singularity 802 between two or more of the rectangular shapes 804. In some embodiments, the vertices of the rectangular shapes 804 can be used to indicate where the singularity 802 is located within a coordinate system, such as a Cartesian coordinate system, of a layout.

[0067] It is understood that the rectangular shapes 804 may include any structure formed on or over any layer of the integrated circuit system 102, of FIG. 1, and that the rectangular

shapes 804 is an example only. The rectangular shapes 804 can represent the original data formed at the layout data level by electronic design automation software or combined in a Boolean operation by a manufacturing software used for fabricating the integrated circuit system 102, of FIG. 1.

[0068] Referring now to FIG. 9, therein is shown a view of a reticle data 900 including a patch cell 902 and/or method between two or more of the rectangular shapes 804 within a reticle system 110 in accordance with an embodiment of the present invention. The view of the reticle data 900 depicts a pair of the rectangular shapes 804 positioned to form the singularity 802.

[0069] In an embodiment, after the script identifies the singularity 802, two equidistant and parallel offset lines, such as the lines 902, can be created between each of the rectangular shapes 804, thereby forming what can be termed a "bridge region" between the rectangular shapes 804. However, it is to be understood that in other embodiments, each of the line 902 need not be equidistant or parallel, each of the lines 902 need only connect or "bridge" a portion of each of the rectangular shapes 804 to an other of the rectangular shape 804.

[0070] By way of example, in one embodiment, a measurement 904, such as a fixed measurement, may be 50 nanometers. In other embodiments, the measurement 904 may need to satisfy a minimum dimension rule to ensure that the bridged region does not create an additional MRC violation.

[0071] Referring now to FIG. 10, therein is shown a view of a reticle data 1000 after merging the patch cell 902 as new data in accordance with an embodiment of the present invention. The view of the reticle data 1000 depicts a new shape 1002 resulting from a Boolean operation, such as an "OR" of the rectangular shapes 804 and the patch cell 902, on the reticle system 110.

[0072] The new shape 1002 can be resolved when patterning the substrate 118, of FIG. 1, with the reticle system 110, of FIG. 1. However, it is to be understood that the size and/or dimension of the measurement 904, of FIG. 9, can be modified to meet the design requirements, such as the technology node, the design rule, and/or the dimensions of a singularity, of the integrated circuit system 102, of FIG. 1.

[0073] In some embodiments, points on each of the line 902 can be used to indicate where the patch cell 902 should subsequently be located within a coordinate system, such as a Cartesian coordinate system, of a layout.

[0074] Referring now to FIG. 11, therein is shown a flow chart of an exemplary process 1100 for removal of the singularity 802, of FIG. 8, by adding the patch cell 902, of FIG. 9, to the reticle system 110, of FIG. 1, in accordance with an embodiment of the present invention. The flow chart of the exemplary process 1100 depicts an identify singularity 1102.

[0075] The identify singularity 1102 may include detecting the coordinates of the vertices of the shapes in the reticle data 800. When the vertices of two shapes coincide the singularity 802 is detected. The detection of the singularity 802 leads to an insert a patch cell 1104.

[0076] The insert a patch cell 1104 may apply two of the lines 902, that are parallel, between the two shapes having the singularity 802, to form the patch cell 902 on the singularity 802. When the patch cell is properly applied a merge data 1106 may be invoked.

[0077] The merge data 1106 may perform a Boolean operation on all of the shapes in the reticle data 900 to form a series of the new shape 1002, of FIG. 10, for all of the shapes in the reticle data 1000. The new shapes 1002 will be free of the singularity 802 throughout the reticle data 1000.

[0078] It has been unexpectedly [found, determined, recognized, ascertained, identified, observed, detected, uncovered] that by applying the unit cell 200, of FIG. 2, and the patch cell 902, of FIG. 9, in conjunction with the grow and shrink strategy, all of the sub-geometries 302 and the singularities 802 may be removed from the reticle system 110.

[0079] Thus, it has been discovered that the integrated circuit system and device of the present invention furnishes important and heretofore unknown and unavailable solutions, capabilities, and functional aspects for producing integrated circuit systems having a better manufacturing yield and reduced cost.

[0080] Referring now to FIG. 12, therein is shown a flow chart of a method 1200 of manufacture of an integrated circuit system in an embodiment of the present invention. The method 1200 includes: forming reticle data in a block 1202; detecting a sub-geometry, a singularity, or a combination thereof in the reticle data in a block 1204; applying a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data in a block 1206; and fabricating an integrated circuit from the reticle data in a block 1208.

[0081] The resulting method, process, apparatus, device, product, and/or system is straightforward, cost-effective, uncomplicated, highly versatile and effective, can be surprisingly and unobviously implemented by adapting known technologies, and are thus

readily suited for efficiently and economically manufacturing integrated circuit systems fully compatible with conventional manufacturing methods or processes and technologies.

[0082] Another important aspect of the present invention is that it valuably supports and services the historical trend of reducing costs, simplifying systems, and increasing performance.

[0083] These and other valuable aspects of the present invention consequently further the state of the technology to at least the next level.

[0084] While the invention has been described in conjunction with a specific best mode, it is to be understood that many alternatives, modifications, and variations will be apparent to those skilled in the art in light of the aforegoing description. Accordingly, it is intended to embrace all such alternatives, modifications, and variations that fall within the scope of the included claims. All matters hithertofore set forth herein or shown in the accompanying drawings are to be interpreted in an illustrative and non-limiting sense.

What is claimed is:

1. A method of manufacture of an integrated circuit comprising:

forming reticle pattern having at least a first shape and a second shape for fabricating an integrated circuit from the reticle pattern;

detecting a sub-geometry, a singularity, or a combination thereof in the reticle pattern between the first shape and the second shape;

applying a unit cell, a patch cell, or a combination thereof to the reticle pattern for removing the sub-geometry, the singularity, or the combination thereof from the reticle pattern including forming a new shape by performing a Boolean operation on the first shape, the second shape, the unit cell, the patch cell, or the combination thereof; and

fabricating the integrated circuit from the reticle pattern having at least the first shape, the second shape, and including the new shapes on the integrated circuit.

2. The method as claimed in claim 1 further comprising setting a width and a height of the unit cell based on the sub-geometry size.

3. The method as claimed in claim 1 wherein applying the patch cell includes:

bridging lines between rectangular shapes; and

intersecting, a measurement from the singularity, the lines and the rectangular shapes.

4. The method as claimed in claim 1 wherein fabricating the integrated circuit includes:

providing a substrate;

coating a photoresist material on the substrate;

focusing a set of projection optics on the photoresist material; and

providing a reticle system for projecting the reticle pattern.

5. The method as claimed in claim 1 wherein detecting the singularity includes locating two rectangular shapes meeting at a corner.

6. A method of manufacture of an integrated circuit system comprising:

forming reticle data having a first shape and a second shape;

detecting a sub-geometry, a singularity, or a combination thereof in the reticle data including locating vertices of the first shape and the second shape;

applying a unit cell, a patch cell, or a combination thereof for removing the sub-geometry, the singularity, or the combination thereof from the reticle data including forming a new shape by performing a Boolean operation on the first shape, the second shape, the unit cell, the patch cell, or the combination thereof; and

fabricating an integrated circuit from the reticle data including forming the new shapes on the integrated circuit.

7. The method as claimed in claim 6 further comprising setting a width and a height of the unit cell based on the sub-geometry size including providing a tab measurement having a fixed value.

8. The method as claimed in claim 6 wherein applying the patch cell includes:

bridging lines between rectangular shapes including forming the lines parallel to each other; and

intersecting, a measurement from the singularity, the lines and the rectangular shapes including forming a bridge region between the rectangular shapes.

9. The method as claimed in claim 6 wherein fabricating the integrated circuit includes:

providing a substrate including providing a stepper for mounting the substrate;

coating a photoresist material on the substrate including applying a super fine pattern forming material;

focusing a set of projection optics on the photoresist material including converging radiation beams; and

providing a reticle system for projecting the reticle data for forming the integrated circuit layer by layer.

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10. The method as claimed in claim 6 wherein detecting the singularity includes locating two rectangular shapes meeting at a corner including failing a mask rules check.