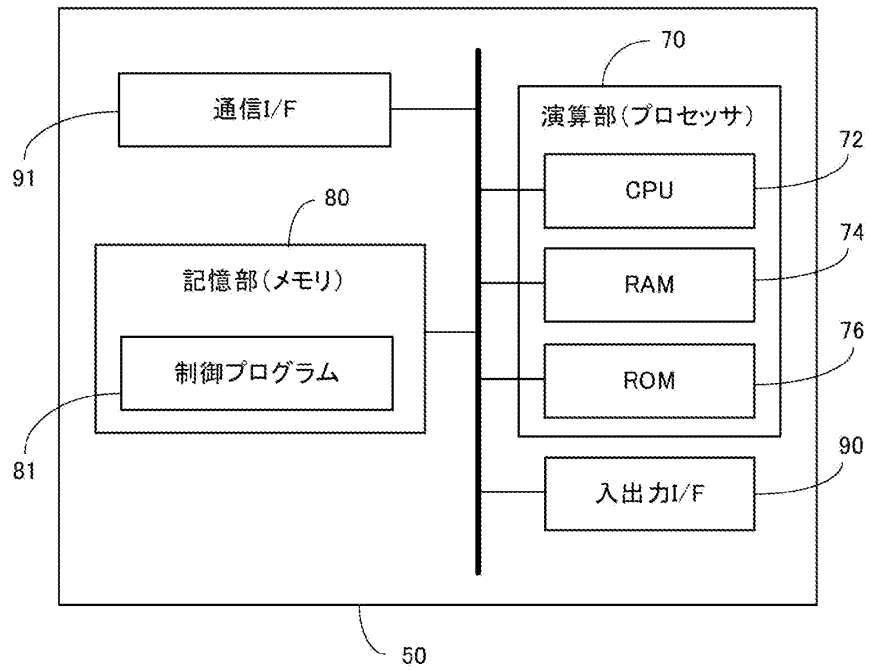


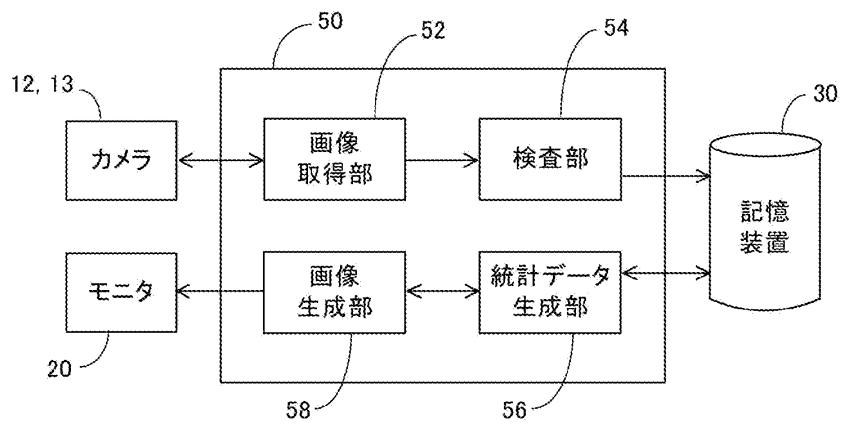
A block diagram showing the system architecture. It consists of two main rectangular blocks. The block on the left is labeled "切断装置" (Cut-off device) and is associated with the reference numeral "1" below it. The block on the right is labeled "記憶装置" (Memory device) and is associated with the reference numeral "30" below it. A double-headed horizontal arrow connects the right side of the "切断装置" block to the left side of the "記憶装置" block, indicating bidirectional communication or data flow between them. The entire diagram is enclosed in a larger frame, with the reference numeral "100" and an arrow pointing to the frame from the bottom left.

Figure 1 is a schematic diagram of a semiconductor manufacturing apparatus 1. The apparatus is divided into two main sections, A1 and B1. Section A1 contains a series of processing units: a material supply unit 3, a pre-processor 4, a processor 5 (with sub-units 5a, 5b, 5c, 5d, 5e), and a post-processor 7. Section B1 contains a processor 11, a transfer unit 12, a transfer unit 13, a transfer unit 14, and a transfer unit 15. A computer 50 is connected to the apparatus. A coordinate system (X, Y, Z) is shown at the bottom left, with a rotation angle θ .

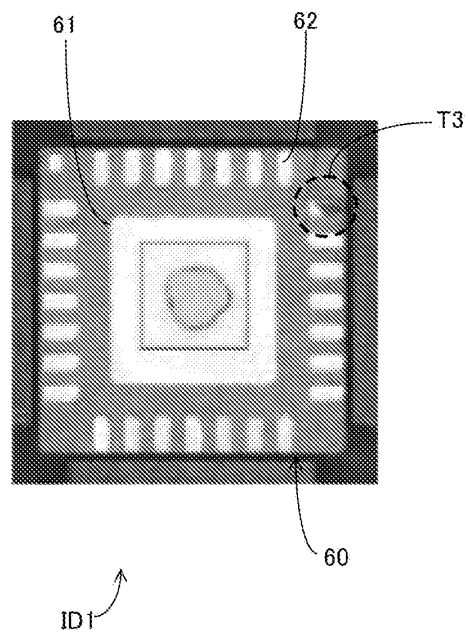
[図4]



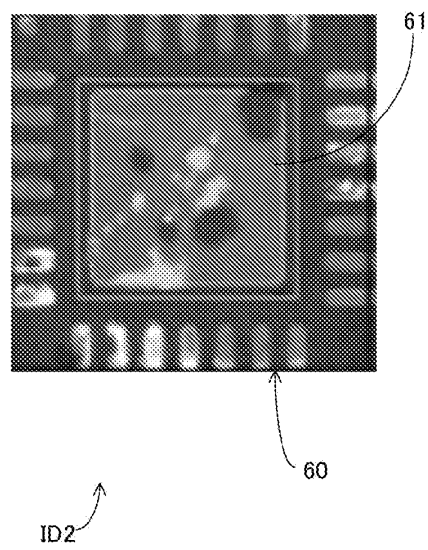
[図5]



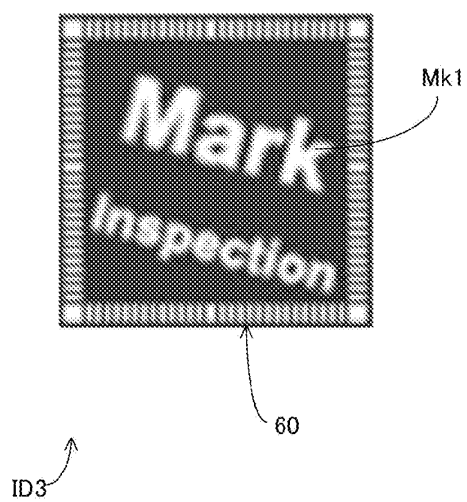
[図6]



[図7]



[図8]

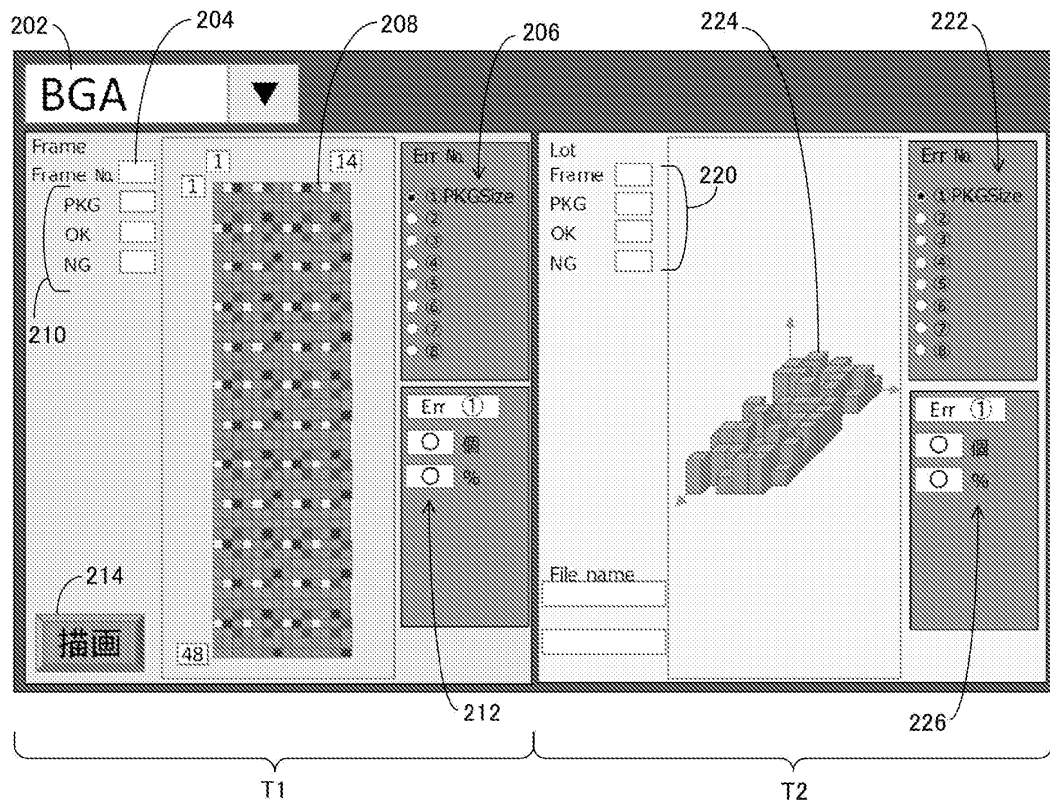


[図9]

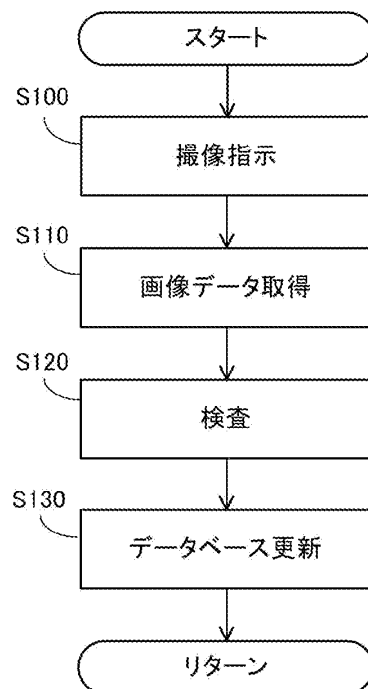
ロット	No.	フレームNo.	位置		検査項目			
			X	Y	0	1	2	...
0000	1	1	1	1	0	0	0	...
0000	2	1	2	1	1	0	5.005	...
0000	3	1	3	1	1	0	4.998	...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	...
0000	870	1	15	58	1	0	5.011	...
0000	871	2	1	1	1	0	4.988	...
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	...

DB1

[図10]



[図11]



[図12]

