

Abstract

A computer system for protecting memory comprising a processor having address outputs and executing a stored program, a memory having a control input, an address-decoder for providing a control signal to the control input of the memory in response to associated address outputs from the processor, and a window circuit. The window circuit comprises a range detector responsive to the address outputs for generating a range-detection signal indicative of an address from the processor being within a protected range, the protected range non-identical to the entirety of the space of addresses within the memory. Access to memory locations within the protected range is permitted only if a request signal is received from the processor. If the request signal is asserted for an unexpectedly long time an error condition is annunciated, for example the processor is reset.

This Sheet Has Been Replaced
