

METHOD AND DEVICE FOR ACQUIRING AND PROCESSING ERROR

ADDRESS INFORMATION

CROSS-REFERENCE TO RELATED APPLICATION

[0001] The present application claims priority to Chinese patent application No.
5 202411458874.1, filed on October 18, 2024, and titled “METHOD AND DEVICE FOR
ACQUIRING AND PROCESSING ERROR ADDRESS INFORMATION”. The content of
the above identified application is hereby incorporated herein in its entirety by reference.

TECHNICAL FIELD

[0002] The present invention relates to the field of chip testing, and in particular, to a
10 method and a device for acquiring and processing error address information.

BACKGROUND

[0003] With the development of electronic technology, electronic devices have come
from one generation to the next at an ever-increasingly faster speed. This has led to growing
demand for memory chips and higher requirements for storage space of the memory chips.
15 As design complexity of the chip increases, requirement for test devices for the memory
chips becomes higher. Currently, testing on a memory chip includes testing on storage
addresses of inner space of the memory chip, as well as conventional input/output tests
common to digital chips. The testing on the storage addresses detects whether a damaged
error address bit exists in the storage space, which is essential for subsequent repair of
20 damaged storage addresses and analysis of failure causes of chip storage addresses.

SUMMARY

[0004] According to various embodiments of the present invention, a method and a

device for acquiring and processing error address information are provided.

[0005] In a first aspect, a method for acquiring and processing error address information is provided. The method includes: reading target test data of a target test object in response to detection of a data reading operation in a user interaction interface, the target
5 test data including error address test data corresponding to a specified address range in error address test data of the target test object; displaying a first-type view in a view window of the user interaction interface based on the target test data, the first-type view being configured to indicate test result information of different addresses in the specified address range; and displaying a second-type view in the view window of the user interaction
10 interface based on the target test data, in response to detection of a view switching operation in the user interaction interface. The second-type view is configured to indicate location distribution information of error addresses in the specified address range on the target test object.

[0006] In a second aspect, an electronic device is provided. The electronic device
15 includes: a memory, configured to store a computer program; a processor, configured to execute the computer program stored in the memory. The execution of the computer program causes the processor to implement the above method for acquiring and processing the error address information.

[0007] In a third aspect, a computer-readable storage medium is provided, having a
20 computer program stored thereon. When the computer program is executed by a processor, the method for acquiring and processing error address information as described above is implemented.

[0008] In a fourth aspect, a computer program product is provided, including a computer program. When the computer program is executed by a processor, the method for acquiring and processing error address information as described above is implemented.

[0009] Details of one or more embodiments of the present invention are presented in the attached drawings and descriptions below. Other features, purposes and advantages of the present invention will become apparent from the description, drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] To clearly illustrate technical solutions in various embodiments of the present invention, the drawings which need to be used for describing various embodiments are described briefly below. Obviously, the drawings in the following description are merely some embodiments of the present invention. For those skilled in the art, other drawings may be obtained in accordance with the accompanying drawings without creative efforts.

[0011] FIG. 1 is a schematic structural diagram of a test device according to an exemplary embodiment of the present invention.

15 [0012] FIG. 2 is a flowchart illustrating a method for acquiring and processing error address information according to an exemplary embodiment of the present invention.

[0013] FIG. 3 is a schematic interface diagram of a first view window according to an exemplary embodiment of the present invention.

[0014] FIG. 4 is a schematic interface diagram of a second view window according to an exemplary embodiment of the present invention.

[0015] FIG. 5 is a schematic interface diagram of a second view window according to another exemplary embodiment of the present invention.

[0016] FIG. 6 is a flowchart illustrating a process of displaying a first-type view according to an exemplary embodiment of the present invention.

[0017] FIG. 7 is a flowchart illustrating a layer superposition process for logical matrix bitmaps according to an exemplary embodiment of the present invention.

5 [0018] FIG. 8 is a schematic interface diagram of a physical matrix view according to an exemplary embodiment of the present invention.

[0019] FIG. 9 is a flowchart illustrating a layer superposition process for physical matrix bitmaps according to an exemplary embodiment of the present invention.

[0020] FIG. 10 is a schematic structural diagram of an apparatus for acquiring and
10 processing error address information according to an exemplary embodiment of the present invention.

[0021] FIG. 11 is a schematic structural diagram of an electronic device according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

15 [0022] In order to make the above objects, features, and advantages of the present invention more obvious and understandable, specific embodiments of the present invention will be described in detail below with reference to the accompanying drawings. In the following description, many specific details are set forth in order to fully understand the present invention. However, the present invention can be implemented in many other ways
20 different from those described herein, and those skilled in the art can make similar improvements without violating the connotation of the present invention. Therefore, the present invention is not limited by the specific embodiments disclosed below.

[0023] Various exemplary embodiments of the present invention will now be described in detail with reference to the accompanying drawings. It should be noted that the relative arrangements of components and steps, numerical expressions, and numerical values set forth in these embodiments do not limit the scope of the present invention unless
5 specifically stated otherwise.

[0024] It may be understood for those skilled in the art that terms such as “first”, and “second” in the embodiments of the present invention are used merely to distinguish between different steps, devices, modules, or the like, and do not denote any specific technical meaning, nor indicate any necessary logical sequence among the terms.

10 [0025] It should further be understood that, in the embodiments of the present invention, “a plurality of” may mean two or more, and “at least one” may mean one, two, or more.

[0026] It should further be understood that any component, data, or structure mentioned in the embodiments of the present invention, in the absence of an explicit
15 limitation or a contrary indication in the context, may be generally understood as one or more components, data, or structures.

[0027] In addition, the term “and/or” in the present invention is merely used to describe an association relationship describing associated objects, and indicates that three relationships may exist. For example, A and/or B, may indicate the following three cases:
20 separate presence of A, coexistence of A and B, and separate presence of B. Furthermore, the character “/” in the present invention generally indicates that the associated objects preceding and succeeding the character “/” are in a relationship of “or”.

[0028] In the present invention, unless otherwise specified or implied, the phrase “at least one” proceeding a list of items refers to any combination of the listed items, including individual members. Both the expression “at least one of a, b, or c” and “at least one of a, b, and c” are intended to encompass: a, b, c, a combination of a and b, a combination of a and c, a combination of b and c, and a combination of a, b and c.

[0029] It should further be understood that the description of the various embodiments of the present invention focuses on differences between the embodiments. For similarities or analogous aspects, reference may be made to each other, which is not repeated herein for the sake of brevity.

10 [0030] Meanwhile, it should be understood that, for the convenience of description, the sizes of various components shown in the accompanying drawings are not necessarily drawn to scale.

[0031] The following description of at least one exemplary embodiment is merely illustrative in nature and is in no way intended to limit the present invention and applications or uses thereof.

[0032] Techniques, methods, and devices known to those skilled in the related art may not be discussed in detail, but be intended to be part of the description where appropriate.

[0033] It should be noted that similar reference numerals and letters denote similar items in the following figures. Therefore, once an item is defined in one drawing, it may not be discussed further in subsequent drawings.

[0034] Embodiments of the present invention may be applied to electronic devices

such as a terminal device, a computer system, and a server. These electronic devices may operate in conjunction with numerous other general-purpose or special-purpose computing system environments or configurations. Examples of well-known terminal devices, computing systems, environments, and/or configurations suitable for use with the electronic
5 devices such as terminal devices, computer systems, servers, and the like include, but are not limited to, personal computer systems, server computer systems, thin clients, thick clients, handheld or laptop devices, microprocessor-based systems, set-top boxes, programmable consumer electronics, network personal computers, minicomputer systems, mainframe computer systems, and distributed cloud computing technology environments
10 incorporating any of the foregoing systems.

[0035] Electronic devices such as terminal devices, computer systems, and servers may be described in the general context of computer system-executable instructions (e.g., program modules) being executed by a computer system. Generally, the program modules may include routines, programs, target programs, components, logic, data structures, and the
15 like, which perform particular tasks or implement particular abstract data types. Computer systems/servers may be implemented in distributed cloud computing environments where tasks are performed by remote processing devices linked through a communication network. In a distributed cloud computing environment, program modules may be located in local or remote computing system storage media including storage devices.

20 [0036] In an embodiment of the present invention, a method for acquiring and processing error address information is provided, to display error address information, indicated by error address test data obtained from an error address test for a storage space of

a target test object with testing equipment, in different types of views on a user interaction interface. This enables users to quickly check and analyze the error address information in the storage space of the target test object through the different types of views.

[0037] The method for acquiring and processing the error address information according to the embodiment of the present invention may be applied to a host computer of a test device, and specifically may be implemented in an apparatus for acquiring and processing the error address information in the host computer. The test device may be configured to perform a semiconductor test on a device under test (DUT), and the DUT may include a wafer, a chip, or the like. In the present invention, the device under test is also referred to as a target test object. Referring to FIG. 1, the test device may include a host computer 10 and a target lower-level computer 20.

[0038] An apparatus 101 for acquiring and processing the error address information may be operated in the host computer 10. The apparatus 101 for acquiring and processing the error address information may be configured to read the error address test data of the target test object from the target lower-level computer 20, and display the error address information corresponding to the acquired error address test data in different types of views on the user interaction interface. The target lower-level computer 20 may be configured to execute test procedures for performing error address testing on the target test object, and store the error address test data acquired by the testing. When the host computer 10 transmits a data read request to the target lower-level computer 20, the target lower-level computer 20 may provide the corresponding error address test data to the host computer 10 according to the data read request.

[0039] FIG. 2 is a flowchart illustrating a method for acquiring and processing error address information according to an exemplary embodiment of the present invention. The method may be performed by the host computer 10 of the test device as described above, and specifically may be performed by the apparatus 101 for acquiring and processing the error address information of the host computer 10. Referring to FIG. 2, the method of this embodiment includes step 210 to step 230.

[0040] Step 210 includes reading target test data of a target test object in response to detection of a data reading operation in a user interaction interface. The target test data includes error address test data corresponding to a specified address range, the error address test data corresponding to the specified address range belongs to error address test data of the target test object.

[0041] The user interaction interface may be an interface that can be interacted with a user in the apparatus for acquiring and processing the error address information, and configured to display the error address information corresponding to the read error address test data.

[0042] In a possible implementation, a trigger control for initiating the data reading request may be provided in the user interaction interface. In response to a trigger operation on the trigger control, it may be determined by the user interaction interface that the data reading operation is detected. Upon detection of the data reading operation by the user interaction interface, the host computer may read the target test data of the target test object.

[0043] In a possible implementation, parameter configuration may be performed by the user in the user interaction interface. Parameters used to read the error address test data

corresponding to a specified address range may be configured. After the data reading operation is detected, the data read request may be generated according to the configured parameters. The data read request may include the configured specified address range. The host computer may transmit the data read request to the target lower-level computer, and the
5 target lower-level computer may provide the error address test data corresponding to the specified address range to the host computer.

[0044] Alternatively, the target lower-level computer may perform the error address testing on a plurality of target test objects, and store error address test data corresponding to the plurality of target test objects. In an example, the target lower-level computer may store
10 error address test data of specified address range corresponding to the plurality of target test objects, and read target test data of the plurality of target test objects in response to the detection of the data reading operation in the user interaction interface.

[0045] Step 220 includes displaying a first-type view in a view window of the user interaction interface based on the target test data. The first-type view is configured to
15 indicate test result information of different addresses in the specified address range.

[0046] In a possible implementation, the first-type view may be a view generated based on the error address test data corresponding to logical addresses of the target test object. The indicated error address information may be error address information corresponding to the logical addresses of the target test object, and the error address test
20 data corresponding to the logical addresses of the target test object may be stored in the target lower-level computer.

[0047] Alternatively, the first-type view may include a view configured to indicate

test results corresponding to all logical addresses included in the specified address range, or may include a view configured to indicate test results corresponding to partial logical addresses in the specified address range.

[0048] In a possible implementation, for the plurality of target test objects, the
5 first-type view may include a view configured to display the test results corresponding to the specified address range of the plurality of target test objects.

[0049] Step 230 includes displaying a second-type view in the view window of the user interaction interface based on the target test data, in response to detection of a view switching operation in the user interaction interface. The second-type view is configured to
10 indicate location distribution information of error addresses in the specified address range on the target test object.

[0050] The user interaction interface may further be provided with a view switching control for switching views. In response to detection of a trigger operation on the view switching control, it may be determined by the user interaction interface that a view
15 switching operation is detected, and the first-type view displayed in the view window may be switched to the second-type view.

[0051] In a possible implementation, the second-type view may be a view generated based on the error address data corresponding to physical addresses of the target test object, and may be configured to indicate actual physical location distribution on the target test
20 object of error addresses in the specified address range of the target test object.

[0052] In a possible implementation, after acquiring the target test data, the logical addresses corresponding to the target test data may be translated by the host computer to

acquire error address data corresponding to the physical addresses. In another possible implementation, the target test data may be translated by the lower-level computer, and the error address data corresponding to the translated physical addresses may be read by the host computer from the lower-level computer. The second-type view may be generated
5 based on the error address data corresponding to the physical addresses by the host computer.

[0053] In an embodiment of the present invention, in response to the detection of the data reading operation in the user interaction interface, the target test data of the specified address range corresponding to the target test object is read. The first-type view is displayed
10 in the view window of the user interaction interface based on the target test data. The user may further perform view switching through the user interaction interface. In response to detection of the view switching on the user interaction interface, the view in the view window may be switched to the second-type view. This allows the user to select different types of views in the user interaction interface to display the error address information
15 corresponding to the target test data. The user may separately select to check: the first-type view configured to indicate the test results of different addresses in the specified address range, and the second-type view configured to indicate the actual location distribution on the target test object of each error address in the specified address range. This facilitates user analysis of the error address information of the target test object through different types
20 of views. By providing different types of views, the user can intuitively check various aspects of the error address information, thereby enabling rapid localization of error addresses on the target test object and efficient analysis of error causes.

[0054] Alternatively, the first-type view may include at least one of a test status view, a logical matrix bitmap, or an error address list.

[0055] The test status view may be configured to indicate test status information of the specified address range. The test status may include Pass/Fail status. The Pass status
5 may indicate that the address testing is passed, and the Fail status may indicate that the address testing is failed, also representing that the tested address is an error address. The test status view may represent an overall test result corresponding to the specified address range. When the target test data indicates that no address test result having the Fail status exists among all address test results in the specified address range, the test status indicated by the
10 test status view may be the Pass status. When the target test data indicates that an address test result having the Fail status exists among all address test results in the specified address range, the test status indicated by the test status view may be the Fail status.

[0056] In a possible implementation, in response to a checking request for the test status view, the test status view corresponding to the target test data may be displayed in a
15 first view window of the user interaction interface.

[0057] A status view checking control for checking the test status view may be provided in the user interaction interface. In a possible implementation, in response to a trigger operation on the status view checking control, it may be determined that a checking request for the test status view is received, and the test status view corresponding to the
20 target test data may be displayed in the first view window of the user interaction interface. Alternatively, the test status view may include an object identifier representing the target test object. The object identifier may have an identifier display form determined according

to target test data of the target test object. When the target test data indicates that the test status of the specified address range corresponding to the target test object is the Pass status, the identifier display form of the object identifier may be a first display form. When the target test data indicates that the test status of the specified address range corresponding to the target test object is the Fail status, the identifier display form of the object identifier may be a second display form. The first display form may be different from the second display form, and may be specifically different in at least one of identifier colors, identifier shapes, or identifier annotations.

[0058] Alternatively, the target test object may include a plurality of digital input/output pins (DQpins), and the target test data may include test data corresponding to the specified address range of each of the plurality of digital input/output pins. Each of the plurality of digital input/output pins may have the same logical address range. When the error address test data of the specified address range corresponding to the target test object is read from the lower-level computer, the error address test data of the specified address range of each of the plurality of digital input/output pins included in the target test object may be read. When the test status view corresponding to the target test data is displayed in the first view window of the user interaction interface, the test status view indicating a test status of each of the plurality of digital input/output pins may be displayed in the first view window of the user interaction interface. The test status corresponding to each of the plurality of digital input/output pins may be determined according to the test data of the specified address range corresponding to each of the plurality of digital input/output pins. In an example, when the test data of the specified address range corresponding to one of the

plurality of digital input/output pins indicates that an address having the Fail status exists in the specified address range corresponding to the digital input/output pin, the test status of the digital input/output pin may be determined to be the Fail status. When the test data of the specified address range corresponding to the digital input/output pin indicates that no

5 address having the Fail state exists in the specified address range corresponding to the digital input/output pin (i.e., each of the addresses has the Pass status), the test status of the digital input/output pin may be determined to be the Pass state. When all digital input/output pins included in the target test object have the Pass status, the test status of the target test object may be the Pass status. When a pin having the Fail status exists in the digital

10 input/output pins of the target test object, the test status of the target test object may be the Fail status. In a possible implementation, a pin identifier corresponding to each of the digital input/output pins may be displayed in the test status view, and each pin identifier may have a display form determined according to a test status of a corresponding digital input/output pin. In an example, when test results of all addresses in the specified address range of a

15 digital input/output pin are in the Pass status, the display form of the pin identifier may be a first display form. When the test results of all the addresses in the specified address range of the digital input/output pin are in the Fail status, the display form of the pin identifier may be a second display form.

[0059] In a possible implementation, both the object identifier configured to indicate

20 the test status of the target test object and the pin identifiers each configured to indicate the test status of corresponding one of the plurality of digital input/output pins included in the target test object may be displayed in the test status view.

[0060] In a possible implementation, when target test data of the plurality of target test objects is read, object identifiers respectively corresponding to the plurality of target test objects may be displayed in the test status view. In response to a selecting operation on an object identifier, a plurality of pin identifiers corresponding to a plurality of digital input/output pins included in a target test object corresponding to the object identifier may be displayed in the test status view. Exemplarily, referring to FIG. 3, object identifiers corresponding to test objects 201, 202, 203, and 204 are displayed in the test status view, and respectively configured to indicate test statuses of the test objects 201, 202, 203, and 204. A plurality of pin identifiers (including pin identifiers of DQL0-DQL7 and pin identifiers of DQU0-DQU7) of a plurality of digital input/output pins included in the test object 201 may be selectively displayed, to respectively indicate test statuses of the digital input/output pins in the test object 201.

[0061] The logical matrix bitmap may be a two-dimensional matrix bitmap configured to indicate test results corresponding to different addresses in the specified address range. In a possible implementation, in response to a checking request for the logical matrix bitmap, the logical matrix bitmap corresponding to the target test data may be displayed in the second view window of the user interaction interface. A matrix bitmap checking control for checking the logical matrix bitmap may be provided in the user interaction interface. In a possible implementation, in response to a trigger operation on the matrix bitmap checking control, it may be determined that a checking request for the logical matrix bitmap is received, and the logical matrix bitmap corresponding to the target test data may be displayed in the second view window of the user interaction interface.

[0062] Alternatively, the logical matrix bitmap corresponding to each of the plurality of digital input/output pins may be generated according to the test data of the plurality of digital input/output pins, and the logical matrix bitmap corresponding to the target test object may include the logical matrix bitmap corresponding to each of the plurality of digital input/output pins. Different matrix units in the logical matrix bitmap may correspond to different logical addresses. A display state of a matrix unit may be determined according to a test result of the corresponding logical address. The display state of a matrix unit corresponding to a logical address whose test result is a Pass status may be different from that of a matrix unit corresponding to a logical address whose test result is a Fail status. Exemplarily, matrix units of different colors may be used to indicate different test results.

[0063] Alternatively, the logical matrix bitmap may include at least one of a thumbnail logical matrix bitmap or a detailed logical matrix bitmap. One matrix unit in the thumbnail logical matrix bitmap may correspond to one logical address range, and one matrix unit in the detailed logical matrix bitmap corresponds to one logical address. In a possible implementation, the thumbnail logical matrix bitmap corresponding to each of the plurality of digital input/output pins may be displayed in the second view window, and/or in response to a selecting operation on a target pin, the detailed logical matrix bitmap corresponding to the target pin may be displayed in the second view window. The thumbnail matrix bitmap corresponding to all digital input/output pins can be displayed in the second view window, which enables quickly checking of the test result of the specified address range for each of the plurality of digital input/output pins. In addition, the detailed logical matrix bitmap of the selected digital input/output pin can also be displayed in the second

view window, so that the detailed test result of each logic address in the specified address range can be checked.

[0064] In a possible implementation, in response to a checking request for the logical matrix view, thumbnail logical matrix bitmaps corresponding to the plurality of digital input/output pins may be displayed in the second view window. In response to a selecting operation on a thumbnail logical matrix bitmap corresponding to one of the plurality of digital input/output pins, a digital input/output pin corresponding to the selected thumbnail logical matrix bitmap may be determined as the target pin. That is, it may be determined that the selecting operation on the target pin is received, and the detailed logical matrix bitmap of the target pin may be displayed in the second view window. Exemplarily, referring to FIG. 4, thumbnail logical matrix bitmaps corresponding to digital input/output pins of the test object 201 are displayed in the second view window. When a selecting operation on DQL0 is received, referring to FIG. 5, a detailed logical matrix bitmap corresponding to the pin DQL0 of the test object 201 is displayed in the second view window.

[0065] In a possible implementation, the detailed logical matrix bitmap and the thumbnail logical matrix bitmap corresponding to the target pin may be displayed simultaneously in the second view window. Alternatively, the detailed logical matrix bitmap corresponding to the target pin may be displayed in a first area of the second view window, while the thumbnail logical matrix bitmap corresponding to the target pin may be displayed in a second area of the second view window. The first area may have a larger area than the second area.

[0066] In an example, the detailed logical matrix bitmap in the first area may be corresponding to a selected matrix bitmap region in the thumbnail logical matrix bitmap in the second area. In response to a selecting operation of an address range on the thumbnail logical matrix bitmap, the detailed logical matrix bitmap displayed in the first area may be updated based on the selected address range. Alternatively, the selecting operation of the address range on the thumbnail logical matrix bitmap may be a frame selecting operation on a partial matrix bitmap region in the thumbnail logical matrix bitmap, and the detailed logical matrix bitmap displayed in the first area may be an enlarged logical matrix bitmap of the framed partial matrix bitmap region. In response to a frame selecting operation on the partial matrix bitmap region in the thumbnail logical matrix bitmap, a corresponding selected address range may be determined according to the framed partial matrix bitmap, and the detailed logical matrix bitmap displayed in the first area may be updated based on test data corresponding to the selected address range. In a possible implementation, in response to a drag operation on the detailed logical matrix bitmap, the selected address range in the thumbnail matrix bitmap may be updated based on a post-drag address range. Alternatively, the user may drag the detailed logical matrix bitmap displayed in the first area. Upon receiving the drag operation on the detailed logical matrix bitmap, the detailed logical matrix bitmap displayed in the first area may be updated based on the drag operation. In addition, the framed partial matrix bitmap region in the thumbnail logical matrix bitmap in the second area may be updated based on an address range corresponding to the updated detailed logical matrix bitmap.

[0067] Alternatively, a horizontal drag axis and a vertical drag axis may be provided

in the first area. In response to a drag operation on the horizontal drag axis and/or the vertical drag axis, the detailed logical matrix bitmap displayed in the first area and the framed partial matrix bitmap region in the thumbnail logical matrix bitmap in the second area may be updated.

5 [0068] In a possible implementation, the second view window may further include a third area configured to display detailed address information. An address information window may be displayed in the third area of the second view window, and address range information corresponding to the detailed logical matrix bitmap currently displayed in the first area may be displayed in the address information window. Specifically, a start address
10 item and an end address item may be displayed in the address information window. A start address of an address range corresponding to the currently displayed detailed logical matrix bitmap may be displayed in the start address item, and an end address of the address range corresponding to the currently displayed detailed logical matrix bitmap may be displayed in the end address item, so that the user can check specific address range information.

15 [0069] Alternatively, in response to an update operation on the address range information in the address information window, the detailed logical matrix bitmap displayed in the first area may be updated based on the updated address range. That is, the user may change the address range in the address information window. In response to the update operation on the address range information, the updated address range may be acquired, and
20 the detailed logical matrix bitmap displayed in the first area may be updated based on the updated address range.

[0070] Alternatively, in response to a drag operation on the detailed logical matrix

bitmap, the address range information in the address information window may be updated based on a post-drag address range information. When the drag operation on the detailed logical matrix bitmap is received, the address range information in the address information window may be updated based on the post-drag address range information, thereby
5 allowing the user to intuitively check the updated address range.

[0071] The address range in the address information window may be corresponding to the selected address range in the thumbnail logical matrix bitmap in the second area, i.e., corresponding to the address range corresponding to the framed partial matrix bitmap region in the thumbnail logical matrix bitmap. In response to an address range update operation on
10 the thumbnail logical matrix bitmap, which updates the framed partial matrix bitmap region, the address range information in the address information window in the third area may be updated.

[0072] Illustratively, referring to FIG. 5, the detailed logical matrix bitmap of the pin DQL0 of the test object 201 may be displayed in the first area 501, and the detailed logical
15 matrix bitmap may be corresponding to the thumbnail logical matrix bitmap in the second area 502. The address information window may be displayed in third area 503, which may be configured to display address range information corresponding to the logical matrix bitmap, and may also be configured to configure address range information to be selected for checking. The address range to be checked may be updated by updating the start address
20 and the end address.

[0073] The error address list may be configured to indicate error addresses in a specified address range. Alternatively, the error address list may include detailed logical

error addresses in the specified address range.

[0074] In a possible implementation, in response to a checking request for the error address list, the error address list corresponding to the target test data may be displayed in a third view window of the user interaction interface.

5 [0075] A list checking control for checking the error address list may be provided in the user interaction interface. In a possible implementation, in response to a trigger operation on the list checking control, it may be determined that the checking request for the error address list is received, and the error address list corresponding to the target test data may be displayed in the third view window of the user interaction interface.

10 [0076] The target test data may include test data of a specified address range of each digital input/output pin. In a possible implementation, the user may select to check error addresses in a target address range falling within the specified address range of a digital input/output pin. That is, in response to selecting operations on the target pin and the target address range, an error address list corresponding to the target address range of the target
15 pin may be displayed in the third view window. After receiving the selecting operations on the target pin and the target address range, test data corresponding to the target address range of the target pin may be acquired. The error address list may be generated based on the test data of the target address range. All logical error addresses (i.e., logical addresses having Fail test results) included in the target address range of the target pin may be listed in
20 the error address list.

[0077] In combination with the above embodiments, in response to the checking request for the error address list, the target pin selected by the user when the detailed logical

matrix bitmap is displayed in the first area may be acquired. In addition, the address range information in the address information window in the third area may be acquired. The address range in the address information window in the third area may be determined as the target address range, and the error address list corresponding to the target address range of the target pin may be generated. That is, after the detailed logical matrix bitmap of the target pin and the corresponding address range information are displayed in the second view window, the user may trigger the display of the error address list for the target pin and corresponding to the address range information in the third view window by performing a trigger operation on the list view control. Alternatively, the target address range may be updated through the update operation on the address in the address range window, thereby triggering an update of the error address list displayed in the third view window.

[0078] In a possible implementation, the first view window, the second view window, and the third view window may be arranged side-by-side, allowing the user to select different view windows to check corresponding error address information.

15 [0079] In an embodiment of the present invention, according to the acquired test data of the error addresses corresponding to the logical addresses, the corresponding test status views, the logical matrix bitmaps and the error address lists may be displayed in the view windows of the user interaction interface. Various error address information may be displayed in different forms, thereby enabling the user to intuitively obtain different error address information of the target test object.

[0080] In an embodiment of the present invention, the detailed logical matrix bitmap and the thumbnail logical matrix bitmap may be displayed simultaneously. The displayed

contents of the detailed logical matrix bitmap and the thumbnail logical matrix bitmap may be corresponding to each other, thereby allowing the user to compare and analyze the information in the detailed logical matrix bitmap and the thumbnail logical matrix bitmap, and thus improving the acquisition efficiency of the error address information.

5 [0081] The storage space in the target lower-level computer for storing the error address test data may include at least one of a Compress Fail Memory (CFM) or an Address Fail Memory (AFM). Compressed test data corresponding to the error address test data may be stored in CFM space, and original error address test data may be stored in AFM space.

[0082] In a possible implementation, the target test data acquired by the host
10 computer from the target lower-level computer may include at least one of the compressed test data or the original test data corresponding to the specified address range.

[0083] Alternatively, the thumbnail logical matrix bitmap may be generated according to the compressed test data. In response to the target test data being the compressed test data, thumbnail logical matrix bitmaps corresponding to the plurality of
15 digital input/output pins may be displayed in the second view window. That is, when the acquired target test data is the compressed test data, thumbnail logical matrix bitmaps corresponding to the plurality of digital input/output pins may be generated according to test data corresponding to the plurality of digital input/output pins included in the compressed test data. The detailed logical matrix bitmap may need to be generated according to the
20 original test data. In response to the target test data being the original test data and the selecting operation on the target pin, the detailed logical matrix bitmap corresponding to the target pin may be displayed in the second view window.

[0084] Alternatively, the user interaction interface may include a parameter configuration page, and the parameter configuration page may be configured to configure access parameters for the storage space. That is, the user may configure the access parameters including the specified address range through the parameter configuration page, 5 thereby enabling the host computer to read the corresponding target test data from the storage space according to the configured access parameters. The parameter configuration page may be displayed in response to a trigger operation on a parameter configuration item in the user interaction interface. The user interaction page may be provided with the parameter configuration item, which is a trigger item for triggering the display of the 10 parameter configuration page. The user may trigger the display of the parameter configuration page through a trigger operation on the parameter configuration item.

[0085] In response to the configuration operation on the parameter configuration page and the data reading operation, the configured access parameters may be acquired, and the target test data may be read based on the access parameters. In a possible 15 implementation, in response to the configuration operation on the parameter configuration page and the data reading operation, the configured access parameters may be acquired, and target test data may be read based on the access parameters.

[0086] Alternatively, the parameter configuration page may include a capture parameter configuration page and an access parameter configuration page. Capture 20 parameters are configured to indicate capture of test data acquired by performing the error address testing on a capture address range of the target test object. Access parameters are configured for accessing the storage space. The user may configure the capture parameters

through the capture parameter configuration page. The capture parameters configured by the user may be acquired and transmitted to the target lower-level computer by the host computer. The lower-level computer of the test device may execute preset test patterns based on the capture parameters to acquire test data from the error address testing
5 performed on the capture address range of the target test object, and store the test data corresponding to the capture address range in the storage space. After the test data corresponding to the capture address range is stored in the storage space, the test data corresponding to the capture address range stored in the storage space may be accessed (i.e., read). The test patterns, which may also be referred to as test configuration information,
10 may include a correspondence between an input signal and an output reference signal. The test patterns may include an input signal input to the object under test and corresponding output reference signal of the object under test. The input signal may include 0 or 1. The output reference signal corresponding to the input signal may be understood as an output truth value corresponding to the input signal, representing information that the object under
15 test should output for the input signal, when the object under test meets the function thereof. In a possible implementation, the preset test patterns may be stored in the target lower-level computer. After receiving the capture parameters transmitted by the host computer, the preset test patterns may be executed based on the capture parameters, and thus the test data corresponding to the capture address range included in the capture parameters may be
20 acquired.

[0087] Alternatively, the capture parameter configuration page may be provided with a capture parameter configuration item for the AFM space and a capture parameter

configuration item for the CFM space. Capture parameters for the AFM space may be configured through the capture parameter configuration item for the AFM space, and capture parameters for the CFM space may be configured through the capture parameter configuration item for the CFM space. In a possible implementation, in response to configuration operations for the capture parameters in the capture parameter configuration items for the AFM space and the CFM space, the capture parameters for the AFM space and the capture parameters for the CFM space may be transmitted to the target lower-level computer, respectively. This enables the corresponding error address test data to be stored in the AFM space and the CFM space. Alternatively, the capture parameters for the AFM space and the CFM space may be identical, so that error address test data of the same address range may be stored in the AFM space and the CFM space. The AFM space may be configured to store original error address test data of the address range, and the CFM space may be configured to store the compressed error address test data of the address range. The user may configure the capture parameters for the AFM space and the capture parameters for the CFM space that include the specified address range. The host computer may transmit the capture parameters for the AFM space and the capture parameters for the CFM space that include the specified address range to the target lower-level computer. The target lower-level computer may execute the preset test patterns based on the capture parameters for the AFM space and the capture parameters for the CFM space, respectively. The original test data of the specified address range may be stored in the AFM space, and the compressed test data of the specified address range may be stored in the CFM space.

[0088] Alternatively, the access parameter configuration page may be provided with

an access parameter configuration item for the AFM space and a access parameter configuration item for the CFM space. Access parameters for the AFM space may be configured through the access parameter configuration item for the AFM space, and access parameters for the CFM space may be configured through the access parameter configuration item for the CFM space. In a possible implementation, an address range included in the access parameters for the AFM space must not exceed the address range included in the capture parameters for the AFM space, and an address range included in the access parameters for the CFM space must not exceed the address range included in the capture parameters for the CFM space.

10 [0089] In a possible implementation, in response to the configuration parameters in the access parameter configuration item for the AFM space, the configured access parameters for the AFM space may be acquired. Based on the specified address range included in the access parameters for the AFM space, the target test data of the specified address range may be read from the AFM space. In response to the configuration parameters in the access parameter configuration item for the CFM space, the configured access parameters for the CFM space may be acquired. Based on the specified address range included in the access parameters for the CFM space, the target test data of the specified address range may be read from the CFM space.

[0090] Alternatively, the access parameters for the storage spaces may be configured by the user through the access parameter configuration items, or corresponding access parameters may be generated automatically based on the capture parameters for the storage space configured by the user. That is, the access parameters for the AFM space may be

generated automatically based on the capture parameters for the AFM space, and the access parameters for the CFM space may be generated automatically based on the capture parameters for the CFM space.

[0091] In a possible implementation, before the capture parameters for the AFM space is configured, capture rule parameters for the AFM space may need to be configured first. The capture parameter configuration items may further be configured to configure the capture rule parameters, which are configured to indicate capture rules for capturing the error address test data and storing the error address test data in the storage space (including the AFM space and the CFM space).

10 [0092] The capture parameter configuration item may include a rule parameter configuration item for configuring the capture rule parameters. Alternatively, the capture rule parameters may include: a storage space available for storing captured test data, a maximum capturable address range, a minimum capturable address range, whether a redundancy mode is enabled, a used functional mode, an address arrangement rule for storing the test data corresponding to each address, write rules for writing the test data into the storage space (for example, a correspondence between bits in the storage space and the plurality of digital input/output pins (DQpin), and types of data that can be written to the storage space), and the like. The rule parameter configuration items may include a configuration term of the capture rule parameters for the CFM space and a configuration term of the capture rule parameters for the AFM space.

[0093] Taking the configuration of the capture rule parameters for the AFM space as an example, when the host computer receives a configuration operation on the configuration

item of the capture rule parameters for the AFM space, the configured capture rule parameters may be acquired. Subsequently, the configured capture rule parameters may be transmitted to the target lower-level computer by the host computer, enabling the target lower-level computer to configure the AFM space according to the capture rule parameters for the AFM space, and thus the error address test data may be captured in the AFM space based on the configured capture rule parameters.

[0094] Alternatively, the access parameter configuration item may include a rule parameter configuration item configured to configure access rule parameters. Alternatively, the access rule parameters may include: an accessible address space in the storage space, a maximum accessible address range, a minimum accessible address range, whether a redundancy mode is enabled, and the like. The rule parameter configuration item may include a configuration item of the access rule parameters for the CFM space and an configuration item of the access rule parameters for the AFM space.

[0095] Taking the configuration of the access rule parameters for the AFM space as an example, when the host computer receives a configuration operation on the configuration item of the access rule parameters for the AFM space, the configured access rule parameters may be acquired. Subsequently, the configured access rule parameters may be transmitted to the target lower-level computer, enabling the target lower-level computer to configure the AFM space according to the access rule parameters for the AFM space.

[0096] In a possible implementation, referring to FIG. 6, a flowchart illustrating the displaying of a first-type view according to an exemplary embodiment is shown. The device for acquiring and displaying error address information may be set to operate in online mode,

and operating conditions for the AFM and/or CFM may be configured (i.e., the configuration of the capture rule parameters and the access rule parameters). The data reading process may be then performed. During the process of reading data, if the reconfigured capture parameters are stored, the AFM space and the CFM space need to be
5 initialized. The test patterns may be executed, and test data of the capture address range indicated by the capture parameters may be stored in the AFM space and the CFM space. Then, AFM data (the original test data) and/or CFM data (the compressed test data) may be read based on the access parameters. If no reconfigured capture parameters exist, the AFM data and/or CFM data may be read directly based on the access parameters.

10 [0097] After reading the CFM data, at least one of the thumbnail logical matrix bitmap or the test status view may be displayed based on the CFM data. Upon reading the AFM data, at least one of the detailed logical matrix bitmap or the error address list may be displayed based on the AFM data. Subsequently, it may be determined whether to reconfigure the operating conditions, i.e., whether to reconfigure the capture rule parameters
15 and the access rule parameters for the AFM space and/or the CFM space. If yes, the data reading process may be re-performed.

[0098] The target test object may include a plurality of digital input/output pins, and the target test data may include test data corresponding to a specified address range of each of the plurality of digital input/output pins. Different logical matrix bitmaps may correspond
20 to test data corresponding to the specified address range of different digital input/output pins. In a possible implementation, a layer superposition operation may be performed on the logical matrix bitmaps corresponding to different pins to compare the error address test

results corresponding to multiple pins. The process may include step 310 and step 320.

[0099] Step 310 includes in response to a layer superposition operation on at least two logical matrix bitmaps, performing a logical operation on the at least two logical matrix bitmaps to acquire a logical superposition layer.

5 [0100] Alternatively, a layer superposition control for triggering layer superposition may be provided in the second view window configured for displaying the logical matrix bitmaps. A pin selection item and an address range configuration item may further be provided in the second view window. The pin selection item may be configured for selection of digital input/output pins to be superposed, and the address range configuration
10 item may be configured for configuration of specific address range for superposing. Alternatively, the address range configuration item may be the address range window displayed in the aforementioned third area, which may be configured to select an address range.

[0101] In a possible implementation, in response to selecting operations on at least
15 two digital input/output pins, an address range, and a logical operation manner, at least two logical matrix bitmaps corresponding to selected address range of the at least two digital input/output pins may be acquired. A logical operation may be performed on the at least two logical matrix bitmaps based on the selected logical operation manner to acquire a logical superposition layer. The logical operation manner may include at least one of an AND
20 operation, an OR operation, or an XOR operation.

[0102] Alternatively, in response to a selecting operation on the pin selection item, at least two selected digital input/output pins may be acquired. In response to selecting

operations on an address range and a logical operation manner, the selected address range and the selected logical operation manner may be acquired.

[0103] Based on the selected address range, test data of the selected address range of the at least two selected digital input/output pins may be acquired. Corresponding logical
5 matrix bitmaps may be then generated based on the test data of the selected address range of the at least two digital input/output pins. Subsequently, the layer superposition operation may be performed on the at least two logical matrix bitmaps based on the selected logic operation manner.

[0104] Alternatively, the logical operation manner may include at least one of an
10 AND operation, an OR operation, or an XOR operation. The AND operation may be configured to filter for Fail addresses that are identical in address in the same address range, thereby enabling the checking and analysis of the identical Fail address distributions across different digital input/output pins in the selected address range. The OR operation may be configured to identify all Fail addresses in the same address range, thereby enabling the
15 checking and analysis of the overall Fail address distributions across different digital input/output pins in the selected address range. The XOR operation may be configured to filter for Fail addresses that differ in address in the same address range, thereby enabling the checking and analysis of different Fail address distributions in the selected address range.

[0105] Alternatively, the layer superposition operation may include at least one of a
20 superposition operation on thumbnail logical matrix bitmaps of the at least two digital input/output pins, or a superposition operation on detailed logical matrix bitmaps of the at least two digital input/output pins.

[0106] Illustratively, referring to FIG. 5, at least two digital input/output pins to be superposed may be selected in an area 504, along with a logical operation manner, and an address range may be selected in a third area 503.

[0107] In a possible implementation, when acquiring the at least two logical matrix
5 bitmaps corresponding to the selected address range of the at least two digital input/output pins, it is necessary to acquire test data corresponding to the selected address range of the at least two digital input/output pins. Alternatively, in response to the selected address range falling within the specified address range, test data corresponding to the selected address range of the at least two digital input/output pins may be obtained from the target test data.
10 When the selected address range falls within the specified address range, the target test data of the specified address range may be cached in the host computer, allowing the test data corresponding to the selected address range of the at least two digital input/output pins to be acquired from the target test data.

[0108] In response to the selected address range falling outside the specified address
15 range, the test data corresponding to the selected address range may be read from the storage space configured to store the error address test data. When the selected address range falls outside the specified address range, the test data of the selected address range may not be cached in the host computer. In this case, the capture parameters and the access parameters including the selected address range may be transmitted to the lower-level
20 computer, thereby enabling the reading of the test data corresponding to the selected address range from the storage space.

[0109] After the test data corresponding to the selected address range is acquired, at

least two corresponding logical matrix bitmaps may be generated.

[0110] In a possible implementation, the layer superposition operation may be performed on the detailed logical matrix bitmaps of the at least two digital input/output pins, and the test data corresponding to the selected address range may be read from the AFM space during a process of reading the test data corresponding to the selected address range from the storage space configured to store the error address test data. Alternatively, in response to the selected address range being greater than a displayed address range, the compressed test data corresponding to the selected address range may be read. In response to the selected address range not being greater than the displayed address range, the original test data of the selected address range may be read. The displayed address range may be an address range corresponding to the number of data points allowed to be displayed in the user interaction interface. Specifically, when the superposed logical superposition layer is displayed in the first area, the displayed address range may be an address range corresponding to the number of the data points allowed to be displayed in the first area.

15 When reading the compressed test data corresponding to the selected address range, the host computer may determine a compression ratio parameter according to the selected address range and the displayed address range, and transmit the compression ratio parameter and the selected address range to the target lower-level computer. The target lower-level computer may read the test data of the selected address range from the AFM space, compress the test data of the selected address range based on the compression ratio parameter to acquire the compressed test data corresponding to the selected address range, and return the compressed test data corresponding to the selected address range to the host computer. The host

computer may generate corresponding logical matrix bitmaps based on the compressed test data corresponding to the selected address range of the selected digital input/output pins, and superpose the generated logical matrix bitmaps to acquire the logical superposition layer.

- 5 [0111] When reading the original test data corresponding to the selected address range, the host computer may transmit the selected address range to the target lower-level computer. The target lower-level computer may read the original test data of the selected address range from the AFM space, and return the original test data corresponding to the selected address range to the host computer. The host computer may generate corresponding
- 10 logical matrix bitmaps based on the original test data corresponding to the selected address range of the selected digital input/output pins, and superpose the generated logical matrix bitmaps to acquire the logical superposition layer.

[0112] Step 320 includes displaying the logical superposition layer in the second view window of the user interaction interface.

- 15 [0113] After the logical matrix bitmaps of the at least two digital input/output pins are superposed, the superposed logical superposition layer may be displayed in the second view window.

- [0114] Alternatively, the superposed logical superposition layer may be displayed in the first area in response to the superposition operation on the detailed logical matrix
- 20 bitmaps of the at least two digital input/output pins. The superposed logical superposition layer may be displayed in the second area in response to the superposition operation on the thumbnail logical matrix bitmaps of the at least two digital input/output pins.

[0115] In a possible implementation, a layer superposition process is shown in FIG.

7. A front-end user interaction interface may receive a selecting operation on different digital input/output pins, receive a selecting operation on a logical operation manner, and create a logical operation expression. A back-end test service unit may parse the logical
5 operation expression and acquire test data according to the selected digital input/output pins and the selected address range. When the test data is not cached in a host computer, the test data may be re-read from a target lower-level computer. In the reading process, when the selected address range is greater than a displayed address range, the compressed test data may be read, and when the selected address range is not greater than the displayed address
10 range, the original test data may be read. When the test data is cached in the host computer, the cached data may be read directly. After the test data is read, a logical operation may be performed on the test data and a logical superposition layer may be acquired. Subsequently, the logical superposition layer may be displayed in the user interaction interface.

[0116] In an embodiment of the present invention, the layer superposition operation
15 may be performed on the logical matrix bitmaps of the plurality of digital input and output pins of the target test object, which facilitates improving the analysis and processing efficiency of the error addresses of the plurality of digital input and output pins.

[0117] In a possible implementation, the second-type view may be a physical matrix view corresponding to physical error address data, and configured to indicate location
20 distribution of each of error addresses of the target test object.

[0118] Alternatively, the process of displaying the second-type view in the view window of the user interaction interface may include step 2301 and step 2302.

[0119] Step 2301 includes acquiring physical error addresses by performing address translation on logical error addresses indicated by the target test data.

[0120] In a possible implementation, the address translation may be performed on the logical error addresses indicated in the target test data to acquire the physical error
5 addresses. The process may include step 1 and step 2.

[0121] Step 1 includes in response to a configuration operation on a configuration item of data source of a user interaction interface, acquiring a configured logical data file and a configured translation rule file.

[0122] The configuration item of the data source may be provided in the user
10 interaction interface, and configured to configure related files for obtaining physical error address data, including a logical data file and a translation rule file. The logical data file may store logical error addresses indicated by the target test data, and the translation rule file may store translation rules for translating logical addresses to physical addresses.

[0123] In a possible implementation, access paths for the logic data file and the
15 translation rule file may be configured, and the logic data file and the translation rule file may be acquired by the host computer according to the access paths.

[0124] Step 2 includes in response to the address translation operation, reading the logical error addresses from the logical data file and the translation rules from the translation rule file, and translate the logical error addresses to the physical error addresses
20 based on the translation rules.

[0125] In a possible implementation, an address translation control may be provided in the configuration item of the data source. In response to a trigger operation on the address

translation control, it may be determined that the address translation operation is received.

The logical error addresses indicated in the target test data may be read from the logical data file, and translated to the physical error addresses based on the translation rules indicated in the translation rule file.

5 [0126] Alternatively, the address translation process may include a partitioning operation on the physical addresses of the target test object and a sorting operation on the logical error addresses. Through partitioning of the physical addresses of the target test object, a physical address space may be divided into different regions. After a logical error address is translated to a physical error address, a physical address space region to which
10 the translated physical error address belongs may be determined based on the divided physical address space regions, enabling rapid localization of the physical location corresponding to the logical error address. The sorting operation on the logical error addresses may be performed based on the physical error addresses, and the physical error addresses may be obtained by translation of the logical error addresses, which facilitates
15 efficient analysis of the physical error addresses.

[0127] In a possible implementation, before the address translation, it may be necessary to configure a physical data source file, which may be a file configured for storing the physical error address data. The configuration of the physical data source file may include: configuring a file path and a file name of the physical data source file. After
20 the address translation, the physical error addresses may be stored in the configured physical data source file based on the configured file path and file name.

[0128] Step 2302 includes displaying a physical matrix bitmap in a view window of

the user interaction interface based on the physical error addresses. The physical matrix bitmap may be configured to indicate location distribution of each of error addresses of the target test object, and the physical matrix bitmap may be marked with the physical error addresses.

5 [0129] In a possible implementation, the physical error addresses may be read from the physical data source file based on the configured file path and file name. The physical matrix bitmap may be generated based on the physical error addresses, and displayed in the view window of the user interaction interface. The physical matrix bitmap may correspond to the entire target test object. The physical error addresses may be acquired by translating
10 the logical error addresses of the digital input/output pins. The generated physical matrix bitmap may illustrate actual physical location distribution on the target test object of the logical error addresses of the digital input/output pins.

[0130] Alternatively, the physical matrix bitmap may include at least one of a thumbnail physical matrix bitmap or a detailed physical matrix bitmap.

15 [0131] The display of the physical matrix bitmap in the view window of the user interaction interface may include step 1 and step 2.

[0132] Step 1 includes displaying the thumbnail physical matrix bitmap in a fourth area of the view window.

[0133] Step 2 includes in response to a selecting operation on an address range in the
20 thumbnail physical matrix bitmap, displaying the detailed physical matrix bitmap corresponding to the selected address range in a fifth area of the view window.

[0134] In a possible implementation, the thumbnail physical matrix bitmap and the

detailed physical matrix bitmap corresponding to the target test object may be displayed simultaneously in the view window. Alternatively, the thumbnail physical matrix bitmap corresponding to the target test object may be displayed in the fourth area of the view window, and the detailed physical matrix bitmap corresponding to the target test object may
5 be displayed in the fifth area. The fifth area may have a larger area than the fourth area. Alternatively, the fourth area may be identical to the aforementioned second area, and the fifth area may be identical to the aforementioned first area.

[0135] In a possible implementation, a selected matrix region in the thumbnail physical matrix bitmap displayed in the fourth area may correspond to the detailed physical
10 matrix bitmap in the fifth area. In response to an operation of address range selection on the thumbnail physical matrix bitmap, the detailed physical matrix bitmap displayed in the fifth area may be updated based on the selected address range. Alternatively, the operation of address range selection on the thumbnail physical matrix bitmap may be a frame selecting operation on a partial matrix bitmap region in the thumbnail physical matrix bitmap, and the
15 detailed physical matrix bitmap displayed in the fifth area may be an enlarged physical matrix bitmap of the framed partial matrix bitmap region. In response to a frame selecting operation on the partial matrix bitmap region in the thumbnail physical matrix bitmap, a corresponding selected address range may be determined according to the framed partial matrix bitmap, and the detailed physical matrix bitmap displayed in the fifth area may be
20 updated based on the physical error addresses corresponding to the selected address range.

In a possible implementation, in response to a drag operation on the detailed physical matrix bitmap, the selected address range in the thumbnail physical matrix bitmap may be updated

based on a post-drag physical address range. Alternatively, the user may drag the detailed physical matrix bitmap displayed in the fifth area. Upon receiving the drag operation on the detailed physical matrix bitmap, the detailed logical matrix bitmap displayed in the fifth area may be updated based on the drag operation. In addition, the framed partial matrix bitmap region in the thumbnail physical matrix bitmap in the fourth area may be updated
5 based on a physical address range corresponding to the updated detailed logical matrix bitmap.

[0136] Alternatively, a horizontal drag axis and a vertical drag axis may be provided in the fifth area. In response to a drag operation on the horizontal drag axis and/or the
10 vertical drag axis, the detailed physical matrix bitmap displayed in the fifth area and the framed partial matrix bitmap region in the thumbnail physical matrix bitmap in the fourth area may be updated.

[0137] In a possible implementation, the user may zoom in on the detailed physical matrix bitmap. In response to a zoom in operation on the detailed physical matrix bitmap,
15 the detailed physical matrix bitmap may be zoomed in accordingly.

[0138] When the detailed physical matrix bitmap is zoomed in to a target state, a logical address corresponding to a target physical address may be displayed in response to a checking operation on the target physical address. The target state may refer to a state in which one physical unit in the detailed physical matrix bitmap corresponds to one physical
20 address.

[0139] Alternatively, the target state may be a maximum zoom-in state of the detailed physical matrix, in which one physical unit in the detailed physical matrix bitmap

may correspond to one physical address. In the target state, in response to the checking operation on the target physical address, the logical address corresponding to the target physical address may be displayed. Alternatively, in response to the selecting operation on the target physical unit corresponding to the target physical address, it may be determined
5 that the checking operation on the target physical address is received, and a superposition sub-window may be displayed in the view window. The superposition sub-window may be configured to display logical address information corresponding to the target physical address.

[0140] Illustratively, referring to FIG. 8, in response to a selecting operation on a
10 target physical unit 801, corresponding logical address information may be displayed in the superposition sub-window 802.

[0141] In a possible implementation, the layer superposition operation may be performed on physical matrix bitmaps corresponding to a plurality of different target test objects, to compare distribution of physical error addresses corresponding to the plurality of
15 test objects. This process may include step 410 and step 420.

[0142] Step 410 includes in response to a layer superposition operation on physical matrix bitmaps of at least two target test objects, superposing the physical matrix bitmaps of the at least two target test objects to acquire a physical superposition layer. The at least two physical matrix bitmaps may respectively correspond to error address test data in a same
20 address range of the at least two target test objects.

[0143] Alternatively, a layer superposition control for triggering layer superposition may be provided in the view window configured to display the physical matrix bitmap. The

view window may further be provided with a target test object selection item for selecting of the target test object to be superposed, and an address range configuration item for configuration of the specific physical address range for superposition.

[0144] In a possible implementation, in response to selecting operations on the at least two target test objects, an address range, and a logical operation manner, at least two physical matrix bitmaps corresponding to the selected address range of the at least two target test objects may be acquired. A logical operation may be performed on the at least two physical matrix bitmaps based on the selected logical operation manner to acquire the physical superposition layer. The logical operation manner may include at least one of an AND operation, an OR operation, or an XOR operation.

[0145] Alternatively, in response to a selecting operation on the target test object selection item, the at least two selected target test objects may be acquired. In response to the selecting operations on the address range and the logical operation manner, the selected physical address range and the selected logical operation manner may be acquired.

15 [0146] Based the selected address range, the physical error addresses in the selected address range of the selected at least two target test objects may be acquired, corresponding physical matrix bitmaps may be generated, and the layer superposition operation may be performed on the at least two physical matrix bitmaps based on the selected logical operation manner.

20 [0147] Alternatively, the logical operation manner may include at least one of an AND operation, an OR operation, or an XOR operation. The AND operation may be configured to filter for Fail addresses that are identical in address in the same address range,

thereby enabling the checking and analysis of the identical Fail address distributions across different target test objects in the selected physical address range. The OR operation may be configured to identify all Fail addresses in the same address range, thereby enabling the checking and analysis of the overall Fail address distributions across different target test
5 objects in the selected physical address range. The XOR operation may be configured to filter for Fail addresses that differ in address in the same address range, thereby enabling the checking and analysis of different Fail address distributions in the selected physical address range.

[0148] Alternatively, the layer superposition operation may include at least one of a
10 superposition operation on thumbnail physical matrix bitmaps of the at least two target test objects, or a superposition operation on detailed logical matrix bitmaps of the at least two target test objects.

[0149] Step 420 includes displaying the physical superposition layer in the view window of the user interaction interface.

15 [0150] Alternatively, in response to the superposition operation on the detailed physical matrix bitmaps of the at least two target test objects, the superposed physical superposition layer may be displayed in the fifth area. In response to the superposition operation on the thumbnail logical matrix bitmaps of the at least two target test objects, the superposed physical superposition layer may be displayed in the fourth area.

20 [0151] In a possible implementation, a physical layer superposition process is shown in FIG. 9. During the process, a front-end user interaction interface may receive a selecting operation on different target test objects, receive a selecting operation on a logical operation

manner, and create a logical operation expression. A back-end test service unit may parse the logical operation expression, acquire data from a physical data source file according to a selected target test object and an address range, and perform a logical operation on the acquired data to acquire a physical superposition layer, which may be displayed in the user
5 interaction interface.

[0152] In an embodiment of the present invention, the layer superposition operation may be performed on the physical matrix bitmaps of the plurality of target test objects, which facilitates improving the analysis and processing efficiency of the position distribution condition of the physical error addresses of the plurality of target test objects.

10 [0153] FIG. 10 is a schematic structural diagram of an apparatus for acquiring and processing error address information according to an exemplary embodiment of the present invention. The apparatus may include a data reading module 1001 and a view display module 1002.

[0154] The data reading module 1001 may be configured to read target test data of a
15 target test object in response to detection of a data reading operation in a user interaction interface. The target test data may include error address test data corresponding to a specified address range in error address test data of the target test object.

[0155] The view display module 1002 may be configured to display a first-type view in a view window of the user interaction interface based on the target test data. The
20 first-type view may be configured to indicate test result information of different addresses in the specified address range.

[0156] The view display module 1002 may further be configured to display a

second-type view in the view window of the user interaction interface based on the target test data, in response to detection of a view switching operation in the user interaction interface. The second-type view may be configured to indicate location distribution information of error addresses in the specified address range on the target test object.

5 [0157] In an exemplary embodiment, the first-type view may include at least one of a test status view, a logical matrix bitmap, or an error address list. The test status view may be configured to indicate test status information of the specified address range. The logical matrix bitmap may be configured to indicate test result information corresponding to each logical address in the specified address range. The error address list may be configured to
10 indicate the error addresses in the specified address range.

[0158] The view display module 1002 may further be configured to perform at least one of the following steps: in response to a checking request for the test status view, displaying the test status view corresponding to the target test data in a first view window of the user interaction interface; in response to a checking request for the logical matrix bitmap,
15 displaying the logical matrix bitmap corresponding to the target test data in a second view window of the user interaction interface; or in response to a checking request for the error address list, displaying the error address list corresponding to the target test data in a third view window of the user interaction interface.

[0159] In an exemplary embodiment, the target test object may include a plurality of
20 digital input/output pins, and the target test data includes test data corresponding to the specified address range of each of the plurality of digital input/output pins.

[0160] The view display module 1002 may further be configured to display a test

status view indicating a test status of each of the plurality of digital input/output pins in the first view window.

[0161] The view display module 1002 may further be configured to perform at least one of the following steps: displaying a thumbnail logical matrix bitmap corresponding to each of the plurality of digital input/output pins in the second view window; or in response to a selecting operation on a target pin, displaying a detailed logical matrix bitmap corresponding to the target pin in the second view window. The target pin may be any one of the plurality of digital input/output pins.

[0162] The view display module 1002 may further be configured for displaying an error address list corresponding to the target address range of the target pin in the third view window in response to selecting operations on the target pin and a target address range. The target address range may belong to the specified address range.

[0163] In an exemplary embodiment, the view display module 1002 may further be configured to display the detailed logical matrix bitmap corresponding to the target pin in a first area of the second view window; display the thumbnail logical matrix bitmap corresponding to the target pin in a second area of the second view window; in response to an operation of address range selection on the thumbnail logical matrix bitmap, update the detailed logical matrix bitmap displayed in the first area based on a selected address range; and in response to a drag operation on the detailed logical matrix bitmap, update the selected address range in the thumbnail logical matrix bitmap based on a post-drag address range.

[0164] In an exemplary embodiment, the view display module 1002 may further be

configured to display an address information window in a third area of the second view window. The address information window may be configured to display address range information corresponding to the detailed logical matrix bitmap currently displayed in the first area.

5 [0165] The view display module 1002 may further be configured to, in response to an update operation on the address range information in the address information window, update the detailed logical matrix bitmap displayed in the first area based on an updated address range; and in response to a drag operation on the detailed logical matrix bitmap, update the address range information in the address information window based on a
10 post-drag address range information.

[0166] In an exemplary embodiment, the target test data may include at least one of compressed test data or original test data corresponding to the specified address range. The view display module 1002 may further be configured to display the thumbnail logical matrix bitmap corresponding to each of the plurality of digital input/output pins in the
15 second view window in response to the target test data being the compressed test data; and display the detailed logical matrix bitmap corresponding to the target pin in the second view window in response to the target test data being the original test data.

[0167] In an exemplary embodiment, the compressed test data may be stored in a compressed data storage space, and the original test data may be stored in an error address
20 storage space. The apparatus may further include a page display module and a data reading module. The page display module may be configured to, in response to a trigger operation on a parameter configuration item in the user interaction interface, display a parameter

configuration page configured for configuration of access parameters for a storage space.

The storage space may include at least one of the compressed data storage space or the error address storage space. The data reading module may further be configured to, in response to a configuration operation on the parameter configuration page and the data reading
5 operation, acquire the configured access parameters, and read the target test data based on the access parameters. The configured access parameters may include a configured specified address range.

[0168] In an exemplary embodiment, the target test object may include a plurality of digital input/output pins, the target test data may include test data corresponding to a
10 specified address range of each of the plurality of digital input/output pins, and different logical matrix bitmaps may correspond to test data corresponding to the specified address range of different digital input/output pins. The apparatus may further include a layer superposition module and a layer display module. The layer superposition module may be configured to, in response to a layer superposition operation on at least two logical matrix
15 bitmaps, perform a logical operation on the at least two logical matrix bitmaps to acquire a logical superposition layer. The layer display module may be configured to display the logical superposition layer in the second view window of the user interaction interface.

[0169] In an exemplary embodiment, the layer superposition module may further be configured to, in response to selecting operations on at least two digital input/output pins, an
20 address range, and a logical operation manner, acquire at least two logical matrix bitmaps corresponding to selected address range of the at least two digital input/output pins; and perform the logical operation on the at least two logical matrix bitmaps based on the

selected logical operation manner to acquire the logical superposition layer. The logical operation manner may include at least one of an AND operation, an OR operation, or an XOR operation.

[0170] The layer superposition module may further be configured to, in response to
5 the selected address range belonging to the specified address range, acquire test data corresponding to the selected address range of the at least two digital input/output pins from the target test data; in response to the selected address range not belonging to the specified address range, read the test data corresponding to the selected address range from a storage space configured to store error address test data; and generate the at least two logical matrix
10 bitmaps based on the test data corresponding to the selected address range.

[0171] In an exemplary embodiment, the layer superposition module may further be configured to, in response to the selected address range being greater than a displayed address range, read compressed test data corresponding to the selected address range. The displayed address range may be an address range allowed to be displayed by the user
15 interaction interface.

[0172] The layer superposition module may further be configured to, in response to the selected address range not being greater than the displayed address range, read original test data corresponding to the selected address range.

[0173] In an exemplary embodiment, the view display module 1002 may further be
20 configured to, acquire physical error addresses by performing address translation on logical error addresses indicated by the target test data; and display a physical matrix bitmap in the view window of the user interaction interface based on the physical error addresses. The

physical matrix bitmap may be configured to indicate location distribution of each of error addresses of the target test object. The physical matrix bitmap may be marked with the physical error addresses.

[0174] In an exemplary embodiment, the view display module 1002 may further be
5 configured to, display a thumbnail physical matrix bitmap in a fourth area of the view window; and in response to a selecting operation on an address range in the thumbnail physical matrix bitmap, display a detailed physical matrix bitmap corresponding to the selected address range in a fifth area of the view window.

[0175] The apparatus may further include a bitmap zoom in module and an address
10 information display module.

[0176] The bitmap zoom in module may be configured to zoom in on the detailed physical matrix bitmap in response to a zoom operation on the detailed physical matrix bitmap.

[0177] The address information display module may be configured to, when the
15 detailed physical matrix bitmap is zoomed in to a target state, display a logical address corresponding to a target physical address in response to a checking operation on the target physical address. The target state may refer to a state in which one physical unit in the detailed physical matrix bitmap corresponds to one physical address.

[0178] In an exemplary embodiment, the layer superposing module may further be
20 configured to, in response to a layer superposition operation on physical matrix bitmaps of at least two target test objects, superpose physical matrix bitmaps of the at least two target test objects to acquire a physical superposition layer. The at least two physical matrix

bitmaps may correspond to error address test data of a same address range of the at least two target test objects, respectively.

[0179] The layer display module may further be configured to display the physical superposition layer in the view window of the user interaction interface.

5 [0180] In an exemplary embodiment, the layer superposition module may further be configured to, in response to selecting operations on the at least two target test objects, an address range, and a logical operation manner, acquire at least two physical matrix bitmaps corresponding to selected address range of the at least two target test objects, and perform a logical operation on the at least two physical matrix bitmaps based on the selected logical
10 operation manner to acquire the physical superposition layer. The logical operation method may include at least one of an AND operation, an OR operation, or an XOR operation.

[0181] In an exemplary embodiment, the view display module 1002 may further be configured to, in response to a configuration operation on a configuration item of data source of a user interaction interface, acquire a configured logical data file and a configured
15 translation rule file. The logical data file may store the logical error addresses indicated by the target test data, and the translation rule file may store translation rules for translating logical addresses to physical addresses.

[0182] The view display module 1002 may further be configured to, in response to the address translation, read the logical error addresses from the logical data file and read
20 the translation rules from the translation rule file, and translate the logical error addresses to physical error addresses based on the translation rules.

[0183] The apparatus may further include a file configuration module and a data

storage module. The file configuration module may be configured to configure a file path and a file name for a physical data source file. The data storage module may be configured to store the physical error addresses in a configured physical data source file. The view display module may further be configured to read the physical error addresses from the
5 physical data source file based on the configured file path and the configured file name, generate the physical matrix bitmap based on the physical error addresses, and display the physical matrix bitmap in the view window of the user interaction interface.

[0184] In addition, an embodiment of the present invention further provides an electronic device, including: a memory, configured to store a computer program; a processor,
10 configured to execute the computer program stored in the memory. The execution of the computer program causes the processor to implement the method of acquiring and processing the error address information according to any one of the foregoing embodiments of the present invention.

[0185] Referring to FIG. 11, the electronic device may include one or more
15 processors and a memory.

[0186] The processor may be a central processing unit (CPU) or other forms of processing units having data processing capabilities and/or instruction execution capabilities, and may control other components in the electronic device to perform desired functions.

[0187] The memory may store one or more computer program products. The
20 memory may include various forms of computer-readable storage media, such as volatile memory and/or non-volatile memory. The volatile memory may include, for example, a random access memory (RAM) and/or a cache. The non-volatile memory may include, for

example, a read-only memory (ROM), a hard disk, a flash memory, and the like. One or more computer program products may be stored on the computer-readable storage medium.

The processor may execute the computer program products to implement the foregoing method for acquiring and processing error address information according to various
5 embodiments of the present invention and/or other desired functions.

[0188] In an example, the electronic device may further include an input device and an output device. These components are interconnected via a bus system and/or other forms of connection mechanism (not shown).

[0189] In addition, the input device may further include, for example, a keyboard, a
10 mouse, and the like.

[0190] The output device may output various information externally, including determined distance information, direction information, and the like. The output device may include, for example, a display, a speaker, a printer, and a communication network and remote output devices connected thereto.

15 [0191] For simplicity, only some of the components related to the present invention in the electronic device are shown in FIG. 11, and components such as buses, input/output interfaces, and the like are omitted. In addition, depending on the specific application, the electronic device may further include any other appropriate components.

[0192] In addition to the aforementioned method and device, an embodiment of the
20 present invention may further provide a computer program product, including computer program instructions. When the computer program instructions are executed by a processor, the processor performs the steps of the method for acquiring and processing error address

information according to various embodiments of the present invention as described in the above sections of this description.

[0193] The computer program product may be written in any combination of one or more programming languages for executing program code that performs the operations of the embodiments of the present invention. The programming languages include object-oriented programming languages, such as Java, C++, etc., as well as conventional procedural programming languages, such as the “C” language or similar programming languages. The program code may execute entirely on a computing device of the user, partly on a device of the user, as a stand-alone software package, partly on the computing device of the user and partly on a remote computing device, or entirely on the remote computing device or server.

[0194] In addition, the embodiments of the present invention may also be a computer-readable storage medium having stored thereon computer program instructions which, when executed by a processor, cause the processor to perform the steps of the method for acquiring and processing error address information according to various embodiments of the present invention as described in the above sections of this description.

[0195] The computer-readable storage medium may employ any combination of one or more readable media. The readable media may include a readable signal medium or a readable storage medium. The readable storage media may include, for example, but are not limited to, an electric, magnetic, optical, electromagnetic, infrared, or semiconductor system, apparatus, or device, or any combination thereof. More specific examples (a non-exhaustive list) of the readable storage medium include: an electrical connection having one or more

wires, a portable disk, a hard disk, a random access memory (RAM), a read-only memory (ROM), an erasable programmable read-only memory (EPROM or Flash memory), an optical fiber, a portable compact disk read-only memory (CD-ROM), an optical storage device, a magnetic storage device, or any suitable combination thereof.

5 [0196] The basic principle of the present invention is described above in connection with specific embodiments. However, it should be noted that the advantages, benefits, effects and the like mentioned in the present invention are merely examples and not limiting. These advantages, benefits, effects and the like should not be considered as necessary to the various embodiments of the present invention. In addition, the specific details disclosed
10 above are merely for the purpose of illustration and ease of understanding, rather than limiting. The above details are not intended to limit the present invention to be implemented by using the specific details described above.

[0197] The various embodiments in this description are described in a progressive manner, with each embodiment focusing on differences from other embodiments. For
15 identical or similar parts among the various embodiments, reference may be made to each other. As for the system embodiments, since the system embodiments substantially correspond to the method embodiments, the description is relatively brief, and reference may be made to some descriptions in the method embodiment for related parts.

[0198] The block diagrams of devices, apparatuses, equipment, and systems involved
20 in the present invention are merely illustrative examples and are not intended to require or imply that connections, arrangements, and configurations must be made in the manner shown in the block diagrams. As will be appreciated by those skilled in the art, these

devices, apparatus, equipment, and systems may be connected, arranged, and configured in any manner. Words such as “comprise”, “include”, “have”, and the like are open-ended words, meaning “including, but not limited to”, and may be used interchangeably therewith.

As used herein, the terms “or” and “and” refer to a term “and/or” and may be used
5 interchangeably therewith, unless the context clearly indicates otherwise. The term “such as” as used herein refers to the phrase “such as but not limited to” and may be used interchangeably therewith.

[0199] The method and apparatus of the present invention may be implemented in many ways. For example, the method and apparatus of the present invention may be
10 implemented by using software, hardware, firmware, or any combination thereof. The above sequence of steps for the method is for illustration only, and the steps of the method of the present invention are not limited to the sequence specifically described above, unless otherwise specifically stated. In addition, in some embodiments, the present invention may also be implemented as programs recorded in a recording medium, and these programs
15 include machine-readable instructions for implementing the method according to the present invention. Accordingly, the present invention also covers a recording medium storing a program for executing the method according to the present invention.

[0200] It should further be noted that, in the apparatus, device, and method of the present invention, various components or steps may be decomposed and/or recombined. The
20 decomposition and/or recombination should be regarded as equivalents of the present invention.

[0201] The above description of the disclosed aspects is provided to enable those

skilled in the art to make or use the present invention. Various modifications to these aspects will be readily apparent to those skilled in the art, and the generic principles defined herein may be applied to other aspects without departing from the scope of the present invention. Therefore, the present invention is not intended to be limited to the aspects shown herein,
5 but is to be accorded the broadest scope consistent with the principles and novel features disclosed herein.

[0202] The above description has been provided for purposes of illustration and description. Furthermore, this description is not intended to limit the embodiments of the present invention to the forms disclosed herein. While multiple exemplary aspects and
10 embodiments have been discussed above, those skilled in the art will recognize certain variations, modifications, alterations, additions, and sub-combinations thereof.

CLAIMS

What is claimed is:

1. A method for acquiring and processing error address information, characterized by comprising:

5 reading target test data of a target test object in response to detection of a data reading operation in a user interaction interface, wherein the target test data comprises error address test data corresponding to a specified address range in error address test data of the target test object;

 displaying a first-type view in a view window of the user interaction interface based on
10 the target test data, wherein the first-type view is configured to indicate test result information of different addresses in the specified address range; and

 displaying a second-type view in the view window of the user interaction interface based on the target test data, in response to detection of a view switching operation in the user interaction interface, wherein the second-type view is configured to indicate location
15 distribution information of error addresses in the specified address range on the target test object.

2. The method of claim 1, wherein the first-type view comprises at least one of a test status view, a logical matrix bitmap, or an error address list, the test status view is configured to indicate test status information of the specified address range, the logical matrix bitmap is
20 configured to indicate test result information corresponding to each logical address in the specified address range, and the error address list is configured to indicate the error addresses in the specified address range; and

displaying the first-type view in the view window of the user interaction interface further comprises at least one of the following steps:

in response to a checking request for the test status view, displaying the test status view corresponding to the target test data in a first view window of the user interaction interface;

in response to a checking request for the logical matrix bitmap, displaying the logical matrix bitmap corresponding to the target test data in a second view window of the user interaction interface; or

in response to a checking request for the error address list, displaying the error address list corresponding to the target test data in a third view window of the user interaction interface.

3. The method of claim 2, wherein the target test object comprises a plurality of digital input/output pins, and the target test data comprises test data corresponding to the specified address range of each of the plurality of digital input/output pins;

displaying the test status view corresponding to the target test data in the first view window of the user interaction interface further comprises: displaying a test status view indicating a test status of each of the plurality of digital input/output pins in the first view window;

displaying the logical matrix bitmap corresponding to the target test data in the second view window of the user interaction interface further comprises at least one of the following steps: displaying a thumbnail logical matrix bitmap corresponding to each of the plurality of digital input/output pins in the second view window; or in response to a selecting operation

on a target pin, displaying a detailed logical matrix bitmap corresponding to the target pin in the second view window, wherein the target pin is any one of the plurality of digital input/output pins; and

displaying the error address list corresponding to the target test data in the third view window of the user interaction interface further comprises: in response to selecting operations on the target pin and a target address range, displaying an error address list corresponding to the target address range of the target pin in the third view window, wherein the target address range belongs to the specified address range.

4. The method of claim 3, wherein displaying the detailed logical matrix bitmap corresponding to the target pin in the second view window further comprises:

displaying the detailed logical matrix bitmap corresponding to the target pin in a first area of the second view window; and

the method further comprises:

displaying the thumbnail logical matrix bitmap corresponding to the target pin in a second area of the second view window;

in response to an operation of address range selection on the thumbnail logical matrix bitmap, updating the detailed logical matrix bitmap displayed in the first area based on a selected address range; and

in response to a drag operation on the detailed logical matrix bitmap, updating the selected address range in the thumbnail logical matrix bitmap based on a post-drag address range.

5. The method of claim 4, further comprising:

displaying an address information window in a third area of the second view window, wherein the address information window is configured to display address range information corresponding to the detailed logical matrix bitmap currently displayed in the first area;

in response to an update operation on the address range information in the address
5 information window, updating the detailed logical matrix bitmap displayed in the first area based on an updated address range; and

in response to a drag operation on the detailed logical matrix bitmap, updating the address range information in the address information window based on a post-drag address range information.

10 6. The method of claim 3, wherein the target test data comprises at least one of compressed test data or original test data corresponding to the specified address range;

displaying the thumbnail logical matrix bitmap corresponding to each of the plurality of digital input/output pins in the second view window is performed in response to the target test data being the compressed test data; and

15 displaying the detailed logical matrix bitmap corresponding to the target pin in the second view window is performed in response to the target test data being the original test data.

7. The method of claim 6, wherein the compressed test data is stored in a compressed data storage space, and the original test data is stored in an error address storage space;

20 before reading the target test data of the target test object in response to detection of the data reading operation in the user interaction interface, the method further comprises:

in response to a trigger operation on a parameter configuration item in the user interaction interface, displaying a parameter configuration page configured to configure access parameters for a storage space, wherein the storage space comprises at least one of the compressed data storage space or the error address storage space; and

5 reading the target test data of the target test object further comprises:

in response to a configuration operation on the parameter configuration page and the data reading operation, acquiring the configured access parameters, and reading the target test data based on the access parameters, wherein the configured access parameters comprise a configured specified address range.

10 8. The method of any one of claims 2 to 7, wherein the target test object comprises a plurality of digital input/output pins, the target test data comprises test data corresponding to a specified address range of each of the plurality of digital input/output pins, and different logical matrix bitmaps correspond to test data corresponding to the specified address range of different digital input/output pins; and

15 the method further comprises:

in response to a layer superposition operation on at least two logical matrix bitmaps, performing a logical operation on the at least two logical matrix bitmaps to acquire a logical superposition layer; and

displaying the logical superposition layer in the second view window of the user
20 interaction interface.

9. The method of claim 8, wherein in response to the layer superposition operation on the at least two logical matrix bitmaps, performing the logical operation on the at least two logical

matrix bitmaps to acquire the logical superposition layer further comprises:

in response to selecting operations on at least two digital input/output pins, an address range, and a logical operation manner, acquiring at least two logical matrix bitmaps corresponding to selected address range of the at least two digital input/output pins; and
5 performing the logical operation on the at least two logical matrix bitmaps based on the selected logical operation manner to acquire the logical superposition layer, wherein the logical operation manner comprises at least one of an AND operation, an OR operation, or an XOR operation.

10. The method of claim 9, wherein acquiring the at least two logical matrix bitmaps
10 corresponding to the selected address range of the at least two digital input/output pins further comprises:

in response to the selected address range belonging to the specified address range, acquiring test data corresponding to the selected address range of the at least two digital input/output pins from the target test data;

15 in response to the selected address range not belonging to the specified address range, reading the test data corresponding to the selected address range from a storage space configured to store error address test data; and

generating the at least two logical matrix bitmaps based on the test data corresponding to the selected address range.

20 11. The method of claim 10, wherein reading the test data corresponding to the selected address range from the storage space configured to store the error address test data further comprises:

in response to the selected address range being greater than a displayed address range, reading compressed test data corresponding to the selected address range, wherein the displayed address range is an address range allowed to be displayed by the user interaction interface; and

5 in response to the selected address range not being greater than the displayed address range, reading original test data corresponding to the selected address range.

12. The method of any one of claims 1 to 7, wherein displaying the second-type view in the view window of the user interaction interface based on the target test data further comprises:

10 acquiring physical error addresses by performing address translation on logical error addresses indicated by the target test data; and

displaying a physical matrix bitmap in the view window of the user interaction interface based on the physical error addresses, wherein the physical matrix bitmap is configured to indicate location distribution of each of error addresses of the target test
15 object, and the physical matrix bitmap is marked with the physical error addresses.

13. The method of claim 12, wherein displaying the physical matrix bitmap in the view window of the user interaction interface further comprises:

displaying a thumbnail physical matrix bitmap in a fourth area of the view window;

in response to a selecting operation on an address range in the thumbnail physical
20 matrix bitmap, displaying a detailed physical matrix bitmap corresponding to the selected address range in a fifth area of the view window; and

in response to a drag operation on the detailed physical matrix bitmap, updating the selected address range in the thumbnail physical matrix bitmap based on a post-drag address range.

14. The method of claim 13, further comprising:

5 zooming in on the detailed physical matrix bitmap in response to a zoom operation on the detailed physical matrix bitmap; and

when the detailed physical matrix bitmap is zoomed in to a target state, displaying a logical address corresponding to a target physical address in response to a checking operation on the target physical address, wherein the target state refers to a state in which
10 one physical unit in the detailed physical matrix bitmap corresponds to one physical address.

15. The method of claim 12, further comprising:

in response to a layer superposition operation on physical matrix bitmaps of at least two target test objects, superposing physical matrix bitmaps of the at least two target test
15 objects to acquire a physical superposition layer, wherein the at least two physical matrix bitmaps correspond to error address test data of a same address range of the at least two target test objects, respectively; and

displaying the physical superposition layer in the view window of the user interaction interface.

20 16. The method of claim 15, wherein in response to the layer superposition operation on physical matrix bitmaps of the at least two target test objects, superposing the physical

matrix bitmaps of the at least two target test objects to acquire the physical superposition layer, further comprises:

in response to selecting operations on the at least two target test objects, an address range, and a logical operation manner, acquiring at least two physical matrix bitmaps
5 corresponding to selected address range of the at least two target test objects, and performing a logical operation on the at least two physical matrix bitmaps based on the selected logical operation manner to acquire the physical superposition layer, wherein the logical operation method comprises at least one of an AND operation, an OR operation, or an XOR operation.

10 17. The method of claim 12, wherein acquiring the physical error addresses by performing the address translation on the logical error addresses indicated by the target test data further comprises:

in response to a configuration operation on a configuration item of data source of a user interaction interface, acquiring a configured logical data file and a configured
15 translation rule file, wherein the logical data file stores the logical error addresses indicated by the target test data, and the translation rule file stores translation rules for translating logical addresses to physical addresses; and

in response to the address translation, reading the logical error addresses from the logical data file and reading the translation rules from the translation rule file, and
20 translating the logical error addresses to physical error addresses based on the translation rules.

18. The method of claim 17, further comprising:

configuring a file path and a file name for a physical data source file; and

storing the physical error addresses in a configured physical data source file,

wherein displaying the physical matrix bitmap in the view window of the user

5 interaction interface based on the physical error address further comprises:

reading the physical error addresses from the physical data source file based on

the configured file path and the configured file name,

generating the physical matrix bitmap based on the physical error addresses; and

displaying the physical matrix bitmap in the view window of the user interaction

10 interface.

19. An electronic device, characterized by comprising:

a memory, configured to store a computer program;

a processor, configured to execute the computer program stored in the memory,

wherein the execution of the computer program causes the processor to implement the

15 method for acquiring and processing the error address information according to any one of
claims 1 to 18.