target range to be determined (e.g., minimum resistivity, maximum resistivity, or range of resistivity). For example, for p-type substrates, the pre-anneal target resistivity equals the post-anneal target resistivity minus the increase in resistivity caused by thermal donor formation during the anneal. For n-type substrates the pre-anneal target resistivity equals the post-anneal target resistivity plus the decrease in resistivity caused by thermal donor formation during the anneal.

[0037] Any suitable model may be used to determine the change of resistivity from thermal donor generation during the anneal(s). For example, the model may be based on calculations from or derived from Voronkov et al., "Properties of Fast-Diffusing Oxygen Species in Silicon Deduced from the Generation Kinetics of Thermal Donors", Solid State Phenomena, Vols. 156-158 (2010), pp. 115-122, which is incorporated herein by reference for all relevant and consistent purposes. The calculations may be based on other published studies of thermal donor formation such as Londos et al., "Effect of Oxygen Concentration on the Kinetics of Thermal Donor Formation in Silicon at Temperatures between 350 and 500°C", Applied Physics Letters Vol. 62, 1525 (1993), which is also incorporated herein by reference for all relevant and consistent purposes. In some embodiments, the model may be based on empirical data relating to changes in resistivity that occur during the anneal.

[0038] In some embodiments, inputs 210 related to the anneal and/or substrate may be input into the model to determine thermal donor formation and/or changes in resistivity that occur during the anneal. For example,

a wide area network (WAN), a mesh network, and/or any other network to communicate with remote devices and systems via the network.

[0054] The computer systems discussed herein may include additional, less, or alternate functionality, including that discussed elsewhere herein. The computer systems discussed herein may include or be implemented via computer-executable instructions stored on non-transitory computer-readable media or medium.

[0055] In an example embodiment for executing step 200, the computer device 400 includes a model (e.g., simulation) of the resistivity change due to thermal donor formation for a range of anneal temperatures and lengths. In an example embodiment for executing step 300, the computer device 400 includes a model (e.g., simulation) of the resistivity of an ingot formed from a silicon melt based on an initial doping amount (e.g., p-type such as boron) and/or with various counter-doping amounts.

[0056] Once the counter-doping schedule is determined, in step 400 an ingot may be grown according to the counter-doping schedule. In accordance with embodiments of the present disclosure and with reference to Figure 2, the ingot is grown by the so-called Czochralski process in which the ingot is withdrawn from a silicon melt 44 held within a crucible 22 of an ingot puller 23.

[0057] The ingot puller 23 includes a housing 26 that defines a crystal growth chamber 16 and a pull chamber 20 having a smaller transverse dimension than the growth chamber. The growth chamber 16 has a generally dome shaped upper wall 45 transitioning from the growth chamber

16 to the narrowed pull chamber 20. The ingot puller 23 includes an inlet port 7 and an outlet port 12 which may be used to introduce and remove a process gas to and from the housing 26 during crystal growth.

[0058] The crucible 22 within the ingot puller 23 contains the silicon melt 44 from which a silicon ingot is drawn. The silicon melt 44 is obtained by melting polycrystalline silicon charged to the crucible 22. The crucible 22 is mounted on a turntable 31 for rotation of the crucible about a central longitudinal axis X of the ingot puller 23.

[0059] A heating system 39 (e.g., an electrical resistance heater 39) surrounds the crucible 22 for melting the silicon charge to produce the melt 44. The heater 39 may also extend below the crucible as shown in U.S. Patent No. 8,317,919. The heater 39 is controlled by a control system (not shown) so that the temperature of the melt 44 is precisely controlled throughout the pulling process. Insulation (not shown) surrounding the heater 39 may reduce the amount of heat lost through the housing 26. The ingot puller 23 may also include a heat shield assembly (not shown) above the melt surface for shielding the ingot from the heat of the crucible 22 to increase the axial temperature gradient at the solid-melt interface.

[0060] A pulling mechanism (not shown) is attached to a pull wire 24 that extends down from the mechanism. The mechanism is capable of raising and lowering the pull wire 24. The ingot puller 23 may have a pull shaft rather than a wire, depending upon the type of puller. The

pull wire 24 terminates in a pulling assembly 58 that includes a seed crystal chuck 32 which holds a seed crystal 6 used to grow the silicon ingot. In growing the ingot, the pulling mechanism lowers the seed crystal 6 until it contacts the surface of the silicon melt 44. Once the seed crystal 6 begins to melt, the pulling mechanism slowly raises the seed crystal up through the growth chamber 16 and pull chamber 20 to grow the monocrystalline ingot. The speed at which the pulling mechanism rotates the seed crystal 6 and the speed at which the pulling mechanism raises the seed crystal (i.e., the pull rate v) are controlled by the control system.

[0061] A process gas is introduced through the inlet port 7 into the housing 26 and is withdrawn from the outlet port 12. The process gas creates an atmosphere within the housing and the melt and atmosphere form a melt-gas interface. The outlet port 12 is in fluid communication with an exhaust system (not shown) of the ingot puller.

[0062] In this regard, the ingot puller 23 shown in Figure 1 and described herein is exemplary and other crystal puller configurations and arrangements may be used to pull a single crystal silicon ingot from a melt unless stated otherwise.

[0063] In accordance with embodiments of the present disclosure, polycrystalline silicon is added to the crucible 22. The polycrystalline silicon is heated to cause silicon to liquefy and form a melt in the crucible. A dopant (e.g., p-type such as boron) is added to the crucible (before or after melting of the polycrystalline silicon).

[0064] While the methods of the present disclosure have been described with reference to the first dopant being a p-type dopant (e.g., boron but also gallium, aluminum or indium) and the counter-dopant or "second" dopant being an n-type dopant (e.g., phosphorous but also antimony or arsenic), in other embodiments, the main dopant may be one or more n-type dopants and the counter-dopant may be a p-type dopant (i.e., the first dopant is p-type or n-type and the second dopant is a type different from the type of the first dopant). When phosphorous is added, any suitable source of phosphorous may be used.

[0065] By counter-doping to achieve the desired pre-anneal resistivity, the length of the constant diameter portion or "main body" of the ingot that is within the target pre-anneal resistivity range (i.e., "prime" portion) may be increased. For example, at least 50% of the length of the constant diameter portion may be within the pre-anneal wafer resistivity target range or at least 60%, at least 70%, at least 80%, at least 90%, at least 95% or the entire constant diameter portion of the ingot is within the pre-anneal wafer resistivity target range.

[0066] In some embodiments, after the ingot is grown, wafers are sliced from the portion of the ingot within the pre-anneal wafer resistivity target range. Devices such as interposer devices are built upon the wafers with the heat treatments described above being performed as part of the device fabrication process. The device may be any device in which thermal donors form as part of the device fabrication process. In some embodiments, the device is an interposer. In some embodiments, the

CLAIMS:

1. A method for producing a single crystal silicon ingot from a silicon melt held within a crucible, the method comprising:

determining a post-anneal target resistivity for wafers sliced from the ingot;

modeling thermal donors generated during a subsequent anneal of wafers sliced from the ingot to determine a pre-anneal wafer resistivity target range;

modeling a dopant profile of the melt during ingot growth to determine a counter-doping schedule in which at least a portion of the ingot is within the pre-anneal wafer resistivity target range;

adding polycrystalline silicon to the crucible;

heating the polycrystalline silicon to cause a silicon melt to form in the crucible;

adding a first dopant to the crucible, the first dopant being p-type or n-type;

contacting the melt with a seed crystal;

withdrawing the seed crystal from the melt to form a single crystal silicon ingot; and

adding a second dopant to the silicon melt while forming the single crystal silicon ingot based on the counter-doping schedule, the second dopant being p-type or n-type and being of a type different from the type of the first dopant.

2. The method as set forth in claim 1 wherein modeling thermal donors generated during a subsequent anneal of wafers sliced from the ingot comprises inputting

the temperature of the anneal and the length of the anneal into the model.

3. The method as set forth in claim 2 wherein modeling thermal donors generated during a subsequent anneal of wafers sliced from the ingot comprises inputting the oxygen content of the wafer into the model.

4. The method as set forth in claim 2 or claim 3 wherein the anneal is at a temperature of at least 300°C.

5. The method as set forth in claim 2 or claim 3 wherein the anneal is at a temperature of at least 450°C.

6. The method as set forth in any one of claims 2 to 5 wherein the length of the anneal is at least 5 hours.

7. The method as set forth in any one of claims 2 to 6 wherein the length of the anneal is at least 20 hours.

8. The method as set forth in any one of claims 2 to 7 wherein the anneal is part of a device manufacturing process.

9. The method as set forth in claim 8 wherein the device manufacturing process comprises forming an interposer device.

10. The method as set forth in any one of claims 1 to 9 wherein the first dopant is p-type.

11. The method as set forth in claim 10 wherein the first dopant is selected from the group consisting of boron, gallium, aluminum, and indium.

12. The method as set forth in claim 10 wherein the first dopant is boron.

13. The method as set forth in any one of claims 10 to 12 wherein the second dopant is n-type and selected from the group consisting of phosphorous, antimony, and arsenic.

14. The method as set forth in any one of claims 10 to 12 wherein the second dopant is n-type and is phosphorous.

15. The method as set forth in any one of claims 1 to 14 wherein the ingot has a constant diameter portion and at least 50% of the length of the constant diameter portion is within the pre-anneal wafer resistivity target range.

16. The method as set forth in any one of claims 1 to 14 wherein the ingot has a constant diameter portion and the entire constant diameter portion of the ingot is within the pre-anneal wafer resistivity target range.

17. The method as set forth in any one of claims 1 to 16 wherein the post-anneal target resistivity comprises a minimum resistivity, maximum resistivity, or a range of resistivity.

18. The method as set forth in claim 17 wherein the post-anneal target resistivity is at least 75 Ω-cm.

19. The method as set forth in any one of claims 1 to 18 wherein modeling the thermal donors generated during a subsequent anneal of wafers sliced from the ingot

to determine a pre-anneal wafer resistivity target range comprises:

storing in the memory of a computer system a model for determining a pre-anneal wafer resistivity target range of a wafer sliced from the ingot; and

executing the model using the oxygen content of the wafer, a length of the anneal, and the temperature of the anneal as inputs.

20. The method as set forth in any one of claims 1 to 19 wherein modeling a dopant profile of the melt during ingot growth to determine a counter-doping schedule in which the ingot is within the pre-anneal wafer resistivity target range comprises:

storing in the memory of a computer system a model for determining a dopant profile of the melt during ingot growth; and

executing the model using an initial doping amount of the melt and the pre-anneal wafer resistivity target range.