CLAIMS

1. ~~A method of forming a~~A semiconductor device, comprising:

~~forming~~ two vertical field effect transistors~~ on a substrate~~, each ~~of the~~ vertical field effect ~~transistors~~transistor comprising an epitaxial region located above a channel region and below a dielectric cap, the epitaxial region comprising two opposing protruding regions of triangular shape that extend horizontally beyond the channel region;

~~depositing~~ a metal gate material disposed on and around the channel region, wherein a portion of the metal gate material is located between the two vertical field effect transistors;

~~depositing~~ an interlevel dielectric layer above the metal gate material; and

~~recessing the interlevel dielectric layer to form two openings, each opening is adjacent to a side of each vertical field effect transistor that is opposing the portion of the metal gate material located between the two vertical field effect transistors, wherein each opening exposes a portion of the epitaxial region of each vertical field effect transistor; and~~

~~depositing, within each of the two openings, a resistive random access memory stack comprising an oxide layer located directly above the exposed portion of the epitaxial region, a top electrode layer directly above the oxide layer and a metal fill above the top electrode layer, wherein the exposed portion of the epitaxial region acts as a bottom electrode for the resistive random access memory stack.~~

~~2. The method of claim 1, wherein forming the two vertical field effect transistors further comprises:~~

~~forming a doped source on the substrate;~~

~~forming the channel region extending from the doped source;~~

~~forming the dielectric cap above the channel region; and~~

~~forming the epitaxial region off a portion of the channel region.~~

~~3. The method of claim 2, further comprising:~~

~~forming a counter-doped layer between the substrate and the doped source, wherein the doped source comprises a first dopant, and the counter-doped layer comprises a second dopant that is different than the first dopant.~~

~~4. The method of claim 1, further comprising:~~

~~etching the resistive random access memory stack in preparation for contact formation.~~

~~5. The method of claim 4, further comprising:~~

~~forming a resistive random access memory contact contacting a top portion of the metal fill in each of the two vertical field effect transistors.~~

~~6. The method of claim 2, further comprising:~~

~~forming a source/drain contact contacting the doped source.~~

~~7. The method of claim 1, further comprising:~~

~~forming a gate contact contacting the metal gate material.~~

~~8. A semiconductor device, comprising:~~

~~two vertical field effect transistors, each vertical field effect transistor comprising an epitaxial region located above a channel region and below a dielectric cap, the epitaxial region comprising two opposing protruding regions of triangular shape that extend horizontally beyond the channel region;~~

~~a metal gate material disposed on and around the channel region, wherein a portion of the metal gate material is located between the two vertical field effect transistors;~~

~~an interlevel dielectric layer above the metal gate material; and~~

~~two~~ resistive random access memory structures, each resistive random access memory is adjacent to a side of a vertical field effect transistor of the two vertical field effect transistors that is opposing the portion of the metal gate material located between the two vertical field effect transistors, wherein each of the resistive random access memory structures comprises an oxide layer located directly above the epitaxial region, a top electrode layer directly above the oxide layer and a metal fill above the top electrode layer, wherein the epitaxial region acts as a bottom electrode for the resistive random access memory structure.

~~9.~~ 2. The semiconductor device of claim ~~8~~1, wherein the two vertical field effect transistor further comprises:

~~a~~ doped source on a substrate, the channel region extending from the doped source.

~~10.~~ 3. The semiconductor device of claim ~~9~~2, further comprises:

a counter-doped layer between the substrate and the doped source, wherein the doped source comprises a first dopant, and the counter-doped layer comprises a second dopant that is different than the first dopant.

~~a counter-doped layer between the substrate and the doped source, wherein the doped source comprises a first dopant, and the counter-doped layer comprises a second dopant that is different than the first dopant.~~

~~11.~~

4. The semiconductor device of claim ~~10~~3, further comprising:

~~a~~ source/drain contact contacting the doped source.

~~12.~~ 5. The semiconductor device of claim ~~8~~1, further comprising:

~~a~~ gate contact contacting the metal gate material.

~~13.~~ 6. The semiconductor device of claim ~~8~~1, further comprising:

~~a~~ resistive random access memory contact contacting a top portion of the metal fill in each vertical field effect transistor.