(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
16 January 2003 (16.01.2003)

PCT

(10) International Publication Number
WO 03/005447 A2

(51) International Patent Classification[7]: H01L 27/108, 21/8242

(21) International Application Number: PCT/GB02/02961

(22) International Filing Date: 27 June 2002 (27.06.2002)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/897,868 2 July 2001 (02.07.2001) US

(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NY 10504 (US).

(71) Applicants *(for MG only)*: **IBM UNITED KINGDOM LIMITED** [GB/GB]; PO Box 41, North Harbour, Portsmouth, Hampshire PO6 3AU (GB). **INFINEON TECHNOLOGIES AG** [DE/DE]; St. Martin Strasse 53, 81669 Munchen (DE).

(72) Inventors: **DIVAKARUNI, Ramachandra**; 131B Heritage Hills, Somers, NY 10589 (US). **GRUENING, Ulrike**; Rainfalerstr. 36, 81539 Munchen (DE). **MANDELMAN, Jack**; 5 Jamie Lane, Stormville, NY 12582 (US). **NESBIT, Larry**; 24 Fawn Drive, Farmington, CT 06032 (US). **RADENS, Carl**; 35 Kuchler Drive, LaGrangeville, NY 12540 (US).

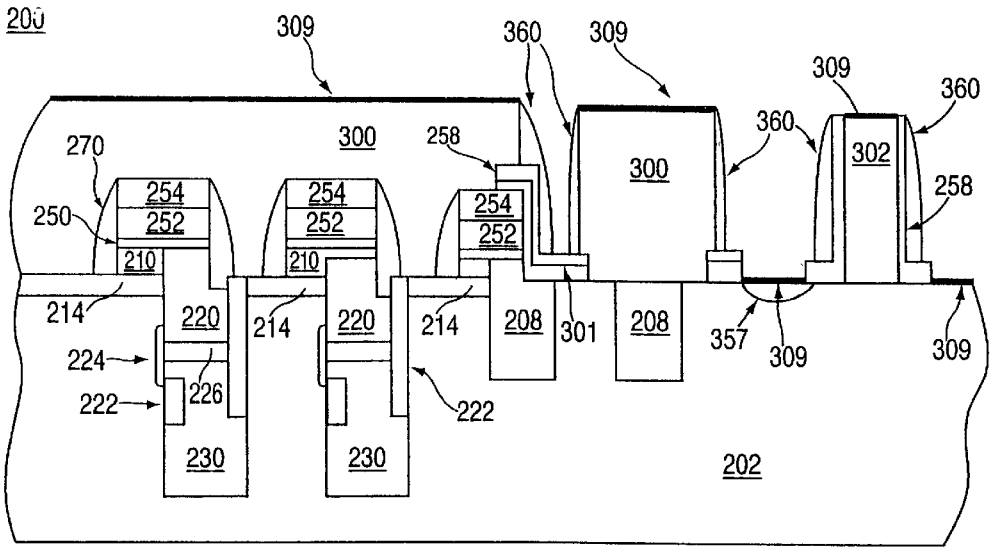
(74) Agent: **MOSS, Robert, Douglas**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Winchester, Hampshire SO21 2JN (GB).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZM, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: STRUCTURE AND METHOD OF FABRICATING EMBEDDED VERTICAL DRAM ARRAYS WITH SILICIDED BITLINE AND POLYSILICON INTERCONNECT



(57) Abstract: A structure and process for fabricating embedded vertical DRAM cells includes fabricating vertical MOSFET DRAM cells with silicided polysilicon layers in the array regions, the landing pad and/or interconnect structures, the support source and drain regions and/or the gate stack. The process eliminates the need for a M0 metallization layer.

WO 03/005447 A2

Published:

— *without international search report and to be republished upon receipt of that report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.