STRESSED SEMICONDUCTOR-ON-INSULATOR STRUCTURE RESISTANT TO HIGH-TEMPERATURE STRESS

The present invention relates to a semiconductor-on-insulator structure (or SeOI) designed for electronics, optics or optoelectronics, in which the semiconductor layer comprises elastic constraints.

It is said that a layer is strained if the crystalline material which makes it up is tensed or compressed elastically during crystalline growth, such as epitaxy, obliging its lattice parameter to be substantially different to the nominal lattice parameter of this material, the nominal lattice parameter meaning the lattice parameter of the material in its bulk and monocrystalline form, and at equilibrium.

Inversely, any layer where the crystalline material which constitutes it has a lattice parameter substantially identical to its nominal lattice parameter is called a 'relaxed' layer.

The invention further relates to a process for producing an SeOI structure in which the semiconductor

layer comprises elastic constraints.

During a first step of the process, a strained film is formed on a wafer, the strained layer being made of a material selected from amongst semiconductor materials.

During a second step, a layer of SiO_2 is formed on the strained film and/or on the surface of a substrate.

During a third step, the strained film is transferred to the substrate to form an SeOI structure whose semiconductor part is constituted by the strained film and whose electrically insulating part is constituted by the SiO_2 layer.

Such a strained semiconductor layer in an SeOI structure can be advantageous to exploit for physical and/or electrical properties which it can exhibit.

Therefore, for example, the main interest of the strained silicon (or Si) layers mainly comprises the fact that they have average mobility of charged particles (such as holes and electrons) more important than that usually found in layers of relaxed Si.

The layers of strained Si can attain mobility of charged particles 100% more significant than that present in layers of relaxed Si.

In the document WO 01/99162, which discloses formation of a layer of strained Si in accordance with this latter general process, it is proposed to transfer the strained film by bonding the wafer to the substrate, then by removing the wafer by etching the latter selectively 'at the back' (otherwise known as 'etch-back' technique), finally producing an SOI structure (acronym for Silicon-On-Insulator) wherein the semiconductor part is the layer of

strained Si.

Alternatively, and always when producing an SOI structure with strained Si, a Smart-Cut® technique, familiar to the expert (and described in particular in the document entitled 'Silicon-On-Insulator Technology; Materials to VLSI, 2nd Edition' by J.-P. Colinge edited by Kluwer Academic Publishers, p.50 and 51.) is employed during the step of removing the wafer in place of said etch-back technique. This process is described in particular in the document entitled 'Preparation of novel SiGe - free strained Si on insulator' by T.A. Langdo et al. (Proceedings of the 2002 IEEE International SOI Conference' Williamsburg/Virginia (USA), page 211).

The applications of such SeOI structures, and more particularly SOI structures, most often concern manufacturing electronic, optical or optoelectronic components, such as transistors or diodes, in strained semiconductor layers.

These embodiments of components often require thermal treatments at raised temperatures.

The elastic constraints in the semiconductor part of an SeOI structure must therefore resist to this thermal treatment likely to cause significant relaxation of the constraints (which would have an effect contrary to the desired effect).

An SeOI structure such as described hereinabove substantially relaxes the elastic constraints in its semiconductor part from a certain temperature, which can be of the order of 950°C to 1000°C or more in the case of said strained SOI structure.

Evident here is a real problem concerning the behaviour of the elastic constraints in the semiconductor part of an SeOI structure when the latter is subjected to a temperature greater than a threshold temperature.

The processes of manufacturing components in the strained semiconductor parts of SeOI structures are thus limited to temperatures lower than this threshold temperature for fear of losing the desired properties, such as electrical or electronic properties, offered by the elastic constraints in such an SeOI structure.

And the varieties of components which can be embodied in strained layers of an SeOI structure thus risk being restrained.

The present invention endeavours to overcome this difficulty by proposing according to a first aspect a semiconductor on insulator structure, comprising a part made of semiconductor material and a part made of electrically insulating material, solid with one another, elastic constraints being in the part of semiconductor material, wherein the part of electrically insulating material has a viscosity temperature TG greater than the viscosity temperature T_{GSIO2} of SiO_2.

Other characteristics of the semiconductor-on-insulator structure are:

- the viscosity temperature T_{GSIO2} of SiO_2 is greater than approximately 1100°C,
- the electrically insulating part is made of Si_3N_4, $Si_xGe_yN_z$ or SiO_yN_z,
- the electrically insulating part comprises Si_3N_4, $Si_xGe_yN_z$ or SiO_yN_z,

- the part in semiconductor material is a film of strained material,
- the part in semiconductor material comprises a film of strained material,
- the strained material is made of $Si_{1-y}Ge_y$, with y value between 0 and 1,
- the part in semiconductor material also comprises a layer of relaxed or pseudo-relaxed material,
- the layer in relaxed or pseudo-relaxed semiconductor material is located between the film of strained material and the electrically insulating part,
- the layer in semiconductor material of relaxed or pseudo-relaxed material is located on the side opposite the electrically insulating part relative to the film of strained material,
- the part in semiconductor material also comprises two layers each made of relaxed or pseudo-relaxed material, one of these two layers being located between the film of strained material and the electrically insulating part, and the other of these two layers being located on the side opposite the electrically insulating part relative to the layer of strained material,
- the relaxed or pseudo-relaxed material is made of $Si_{1-x}Ge_x$,
- the part in semiconductor material is constituted successively from the electrically insulating part:
  - by a layer of strained $Si_{1-y}Ge_y$;
  - by a layer of relaxed or pseudo-relaxed $Si_{1-x}Ge_x$,
- the part in semiconductor material is constituted successively from the electrically insulating part:

- by a layer of relaxed or pseudo-relaxed $Si_{1-z}Ge_z$;
- by a layer of strained $Si_{1-y}Ge_y$,
- the part made of semiconductor material is constituted successively by the electrically insulating part:
  - by a layer of relaxed or pseudo-relaxed $Si_{1-z}Ge_z$;
  - by a layer of strained $Si_{1-y}Ge_y$;
  - by a layer of relaxed or pseudo-relaxed $Si_{1-x}Ge_x$.

According to a second aspect, the invention proposes a process for realising a semiconductor-on-insulator structure as per the foregoing claims, from a donor wafer comprising an upper layer of crystalline material having a first lattice parameter, wherein comprising the following steps:

(a) growth on the upper layer of the donor wafer of a film made of material selected from semiconductor materials having a nominal lattice parameter substantially different to the first lattice parameter, over a sufficiently minimal thickness to be essentially constrained elastically;

(b) formation of at least one layer of electrically insulating material and having a viscosity temperature T_G greater than the viscosity temperature T_{GSiO2} of SiO_2 on the surface of the donor wafer on the side where the strained layer has been formed and/or on a surface of the receptor substrate;

(c) bonding the receptor substrate to the donor wafer at the insulating layer(s);

(d) removing at least a part of the donor wafer.

Other characteristics of the manufacturing process of a semiconductor-on-insulator structure are:

- it further comprises, between step (a) and step (b), an additional growth step of a relaxed or pseudo-relaxed layer, made of material selected from semiconductor materials, on the strained film,
- the electrically insulating layer is formed during step (b) by nitriding of the surface(s),
- the electrically insulating layer is deposited on at least one surface to be bond,
- the insulating layer formed during step (b) is constituted by Si_3N_4, $Si_xGe_yN_z$ or SIO_yN_z,
- step (d) relates to removal of a part of the donor wafer, with the part of the donor wafer transferred to the receptor substrate after removal being at least a part of the upper layer of crystalline material,
- it comprises:
  - an additional step implemented before step (c) consisting of implanting atomic samples in the donor wafer at a preset depth effectively creating an embrittlement zone in the vicinity of the implant depth; and wherein
  - step (d) comprises an energy contribution such as to cause detachment at the level of the embrittlement zone present in the donor wafer,
- it also comprises, before step (a), a step of formation of the donor wafer comprising:
  - formation of a porous layer on a crystalline support substrate;
  - growth of a crystalline layer on the porous layer;

- the support substrate - porous layer - crystalline layer ensemble constituting the donor wafer, the porous layer constituting an embrittlement zone in the donor wafer;

and wherein step (d) comprises an energy contribution such as to cause detachment at the level of the embrittlement zone present in the donor wafer,

- step (d) comprises a finishing step of the surface of the part of donor wafer transferred to the receptor substrate,

- step (d) also relates to removal of the part of the donor wafer transferred to the receptor substrate, such as to remove all the donor wafer,

- removal of the part of the donor wafer remaining on the film during step (d) is done by selective chemical etching vis-à-vis the strained material of the film.

Other aspects, aims and advantages of the present invention will emerge more clearly from the following detailed description of implementation of the preferred processes of the latter, given by way of non-limiting example and done with reference to the accompanying drawings, in which:

Figure 1 illustrates the different steps of a first process for realising an electronic structure comprising a thin layer of strained silicon according to the present invention.

Figure 2 illustrates the different steps of a second process for realising an electronic structure comprising a thin layer of strained silicon according to the present invention.

Figure 3 illustrates the different steps of a third process for realising an electronic structure comprising a thin layer of strained silicon according to the present invention.

Figure 4 illustrates the different steps of a fourth process for realising an electronic structure comprising a thin layer of strained silicon according to the present invention.

A first object of the present invention consists of forming a film of strained semiconductor material on a substrate.

A second object of the invention is implementing a reliable process for transferring a film of strained material of a donor wafer to a receptor substrate, the whole forming a desired electronic structure, without relaxation of the constraint inside the film during transfer.

A third object of the invention, in terms of implementing the transfer process of the strained film, to realise an SeOI structure whereof the semiconductor part comprises elastic constraints, and to conserve the behaviour of these constraints during thermal treatment at high temperature.

In a particular case, this means to be able to conceive the behaviour of the constraints at least relatively of a layer of strained Si of a SeOI structure, during thermal treatment at temperatures greater than around 950°C to 1000°C.

Such thermal treatment can be employed during processing carried out after or during formation of the

strained film, such as for example realisation of components in the film.

In the non-limiting examples of the processes according to the present invention which will be touched on, whereof the main steps are described with reference to Figures 1 to 4, case studies will be presented where the strained film 2 to be transferred to realise the SeOI structure according to the present invention is made of strained Si.

Figures 1a to 1d illustrate the steps of a first of these processes according to the present invention.

With reference to Figure 1a, this is based on a donor wafer 1 whose function is to be a substrate to the growth of the strained film 2 (with reference to Figure 1b).

The donor wafer 1 is a 'pseudo-substrate' comprising a support substrate 1A made of monocrystalline Si and a buffer structure 1B which is interfaced with the strained film 2.

Buffer structure 1B designates any structure behaving in the manner of a buffer layer.

Buffer layer generally designates a transition layer between a first crystalline structure such as the support substrate 1A and a second crystalline structure such as the film 2, whose first function is modification of properties of the material, such as structural or stoichiometric properties, or surface atomic recombination.

In a particular case of buffer layer, the latter can produce a second crystalline structure whose lattice parameter differs substantially from that of the support substrate 1A.

Advantageously, the buffer structure 1B presents on its surface a substantially relaxed crystallographic structure and/or without a notable number of structural defects.

Advantageously, the buffer layer has at least one of the two following functions:

- decreasing the density of defects in the upper layer;
- adaptation of a lattice parameter between two crystallographic structures of different lattice parameters.

To execute the second function the buffer layer has in the region of one of its faces a first lattice parameter substantially identical to that of the support substrate 1A and in the region of its other face a second lattice parameter.

The buffer layer in the buffer structure 1B presents on its surface a lattice parameter substantially different to the lattice parameter of the support substrate 1A, and thus can have in the same donor wafer 1 a layer having a lattice parameter different to that of the support substrate 1A.

In certain applications the buffer layer can also allow the overlying layer to not contain an accumulation of defects and/or undergo noticeable constraints.

According to a first technique for realising a buffer structure 1B, a buffer layer is formed so as to have a lattice parameter overall being modified progressively on an ensuing thickness to establish the transition between the two lattice parameters.

Such a layer is generally called a metamorphic layer.

Such a buffer layer is advantageously made of SiGe with preferably a concentration of Ge progressively growing from the interface with the support substrate 1A.

The thickness is typically between 1 and 3 micrometers, for surface concentrations of Ge of less than 30%, to produce good structural surface looseness, and to confine defects associated with the difference in lattice parameter such that they are embedded.

Optionally, growth of an additional layer, in SiGe having a constant Ge composition, follows or precedes formation of the buffer layer, the whole forming said buffer structure 1B.

The additional layer is in SiGe substantially relaxed by the buffer layer, with an advantageously uniform Ge concentration and substantially identical to that of the buffer layer in the vicinity of their interface.

The concentration of germanium in the silicon inside the layer of relaxed SiGe is typically between 15% and 30%.

This 30% limitation represents a limitation typical of current techniques, but it can be adjusted to evolve in coming years.

The additional layer has a thickness varying widely, according to case, with a typical thickness between 0.5 and 1 micron.

According to a second technique for realising the buffer structure 1B, this is based on a technique for depositing a superficial layer on a support substrate 1A, said superficial layer having a nominal lattice parameter substantially different to the lattice parameter of the

adjacent surface material of the support substrate 1A.

Nominal lattice parameter is here referred to the lattice parameter of a material in the solid, monocrystalline and balanced form.

This superficial layer is deposited so that the deposited layer is practically exempt from plastic defects, such as dislocations.

This superficial layer is made so as to finally give:

- a first part in contact with the support substrate 1A, which confines plastic defects, such as dislocations; and
- a second part, relaxed or pseudo-relaxed by the first part, and having no or few plastic defects.

The first part of the deposited superficial layer thus plays the role of a buffer layer.

The depositing technique employed to realise such a buffer layer can comprise variations in time of temperatures and chemical deposit compositions.

A buffer layer having a chemical composition substantially constant in its thickness can be successfully produced, as opposed to a buffer layer created according to the first technique.

One or several layers can however be intercalated between the buffer layer of the second part of the superficial layer.

The buffer layer can also have a thickness less than lower thickness of the buffer layers produced according to the first technique.

The document WO 00/15885 discloses an embodiment of such a buffer structure according to the latter technique

comprising in particular the following steps:

- deposit on a support substrate 1A of Si of a first Ge or SiGe layer,
- then, optionally, deposit of a second additional layer, able to improve the crystallographic quality of the overlaying film 2, such as described in WO 00/15885, the second layer being in:
  - SiGe (50/50) in the case where the first layer of the buffer layer is in Ge;
  - strained Si in the case where the first layer of the buffer layer is in SiGe.

The thickness of this buffer structure 1B can in particular be of the order of 0.5 to 1 micron, which is less than the thickness of a buffer layer made according to the first technique.

The donor wafer 1 has been produced in this manner, with the donor wafer 1 comprising said support substrate 1A in Si and said buffer structure 1B in Ge or in SiGe.

According to a third production technique for a buffer structure 1B, a first step consists of a depositing a layer 1B of strained SiGe on a support substrate 1A in Si, with the support substrate 1A and possibly the epitaxied layer 1B being included in the donor wafer 1.

A second step consists of implanting atomic samples, such as hydrogen and/or helium, having an implantation energy and a sample dosage determined such as to form a perturbation zone in the thickness between the depth of implant and the strained layer.

A perturbation zone is defined as a zone having internal constraints susceptible of forming structural

perturbations in the surrounding parts.

These internal constraints are then susceptible to creating crystallographic perturbations in the overlying strained layer.

During the first step the ranges of implant energy of H or He are typically between 12 and 25 keV.

The implanted doses of H or He are typically between 10^{14} and 10^{17} cm^{-2}.

- Therefore, for example, H will preferably be used for the implant dosed at around 3.10^{16} cm^{-2} with an energy around 25 keV for a strained layer 1B at 15% Ge.

- Therefore, for example, H will preferably be used for the implant dosed at around 2.10^{16} cm^{-2} with an energy around 18 keV for a strained layer 1B at 30% Ge.

The depths of implant of the atomic samples in the donor wafer 1 are typically between approximately 50 nm and 100 nm.

To create or accentuate the perturbations of the perturbation zone, the buffer layer is produced according to this third technique during implementation of a third step by a thermal energy contribution adapted and conveniently parametered to cause at least relative relaxation of elastic constraints of the layer 1B in strained SiGe so as to form a relaxed strained layer in SiGe.

The thermal treatment is preferably utilised in an inert or oxidising atmosphere.

Therefore, a particular thermal treatment to be used for this type of donor wafer 1 is carried out at temperatures typically between 400°C and 1000°C over a

period which can vary from 30 s to 60 minutes, and more particularly of approximately 5 minutes to approximately 15 minutes.

Therefore, the perturbation zone:

- confines defects of dislocation type; and
- adapts the lattice parameter of the support substrate 1A in Si to the nominal lattice parameter of the strained layer 1B in SiGe.

It can therefore be considered here as a buffer layer.

A variant to this technique consists of forming the film in Si 2 on layer 1B of strained SiGe prior to implantation of the samples.

Implantation then thermal treatment will then relax or pseudo-relax the layer of strained SiGe (as described hereinabove) and constrain the film 2.

In this case, formation of the buffer layer and formation of the constraint in the film 2 are closely associated.

For more precision, reference can be made to B. Hollander et al., in particular in the document entitled 'Strain relaxation of pseudomorphic $Si_{1-x}Ge_x$ / Si(100) heterostructures after hydrogen or helium ion implantation for virtual substrate fabrication' (in Nuclear and Instruments and Methods, in Physics Research B 175-177 (2001) 357 -367).

Irrespective of the structural configuration of the donor wafer 1 in this application of the process according to the invention, the latter is constituted at the level of the interface with the strained film 2 of a material made of crystalline $Si_{1-x}Ge_x$ having little or no crystallographic

defects.

The donor wafer 1 comprises an upper layer which has a thickness which is sufficient to impose its lattice parameter on the strained film 2 which will be overlying, without the latter substantially influencing the crystalline structure of the upper layer of the donor wafer 1.

A light finishing step for the surface of the donor wafer 1 is advantageously performed to improve the surface quality, by means of surface finishing techniques such as polishing, chemical etching, abrasion, mechanical-chemical planarising (CMP), sacrificial oxidation, bombardment of atomic samples, or other smoothing techniques.

With reference to Figure 1b, growth of a film 2 in Si is used on the $Si_{1-x}Ge_x$ growth substrate of the donor wafer 1.

The Si film 2 is advantageously formed by epitaxy from using known techniques such as CVD and MBE techniques (respective abbreviations of Chemical Vapor Deposition and Molecular Beam Epitaxy).

Since the silicon has a lattice parameter different to that of the germanium, the film 2 is obliged by the growth $Si_{1-x}Ge_x$ to augment its nominal lattice parameter to appear substantially identical to that of its growth substrate and thus present internal tension constraints.

These modifications to its internal crystallographic structure will boost mobility of the charged particles (such as the holes and electrons) by modifying the structure of the energy bands of the silicon crystal.

The desired electric properties for this film 2 in

this invention are thus obtained.

For a layer to be elastically strained, its thickness must not surpass a critical thickness of elastic constraint

Beyond the critical thickness, plastic constraints and elastic relaxations can appear in the film 2, which would substantially deteriorate its electrical properties.

The critical thickness of elastic constraints depends mainly on the material selected to make up the strained layer and on the difference of the lattice parameter with the material of the crystalline structure on which it has been formed.

Therefore, since silicon has a lattice parameter of approximately 4.2% less than that of the germanium, the disaccord in lattice between the silicon of the film 2 and the $Si_{1-x}Ge_x$ growth support is such that it implies a critical thickness of the film 2 of between approximately 100 Å and 2000 Å, depending on the value of x.

For example, if $x = 0.2$, then the strained Si film 2 is typically of the order of 200 Å approximately.

The critical thickness may also depend on growth parameters such as the temperature at which the film 2 was formed, nucleation sites from which it was epitaxied, or growth techniques employed (for example CVD or MBE).

Values of critical thickness of a Si film 2 epitaxied on a $Si_{1-x}Ge_x$ growth substrate are for example presented in the document entitled 'High-mobility Si and Ge structures' by Friedrich Schaffler (Semiconductor Science Technology, 12 (1997) 1515-1549).

The thickness of the strained Si film 2 is thus typically a few hundred angstroms, preferably between 100

and 500 Å.

Once it is formed, the film 2 thus has a lattice parameter substantially close to that of the $Si_{1-x}Ge_x$ and presents elastic constraints in tension.

The donor wafer 1 and film 2 ensemble form a pre-bonding wafer 10.

With reference to Figure 1c, the pre-bonding wafer 10 with a receptor substrate 4 is put into use.

Prior to such bonding, at least one insulating layer 3 made of an electrically insulating material is formed on the surface of the pre-bonding wafer 10 and/or on the surface of the receptor substrate 4.

The material selected for an insulating layer 3 is a material having a viscosity temperature T_G greater than the viscosity temperature T_{GSiO2} of the SiO_2.

The value of T_{GsiO2} of the SiO_2 can vary substantially according to certain criteria, such as:

- the production technique employed to produce the layer of SiO_2, if the layer is produced by thermal oxidation (whether in a dry or humid atmosphere, associated or not with the use of chemical samples), T_{GsiO2} is of the order of approximately 1100°C to approximately 1150°C, while in the case of a layer formed by depositing SiO_2, this T_{GsiO2} is in general less;
- the parameters for producing the SeOI structure, such as the energy for activating the surfaces to be stuck affected prior to bonding,
- structural parameters, such as the charge coefficient of constraints presented by film 2.

The viscosity temperature T_{GsiO2} of the SiO_2 can thus

reach as much as 1100°C to 1150°C.

If the viscosity temperature T_G is a theoretical thermal limit beyond which the elastic constraints seem to relax to a large extent, initial relaxations of constraints can appear before T_G at temperatures less than T_G (typically less, to approximately 100°C to 200°C), the percentage of relaxation being nevertheless more and more important as T_G is approached.

The function of an insulating layer 3 is principally double:

- to electrically insulate the receptor substrate 4 of the film 2, especially in the final SeOI structure 20 (see Figure 1d);
- to keep the elastic constraints in the film 2 at high temperatures (greater than approximately 950°C to 1000°C).

This insulating layer 3 can also have particularly significant adhesive properties to be exploited during the bonding step.

The insulating layer 3 can be formed by direct deposit on the surface in question or by chemical reaction between atomic samples of the surface in question with gaseous samples in a controlled atmosphere.

In a first advantageous case according to the invention, the material of the insulating layer 3 is made of Si_3N_4.

A layer of Si_3N_4 thus has a temperature T_G which is greater than around 1500°C.

The insulating layer of Si_3N_4 can be formed by nitriding with the silicon of the film 2 and/or with the

silicon of the receptor substrate 4 (if the latter contains any on the surface), or by depositing a nitride layer by a CVD technique on the surface in question.

It should be noted that the Si_3N_4 has bonding properties almost equivalent the bonding properties of the SiO_2 in terms of bonding energy and transfer quality, in particular in the case of utilising a Smart-Cut® process, with reference for example to the document entitled 'From SOI to SOIM Technology: application for specific semiconductor processes' by O. Rayssac et al. (in SOI Technology and Devices X, PV 01-03 ecs Proceedings, Pedington, and J (2001)).

In a second advantageous case according to the present invention, the material of the insulating layer 3 is SiO_yN_z.

During formation of an insulating layer 3 of SiO_yN_z the value of z can be played on advantageously, to have the viscosity temperature T_G evolve which for this material is substantially a function of this nitrogen composition.

Therefore, with a growing composition z, it is possible to have the T_G of the insulating layer 3 evolve typically between a T_G of the order of that of the SiO_2 (which may vary around 1100°C) and a T_G of the order of that of the Si_3N_4.

By playing on y, a wide range of T_G can be covered.

The values T_G of the insulating layer 3, if they depend essentially on the material of the vitreous layer, can also fluctuate according to the conditions by which it was formed.

In an advantageous case, the conditions for forming the insulating layer 3 can be adapted in a controlled

manner so as to select a T_G "à la carte" greater than T_{Gsio2}.

The deposit parameters can thus be played on, such as temperature, time, dosage and potential of the gaseous atmosphere, etc.

Doping elements can also be added to the main gaseous elements contained in the vitrification atmosphere, such as boron and phosphorous which can have the effect of reducing the T_G.

After one or more insulating layers 3 are formed on one or two surfaces to be bonded, a finishing step is advantageously implemented on the two surfaces to be stick, before the bonding step, for example by means of one of said finishing techniques, in order to smooth the surfaces for bonding as much as possible.

Bonding consists of putting the bonding surfaces of the pre-bonding wafer 10 and le receptor substrate 4 in contact.

The bonding operation per se is carried out by contacting the surfaces to be bonded together.

The bonding bonds are preferably molecular in nature by using hydrophilic properties of the surfaces to be bond.

To attribute or accentuate the hydrophilic properties of the surfaces to be bond, chemical cleaning of the two structures for bonding can be done in baths, comprising SC1 treatment well-known to the expert.

Annealing of the bonded assembly can also be utilised to reinforce the bonding bonds, for example by modifying the nature of the bonding bonds, such as covalence bonds or other bonds.

For greater precision in terms of bonding techniques, reference can be made in particular to the document entitled 'Semiconductor Wafer Bonding' (Science and technology, lnterscience Technology) by Q. Y. Tong, U. Gösele and Wiley.

Figure 1d illustrates the SeOI structure obtained after the donor wafer 1 is removed.

According to a first method of realising removal of the donor wafer 1, all or part of the donor wafer 1 is detached at an embrittlement zone previously formed in the donor wafer 1, via power supply.

This embrittlement zone is substantially parallel to the bonding surface, and presents bond fragility between the part above it and below it, these fragile bonds being capable of being broken during power supply, such as thermal and/or mechanical power.

According to a first technique a technique called Smart-Cut® is used to execute the embrittlement zone, comprising in the first instance implantation of atomic samples in the donor wafer 1, at the embrittlement zone.

The implanted samples can be hydrogen, helium, a mixture of these two samples or other light samples.

Implantation preferably takes place just before bonding.

The implantation power is selected such that the samples, implanted via the surface of the insulating layer 3 (in the event where it is formed on the donor wafer 1), pass through the thickness of the insulating layer 3, the thickness of the strained film 2 and a preset thickness of the upper part of the donor wafer 1.

It is preferable to implant in the donor wafer 1 sufficiently deeply so that the strained film 2 does not suffer damages during the step of detaching the donor wafer 1.

The depth of implant in the donor wafer 1 is typically 1000 Å approximately and more.

The brittleness of the bonds in the embrittlement zone is found mainly by selecting the dosage of the implanted samples, with the dosage being typically between 10^{16} cm^{-2} and 10^{17} cm^{-2}, and more precisely between approximately 2.10^{16} cm^{-2} and approximately 7.10^{16} cm^{-2}.

Detachment at this embrittlement zone is usually effected by mechanical and/or thermal power supply.

For greater precision for the Smart-Cut® process, reference can be made to the document entitled 'Silicon-On-Insulator Technology': Materials to VLSI, 2nd Edition by J.-P. Colinge, edited by Kluwer Academic Publishers, p.50 to 51.

In accordance with a second mode of execution of the embrittlement zone, a technique described in particular in the document EP 0 849 788 is used.

The embrittlement zone is here created before formation of the film 2, and during formation of the donor wafer 1.

Producing the embrittlement zone comprises the following main operations:

- formation of a porous layer on a substrate;
- growth of one or more layer(s) on the porous layer.

The substrate - porous layer - layer(s) ensemble constitutes the donor wafer 1, and the porous layer

constitutes the embrittlement zone of the donor wafer 1.

Power supply, such as thermal and/or mechanical power supply, at the porous embrittlement zone, then results in detachment of the support substrate 1A of the overlying layer(s) on the porous layer.

The preferred technique according to the present invention for removing material at the embrittlement zone, realised according to one of the two of non-limiting production hereinabove, therefore allows a significant part of the donor wafer 1 to be withdrawn rapidly and en bloc.

It also allows the withdrawn part of the donor wafer 1 to be reused in another process, such as for example a process according to the present invention.

Therefore, reformation of a strained film on the withdrawn part and a possible other part of a donor wafer and/or other layers can be implemented, preferably after polishing the surface of the withdrawn part.

A surface finishing step allows the remaining part of the $Si_{1-x}Ge_x$ donor wafer to be withdrawn 1, with the latter able to be reduced by different finishing techniques such as CMP polishing, abrasion, thermal RTA annealing, sacrificial oxidation, chemical etching, either singly or in combination.

In an advantageous manner removing the finishing material utilises at least at the end of the step selective chemical etching, in combination or not with mechanical means.

Therefore selective etching solutions of the SiGe vis-à-vis the Si such as a solution comprising $HF:H_2O_2:CH_3COOH$ (selectivity of around 1:1000) can be used to withdraw the

remaining part of the $Si_{1-x}Ge_x$.

The film 2 has a crystalline structure and properties of homogeneity in thickness close to those it had after growth on the donor wafer 1.

After the bonding step, a second technique for removing material without detachment and without embrittlement zone can be used according to the present invention to remove the donor substrate 1.

It consists of implementing chemical and/or mechanical and/or mechanical-chemical etching.

For example, optionally selective etching of the materials of the donor wafer 1 to be removed can be utilised, according to a process of the etch-back type.

This technique consists of etching the donor substrate 1 from behind, that is, from the free face of the donor wafer 1.

Wet etching employing etching solutions adapted to the materials to be removed can also be used.

Dry etching can also be used to remove material, such as plasma etching or pulverisation etching.

The etching can also be purely chemical or electrochemical or photoelectrochemical.

The etching can be preceded or followed by mechanical attack of the donor wafer 1, such as lapping, polishing, mechanical or pulverisation etching of atomic samples.

The etching can also be accompanied by mechanical attack, such as polishing optionally combined with a mechanical abrasive action in a CMP process.

All the abovementioned techniques for removing material from the donor wafer 1 are proposed by way of

example in the present document, but they do not constitute a limitation, because the invention extends to all types of techniques capable of removing of material from the donor wafer 1 as per the process according to the invention.

With reference to Figure 1d, an SOI structure 20 is obtained whereof the semiconductor part (that is, the film 2) is made of strained Si, and in the insulating part (that is, the insulating layer 3) at a viscosity temperature T_G greater than T_{GSiO2} such as for example Si_3N_4 or SiO_YN_Z.

The 20 SOI structure permits thermal treatment greater than 950°C to 1000°C, such as certain treatments to be utilised for producing constituents in the film 2, without its semiconductor part in strained material undergoing significant elastic relaxation, as is the case for SOI structures having an insulating part in SiO_2.

A second process according to the present invention is presented with reference to Figures 2a to 2d.

This process is overall the same as that described with reference to Figures 1a to 1d, with the exception of the step of removing the donor wafer 1.

Indeed, removing material from the donor wafer 1 here relates to not the whole donor wafer 1 but only a part of the donor wafer 1, with the other part of the donor wafer 1 forming an upper layer 5 on the structure 20 (with reference to Figure 2d).

The techniques for removing material are substantially the same as those disclosed hereinabove (with reference to Figure 1d).

They are however utilised so as to conserve this upper layer 5, and so that the latter is constituted by at least

a patio of the buffer structure 1B.

This process according to the invention is advantageously used for a buffer structure 1B produced according to said first technique or said second technique for producing a buffer structure 1B.

This process according to the invention is particularly advantageous if one or the other of the two types of buffer structure (the two types of buffer structure being associated respectively to the two production techniques) comprises in its upper part a layer of $Si_{1-x}Ge_x$ having a composition which is substantially constant without too many crystallographic defects. In this case, utilising techniques for removing material is parametered such that the upper layer 5 comprises at least in part the latter $Si_{1-x}Ge_x$ layer. The result is therefore a structure 20 comprising an upper layer 5 of quality $Si_{1-x}Ge_x$.

After removal of material, a surface finishing step is advantageously used to withdraw surface roughness and unevenness in thickness of the upper layer 5 of $Si_{1-x}Ge_x$, for example by polishing, abrasion, CMP planarising, chemical etching, either singly or in combination.

According to a variant, the donor wafer 1 comprises an etching stop layer located between the upper layer 5 and the rest of the donor wafer 1, effectively terminating the finishing step by selective etching at this stop layer, and obtaining an upper layer 5 which is particularly homogeneous in thickness and with a smooth surface.

With reference to Figure 1d, the final result is a $Si_{1-x}Ge_x$ / SOI structure 20 whereof the semiconductor part (that

is, the upper Ia layer 5 and the film 2) comprises strained Si, and whereof the insulating part (that is, the insulating layer 3) has a viscosity temperature T_G greater than T_{GSiO2}, such as for example Si_3N_4 or SiO_YN_Z.

The structure 20 thus allows thermal treatment greater than 950°C to 1000°C, without losing too many constraints in the film 2.

In a particular case where thermal treatment is done at a temperature and for a period greater than a temperature and a reference period from which the Ge diffuses in the Si, the Ge contained in the upper layer 5 can diffuse in the film 2.

In certain other cases this diffusion effect, if well controlled, can be desired.

In fact, diffusion can be controlled such that the samples of Ge are distributed uniformly in the entirety of the two layers 2 and 5, forming a single layer of SiGe having a substantially uniform Ge concentration.

There is in particular a discussion of the latter point in the document US 5 461 243, column 3, lines 48 to 58.

A third process according to the invention is presented with reference to Figures 3a to 3e.

This process is overall the same as that described with reference to Figures 1a to 1d, with the exception that it comprises an additional step of crystalline growth of an additional layer 6 used with reference to Figure 3c.

This additional layer 6 is epitaxied, for example by a CVD or MBE technique, on the film 2 of strained Si.

The material it is constituted by can be any type of

material.

However, this material is preferably made of $Si_{1-x}Ge_x$ with a composition z substantially identical to the composition x of $Si_{1-x}Ge_x$ present on the surface of the buffer structure 1B, such that the additional layer 6 is relaxed or pseudo-relaxed.

After the growth of the additional layer 6, the insulating layer 3 is formed at the level of the additional layer 6 and/or on the surface of the receptor substrate 4.

In the event where formation of the insulating layer 3 takes place at the surface of the additional layer 6, it can be produced by direct deposit, or by chemical reaction between atomic samples and the material constituting the surface of the additional layer 6, with gaseous samples in a controlled atmosphere.

An insulating layer of $Si_xGe_yN_z$ can be formed by nitration with the silicon - germanium of the additional layer 6 in $Si_{1-z}Ge_z$.

The bonding steps (with reference to Figure 3d) and removal of material (Figure 3e) are then typically identical to those designated by 1c and 1d.

With reference to Figure 3e, the final result is a strained/SGOI Si structure 20 whereof the semiconductor part (that is, the film 2 and the additional layer 6) comprises strained Si, and whereof the insulating part (that is, the insulating layer 3) has a viscosity temperature T_G greater than SiO2 such as for example be $Si_xGe_yN_z$.

The structure 20 then allows thermal treatment greater than 950°C to 1000°C to be undertaken, without losing too

many constraints in the film 2.

In a particular case where thermal treatment is effected at a temperature and for a period greater than a temperature and reference period from which the Ge diffuses in the Si, the Ge contained in the additional layer 6 can diffuse in the film 2.

In certain other cases, this diffusion effect, if well controlled, can be desired.

Indeed, diffusion can be controlled such that the samples of Ge are distributed uniformly in the entirety of the two layers 2 and 6 forming a single layer of SiGe having a Ge concentration which is substantially uniform.

In particular, a discussion on this latter point is found in the document US 5 461 243, column 3, lines 48 to 58.

With reference to Figures 4a to 4e, and more particularly to Figures 4c and 4e, a fourth process according to the present invention is overall the same as that described with reference to Figures 1a to 1d, with the exception:

- removing the material from the donor wafer 1 here relates to not the whole donor wafer 1, but only a part of the donor wafer 1, leaving an upper layer 5 in the upper part of the final structure 20 (with reference to Figure 4e);
- it comprises an additional step of crystalline growth of an additional layer 6 which is utilised with reference to Figure 4c.

This process comprises a step identical to that described with reference to Figure 2d, forming an upper

layer 5 (see Figure 4e), and a step identical to that described with reference to Figure 3c, forming an additional layer 6 (see Figure 4e) intercalated between the film 2 and the receptor substrate 4.

The means for forming these two layers 5 and 6, as well as the possibilities of evolving their structure and their effect on the final structure are thus essentially the same as those described in the processes with reference to Figures 2a to 2d and Figures 3a to 3e.

With reference to Figure 4e, the final result is a SiGe / strained Si / SGOI structure 20 whereof the semiconductor part (that is, the film 2 and the additional layer 6) comprises strained Si, and whereof the insulating part (that is, the insulating layer 3) has a viscosity temperature greater than 950°C to 1000°C such as for example $Si_xGe_yN_z$.

The structure 20 can then undertake thermal treatment greater than T_{GSiO2} without losing too many constraints in the film 2.

In a particular case where thermal treatment is effected at a temperature and for a period greater than a temperature and reference period from which the Ge diffuses in the Si, the Ge contained in the additional layer 6 and in the upper layer 5 can diffuse in the film 2.

In certain other cases, this diffusion effect, if well controlled, can be desired.

In effect, diffusion can be controlled such that the samples of Ge are distributed uniformly in the entirety of the three layers 2, 5 and 6 forming a single layer of SiGe having a Ge concentration which is substantially uniform.

In particular, a discussion of the latter point is found in the document US 5 461 243, column 3, lines 48 to 58.

According to one of the four preferred processes according to the present invention hereinabove, and according to an equivalent of the latter, steps for producing the components can be integrated into or succeed this process according to the present invention.

Therefore, preparation steps for the production of components can be implemented during the process, without altering the percentage of constraints in the film 2.

They are used at the level of the strained Si film 2 of the SGOI structure with reference to Figure 1d, the upper layer 5 of relaxed $Si_{1-x}Ge_x$ and/or the film 2 of the SiGe/SOI structure with reference to Figure 2d, the film 2 and/or the additional layer 6 of relaxed $Si_{1-z}Ge_z$ of the strained Si/SGOI structure with reference to Figure 3e, the upper layer 5 of relaxed $Si_{1-x}Ge_x$ and/or the film 2 and/or the additional layer 6 of relaxed $Si_{1-z}Ge_z$ of the SiGe/Si strained SGOI structure with reference to Figure 4e.

Local treatment designed to etch patterns in the layers, for example by lithography, photolithography, reactive-ion etching or by any other etching with pattern masking.

One or more steps for producing components, such as transistors, in the strained Si film 2 (or in the layer of relaxed SiGe 2' in the case where the latter is not covered with a layer of strained Si 11) can in particular be implemented without altering the percentage of constraints of the film 2.

The techniques described in the invention are proposed by way of example in the present document, but they do not constitute a limitation, because the invention extends to all types of techniques capable of using a process according to the invention.

One or more epitaxies can be used on the final structure 20 (with reference to Figures 1d, 2d, 3e, 4e), such as epitaxy of a layer of SiGe or SiGeC, or epitaxy of a layer of Si or strained SiC, or successive epitaxies of SiGe or SiGeC layers and layers of Si or strained SIC alternating to form a multilayer structure. Accordingly, and in particular, a thickening of the film 2 can be attained by epitaxy of Si on the film 2 initially obtained after transfer.

The applicant has also noticed that thickening of a film 2 of strained Si can be made such that its thickness becomes more significant than the standard critical thickness of the Si, without the latter losing elastic constraints.

The standard critical thickness of the Si can be found from the value of the percentage of constraints of the film 2 and from the fact that this percentage of constraints can be associated directly with the concentration of Ge in the $Si_{1-x}Ge_x$ on the pseudo-substrate (i.e. the value x) on which the film 2 was or would be epitaxied (if the percentage of constraints of the film 2 was not modified since formation, the concentration x of associated Ge is that of the pseudo-substrate of $Si_{1-x}Ge_x$ on which the film 2 was epitaxied before being transferred).

The value of the standard critical thickness of the Si

of the film 2 can thus be associated directly with the concentration of Ge of the pseudo-substrate of $Si_{1-x}Ge_x$ on which the film 2 was or would be epitaxied. Examples of standard critical thickness of the Si can be found in particular in 'High-Mobility Si and Ge Structures' by Friedrich Schaffler (Semiconductor Science Technology, 12 (1997) 1515-1549).

Therefore, the applicant has noted that, in a structure comprising a layer of material becoming viscous from a T_G, and a strained Si film 2 on the viscous material, the critical thickness of the film 2 (beyond which the film 2 is no longer mainly elastically strained) is typically more significant than the standard critical thickness of the Si.

Therefore, experience has shown that it is possible to increase the thickness of the film 2 by approximately 60 nanometres, without there being substantial loss of elastic constraints intrinsic to the film 2.

The thick film 2 can thus be used as an active layer (taking advantage of the considerable mobility of electrons exhibited by such a material).

Once the final structure is achieved, with or without thickening, finishing treatment can be put into practice, comprising annealing, for example. The present invention is not just limited to a strained Si film 2, but also extends to alloys $Si_{1-y}Ge_y$ including between 0 and 1, capable of being strained by a growth support of $Si_{1-x}Ge_x$ (on the surface of the donor wafer 1) when $x \neq y$.

Therefore, in a first particular application, the donor wafer 1 would be a solid substrate of Si on which a

film 2 of strained $Si_{1-x}Ge_x$ would be grown (by the solid substrate). Since transfer to form a final semiconductor-on-insulator structure is thus identical to the process according to the present invention described hereinabove, formation of the embrittlement zone 3 is done in the solid substrate.

In a second particular application, the donor wafer 1 would be a solid substrate of $Si_{1-x}Ge_x$, including between approximately 0.7 and 1, on which a Si film 2 or $Si_{1-x}Ge_x$ film would be grown, with these materials being strained by the solid substrate. Since transfer to form a final semiconductor-on-insulator structure is identical to the process according to the present invention described hereinabove, formation of the embrittlement zone 3 is done in the solid substrate.

In a third particular application, a buffer structure 1B of $Si_{1-z}Ge_z$ (with z diminishing gradually in thickness) is intercalated between the solid substrate 1A of $Si_{1-y}Ge_y$ ($y \in [0 \neq 1]$) and the film 2 (in strained Si or strained $Si_{1-x}Ge_x$) in order to find the constraint coefficient of the desired film 2.

In general, the strained film 2 can be in other types of material, such as alloys of type III-V or II-VI, or in other semiconductor materials capable of being used by a process according to the present invention and being in a semiconductor-on-insulator structure according to the present invention.

For example, the film 2 can be made of a nitride material, such as an alloy (Al, Ga, In) - (N), which has been initially formed on a donor wafer 1 constituted by a

solid substrate or a pseudo-substrate in sapphire or SiC.

In the layers of semiconductors discussed in this document, other constituents can be added, such as carbon at a concentration of carbon in the layer considered substantially less than or equal to 50% or, more particularly, at a concentration less than or equal to 5%.

CLAIMS

1. Semiconductor-on-insulator structure, comprising a part made of semiconductor material and a part of electrically insulating material, solid with one another, elastic constraints being in the part of semiconductor material, wherein the part of electrically insulating material presents a viscosity temperature T_G greater than the viscosity temperature T_{GSiO2} of the SiO_2.

2. The semiconductor-on-insulator structure as claimed in the preceding claim, wherein the viscosity temperature T_{GSiO2} of the SiO_2 is greater than approximately 1100°C.

3. The semiconductor-on-insulator structure as claimed in either of the two preceding claims, wherein the electrically insulating part is made of Si_3N_4, $Si_xGe_yN_z$ or SiO_yN_z.

4. The semiconductor-on-insulator structure as claimed in either of Claims 1 to 2, wherein the electrically insulating part comprises Si_3N_4, $Si_xGe_yN_z$ or SiO_yN_z.

5. The semiconductor-on-insulator structure as claimed in any one of the preceding claims, wherein the part of semiconductor material is a film of strained material.

6. The semiconductor-on-insulator structure as claimed in any one of Claims 1 to 4, wherein the semiconductor material part comprises a film made of strained material.

7. The semiconductor-on-insulator structure as claimed in any one of the two preceding claims, wherein the strained material is made of $Si_{1-y}Ge_y$, with y value between 0 and 1.

8. The semiconductor-on-insulator structure as claimed

in Claim 6, wherein semiconductor material part further comprises a layer of relaxed or pseudo-relaxed material.

9. The semiconductor-on-insulator structure as claimed in the preceding claim, wherein the layer of relaxed or pseudo-relaxed semiconductor material is located between the film of strained material and the electrically insulating part.

10. The semiconductor-on-insulator structure as claimed in Claim 8, wherein the layer of relaxed or pseudo-relaxed semiconductor material is located at the side opposite the electrically insulating part relative to the film of strained material.

11. The semiconductor-on-insulator structure as claimed in Claim 6, wherein the semiconductor material part further comprises two layers each of a relaxed or pseudo-relaxed material, one of these two layers being situated between the film made of strained material and the electrically insulating part, and the other of these two layers being situated on the side opposite the electrically insulating part relative to the layer of strained material.

12. The semiconductor-on-insulator structure as claimed in any one of the four preceding claims combined with Claim 7, wherein the relaxed or pseudo-relaxed material is $Si_{1-x}Ge_x$.

13. The semiconductor-on-insulator structure as claimed in the preceding claim, wherein the semiconductor material part is constituted successively from the electrically insulating part:

- by a strained $Si_{1-y}Ge_y$ layer;
- by a layer of relaxed or pseudo-relaxed $Si_{1-x}Ge_x$.

14. The semiconductor-on-insulator structure as claimed in Claim 12, wherein the semiconductor material part is constituted successively from the electrically insulating part:

- by a layer of relaxed or pseudo-relaxed $Si_{1-z}Ge_z$;
- by a layer of strained $Si_{1-y}Ge_y$.

15. The semiconductor-on-insulator structure as claimed in Claim 12, wherein the material semiconductor part is constituted successively from the electrically insulating part:

- by a layer of relaxed or pseudo-relaxed $Si_{1-z}Ge_z$;
- by a layer of strained $Si_{1-y}Ge_y$;
- by a layer of relaxed or pseudo-relaxed $Si_{1-x}Ge_x$.

16. A process for realising a semiconductor-on-insulator structure as claimed in any one of the preceding claims, from a donor wafer comprising an upper layer of crystalline material having a first lattice parameter, comprising the following steps:

(a) growth on the upper layer of the donor wafer of a film of material selected from semiconductor materials having a nominal lattice parameter substantially different to the first lattice parameter, over a thickness sufficiently minimal to be essentially elastically strained:

(b) formation of at least one layer of electrically insulating material having a viscosity temperature T_G greater than the viscosity temperature T_{GSiO2} of the SiO_2 on the surface of the donor wafer on the side where the strained layer was formed and/or on a surface of the receptor substrate;

(c) bonding of the receptor substrate to the donor wafer at the level of the insulating layer(s);

(d) removal of at least a part of the donor wafer.

17. The process as claimed in the preceding claim, further comprising, between step (a) and step (b), an additional growth step of a relaxed or pseudo-relaxed layer, of a material selected from semiconductor materials, on the strained film.

18. The process as claimed in any one of the two preceding claims, wherein the electrically insulating layer is formed, during step (b), by nitriding of the surface(s).

19. The process as claimed in either of Claims 17 and 18, wherein the electrically insulating layer is deposited on at least one surface to be bonded.

20. The process as claimed in either of the two preceding claims, wherein the insulating layer formed during step (b) is made up by Si_3N_4, $Si_xGe_yN_z$ or SiO_yN_z.

21. The process as claimed in any one of the five preceding claims, wherein step (d) relates to removal of a part of the donor wafer, with the part of the donor wafer transferred to the receptor substrate after removal being at least a part of the upper layer of crystalline material.

22. The process as claimed in the preceding claim, characterised in that:

- it comprises an additional step implemented before step (c) consisting of implanting atomic samples into the donor wafer at a preset depth creating an embrittlement zone in the vicinity of the depth of implant; and wherein
- step (d) comprises a power supply so as to cause

detachment at the embrittlement zone present in the donor wafer.

23. The process as claimed in Claim 22, further comprising, prior to step (a), a step of formation of the donor wafer comprising:

- formation of a porous layer on a crystalline support substrate;
- growth of a crystalline layer on the porous layer; the support substrate - porous layer - layer crystalline ensemble constituting the donor wafer, the porous layer constituting an embrittlement zone in the donor wafer;

and wherein step (d) comprises a power supply such as to cause detachment at the embrittlement zone present in the donor wafer.

24. The process as claimed in any one of the three preceding claims, wherein step (d) comprises a finishing step of the surface of the part of the donor wafer transferred to the receptor substrate.

25. The process as claimed in any one of Claims 22 to 24, wherein step (d) also relates to removal of the part of the donor wafer transferred to the receptor substrate, such as to remove all of the donor wafer.

26. The process as claimed in the preceding claim, wherein removal of the part of the donor wafer transferred to the receptor substrate during step (d) is implemented by selective chemical etching with respect to the strained material of the film.