

CLAIMS

1. A computer program product for facilitating processing in a computing environment, said computer program product comprising:
 - a computer readable storage medium readable by a processing circuit and storing instructions for performing a method comprising:
 - obtaining an instruction to perform a load and shift operation; and
 - executing the instruction, the executing comprising:
 - loading data from a location in memory, the location in memory designated by one or more fields associated with the instruction;
 - shifting the data by a shift amount to obtain a shifted value;
 - obtaining an intermediate result using the shifted value; and
 - performing guarded storage detection based on the intermediate result.
2. The computer program product of claim 1, wherein the data comprises a pointer.
3. The computer program product of claim 1, wherein the shifting comprises shifting the data left by the shift amount to obtain the shifted value.
4. The computer program product of claim 1, wherein the method further comprises obtaining the shift amount from a register used to specify one or more attributes of a guarded storage area.
5. The computer program product of claim 1, wherein the performing guarded storage detection comprises:
 - comparing a first portion of the intermediate result with an origin of a guarded storage area;
 - determining whether a particular section of the guarded storage area is guarded, the determining using a second portion of the intermediate result; and
 - detecting a guarded storage event based on the comparing indicating a specific result and the determining indicating the particular section is guarded.

6. The computer program product of claim 5, wherein the performing guarded storage detection further comprises placing the intermediate result in a selected location designated by the instruction, based on the comparing and determining not detecting the guarded storage event.
7. The computer program product of claim 6, wherein the selected location is a register specified by a field of the instruction.
8. The computer program product of claim 1, wherein the obtaining the intermediate result includes adjusting the shifted value based on an addressing mode of a processor executing the instruction.
9. The computer program product of claim 1, wherein the method further comprises determining the location in memory, the determining using an index field, a base field and a displacement field of the instruction.
10. The computer program product of claim 1, wherein the instruction is a single architected instruction comprising an operation code indicating a load logical and shift guarded operation, a register field to specify a register to place a result based on determining that a guarded storage event was not detected, and a plurality of fields to determine the location in memory.
11. A computer system for facilitating processing in a computing environment, said computer system comprising:
 - a memory; and
 - a processor in communication with the memory, wherein the computer system is configured to perform a method, said method comprising:
 - obtaining an instruction to perform a load and shift operation; and
 - executing the instruction, the executing comprising:
 - loading data from a location in memory, the location in memory designated by one or more fields associated with the instruction;
 - shifting the data by a shift amount to obtain a shifted value;
 - obtaining an intermediate result using the shifted value; and

performing guarded storage detection based on the intermediate result.

12. The computer system of claim 11, wherein the performing guarded storage detection comprises:

comparing a first portion of the intermediate result with an origin of a guarded storage area;

determining whether a particular section of the guarded storage area is guarded, the determining using a second portion of the intermediate result; and

detecting a guarded storage event based on the comparing indicating a specific result and the determining indicating the particular section is guarded.

13. The computer system of claim 12, wherein the performing guarded storage detection further comprises placing the intermediate result in a selected location designated by the instruction, based on the comparing and determining not detecting the guarded storage event.

14. The computer system of claim 11, wherein the obtaining the intermediate result includes adjusting the shifted value based on an addressing mode of a processor executing the instruction.

15. The computer system of claim 11, wherein the instruction is a single architected instruction comprising an operation code indicating a load logical and shift guarded operation, a register field to specify a register to place a result based on determining that a guarded storage event was not detected, and a plurality of fields to determine the location in memory.

16. A computer-implemented method of facilitating processing in a computing environment, said computer-implemented method comprising:

obtaining an instruction to perform a load and shift operation; and

executing the instruction, the executing comprising:

loading data from a location in memory, the location in memory designated by one or more fields associated with the instruction;

shifting the data by a shift amount to obtain a shifted value;

obtaining an intermediate result using the shifted value; and

performing guarded storage detection based on the intermediate result.

17. The computer-implemented method of claim 16, wherein the performing guarded storage detection comprises:

comparing a first portion of the intermediate result with an origin of a guarded storage area;

determining whether a particular section of the guarded storage area is guarded, the determining using a second portion of the intermediate result; and

detecting a guarded storage event based on the comparing indicating a specific result and the determining indicating the particular section is guarded.

18. The computer-implemented method of claim 17, wherein the performing guarded storage detection further comprises placing the intermediate result in a selected location designated by the instruction, based on the comparing and determining not detecting the guarded storage event.

19. The computer-implemented method of claim 16, wherein the obtaining the intermediate result includes adjusting the shifted value based on an addressing mode of a processor executing the instruction.

20. The computer-implemented method of claim 16, wherein the instruction is a single architected instruction comprising an operation code indicating a load logical and shift guarded operation, a register field to specify a register to place a result based on determining that a guarded storage event was not detected, and a plurality of fields to determine the location in memory.