An Embedded Stressor Structure and Process

Abstract

Example embodiments are structures and methods for forming an FET with embedded stressor S/D regions (e.g., SiGe), a doped layer below the embedded S/D region adjacent to the isolation regions, and a stressor liner over reduced spacers of the FET gate. We provide a gate structure over a first region in a substrate. We provide isolation regions in the first region spaced from the gate structure; and a channel region in the substrate under the gate structure. We form S/D recesses in the first region in the substrate adjacent to the gate structure. We form S/D stressor regions filling the S/D recesses. We implant dopant ions into the S/D stressor regions and into the substrate below the S/D stressor regions adjacent to the isolation regions to form upper stressor doped regions.

Figure 9