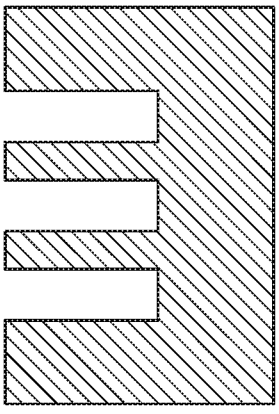
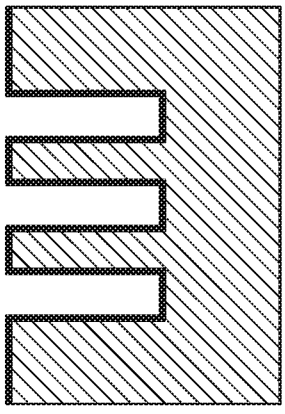
ATTRIBUTES	SILICON INTERPOSER	EMBEDDED Cu TRACE	SAP Cu TRACE
TECHNOLOGY	BEOL	POLYMER WITH CONFORMAL SEED METAL	PR + POLYMER WITH BOTTOM SEED METAL
PLATFORM	WAFER	WAFER	WAFER
MAXIMUM ROUTING/mm (L/S: μm)	~1300 (0.4/0.4)	~330 (2/1)	~500 (1/1)
COST	HIGH	LOW	LOW
RF INSERTION LOSS AT HIGH FREQUENCY	MEDIUM HIGH	LOW	MEDIUM HIGH

FIG. 1



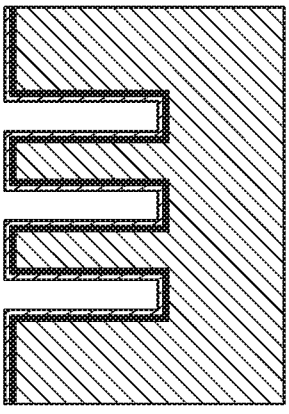
Via etching on Silicon

FIG. 2A



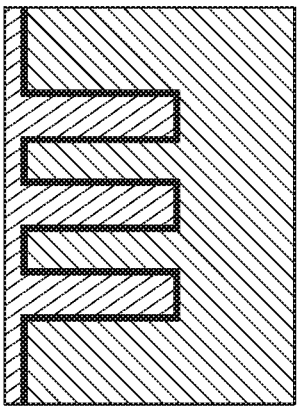
Dielectric layer deposition

FIG. 2B



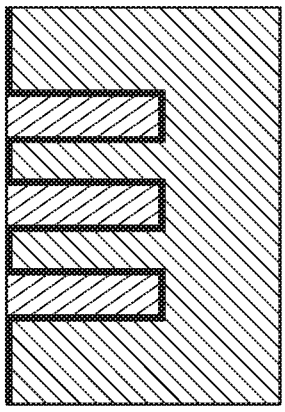
Barrier/adhesion layer and seed layer deposition

FIG. 2C



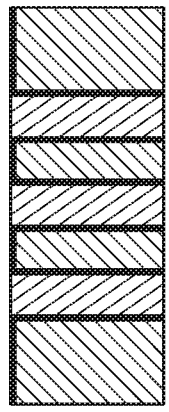
Electroplating

FIG. 2D



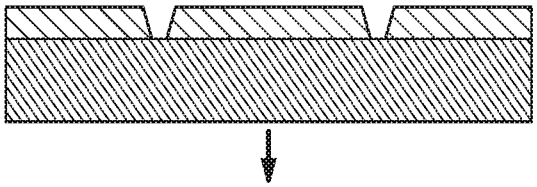
Chemical mechanical polishing

FIG. 2E



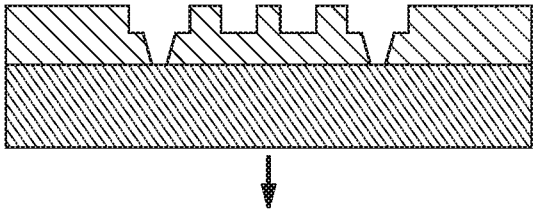
Silicon back grinding/etching

FIG. 2F



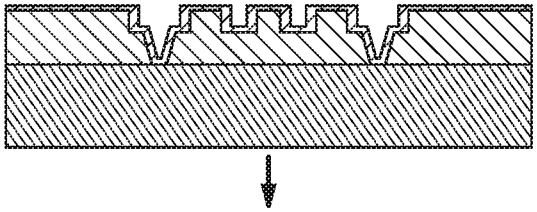
Dielectric1 process

FIG. 3A



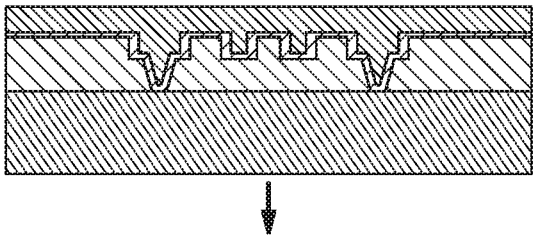
Dielectric2 process

FIG. 3B



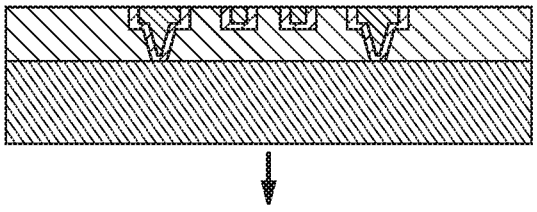
Seed layer PVD

FIG. 3C



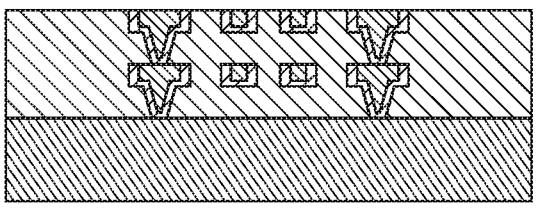
Cu ECP

FIG. 3D



Excess Cu overburden & seed layer Removal

FIG. 3E



RDL2 formation

FIG. 3F

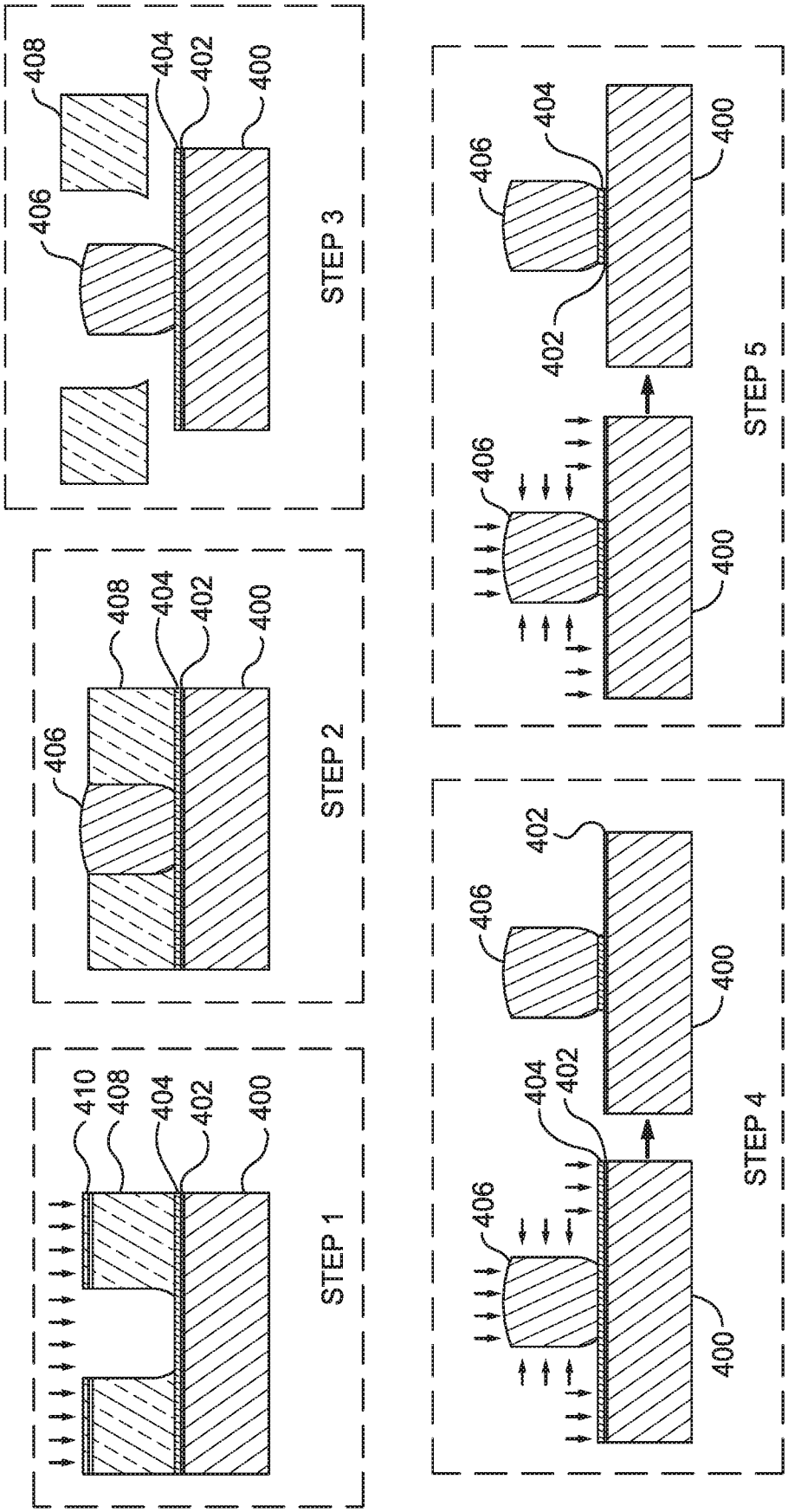

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STEP 5
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FIG. 4

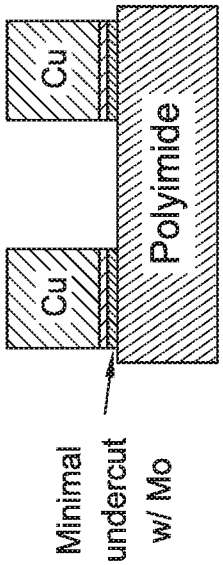


FIG. 5D

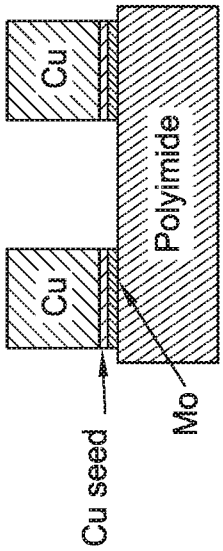


FIG. 5E

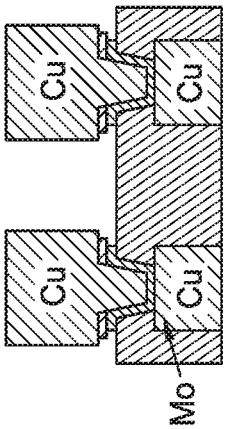


FIG. 5F

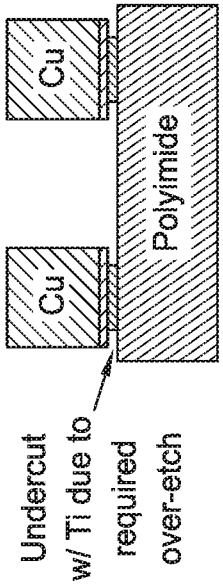


FIG. 5A

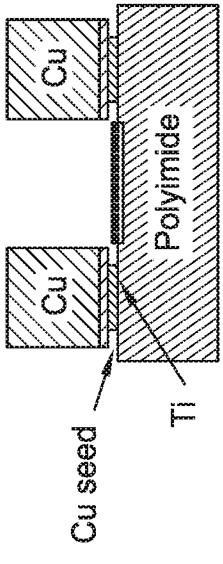


FIG. 5B

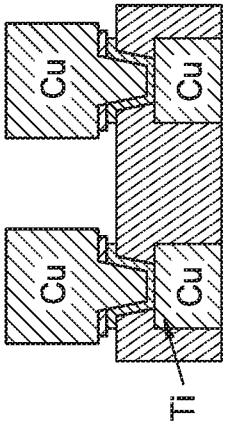


FIG. 5C