

Apparatus for and Method of Synchronizing a Clock Signal

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Abstract of the Disclosure

The present disclosure includes a discussion of a method of synchronizing a sampling clock signal to a received data
10 signal (131). The clock recovery circuit (127) generates several clock signals (339, 341, 343, 345) at the symbol rate, with each clock signal having a unique phase. To permit fast initial acquisition, the set of clock signals includes a pair of clocks which differ in phase by one-half of a symbol interval.

15 Additionally, the clock recovery circuitry (127) generates error signals (347, 349, 351, 353) representing the difference between the phase of the received data signal and the phase of each clock signal. The error signals (347, 349, 351, 353) are processed over multiple symbol times to determine the optimal
20 sampling phase. The clock recovery circuit (127) then adjusts or maintains the phase of the symbol clock (139) to provide the optimal sampling phase.

FIGS. 1 & 3 accompanies this abstract.