

DATA READ DEVICE OF VIDEO MEMORY

The present invention relates to data read devices for video memories in digital image processing devices.

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A video memory is a means for recording or storing a composite image signal which has been converted to a digital signal.

Generally, the composite image signal is comprised of a luminance signal Y and chrominance signals R-Y and B-Y, and in order to record the digitalized composite image signal in a memory, the said signal is separated into the luminance signal Y and chrominance signals R-Y and B-Y, so that data of luminance signal Y and chrominance signals R-Y and B-Y can be stored separately.

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Here, a data ratio of the luminance signal Y and chrominance signals R-Y and B-Y comprising the composite image signal is 4:1:1, which is directly recorded into and read out from the video memory.

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However, when the data of a luminance signal and a chrominance signal having different ratios are stored to a separate memory by using a standardized conventional memory, there arises a disadvantage involving a considerable waste of memory.

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As a result of this, in order to optimize a capacity of the memory, the data of luminance signal Y and chrominance signals R-Y and B-Y are mixedly recorded in the video memory in proportion to the ratio of the composite image signal.

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Preferred embodiments of the present invention aim to provide a data read device of a video memory in which, in order to reduce waste of the video memory, R-Y and B-Y signals mixedly recorded in a video memory are read thereby to execute signal processing.

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According to one aspect of the present invention, there is provided a data read device for a video memory, the device comprising:

video memory means wherein luminance signal data and chrominance signal data of a composite image signal are mixedly recorded in a predetermined ratio;

clock generating means for generating a clock signal and a control signal having predetermined frequencies by inputting a reference clock signal, a horizontal synchronizing signal and a vertical synchronizing signal;

address generating means for generating an address signal of the video memory means in response to the control signal generated from the clock generating means;

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image data separating means for respectively separating and outputting the luminance signal data and chrominance signal data in response to the clock signal output from the clock generating means by receiving an input of data output from the video memory means, wherein the image data separating means comprises:

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first delay means for delaying by one clock data read out from the video memory means;

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first latch means for conforming an output time of clock-delayed data from the first delay means to that of undelayed data;

5 second latch means for delaying data output from the first latch means thereby to conform the output time;

10 first separating means for separating the luminance signal and chrominance signal data from the data output from the second delay means thereafter to output the same; and

second separating means for separating data of R-Y and B-Y from the chrominance signal data output from the first separating means; and

15 a Digital-to-Analog converter for converting the luminance signal data and chrominance signal data from the image data separating means to an analog signal.

Preferably, the first delay means comprises:

20 a first flip-flop which inputs data output from one of two video memories and is operated by a clock signal having a first frequency;

25 a second flip-flop which inputs data output from the first flip-flop and is operated by a first clock and

a third flip-flop which inputs data other than the data input to the first flip-flop out of the video memories and is operated by a clock signal having said first frequency.

Preferably, the first latch means comprises:

a fourth flip-flop for inputting data output from the second flip-flop and being operated by the second clock; and

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a fifth flip-flop for inputting data output from the third flip-flop and being operated by the second clock.

Preferably, the second delay means comprises:

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a ninth flip-flop for inputting data output from the fourth flip-flop and being operated by a third clock;

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a sixth flip-flop for inputting data output from the fifth flip-flop and being operated by the third clock;

a seventh flip-flop for inputting data output from the sixth flip-flop and being operated by the third clock; and

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an eighth flip-flop for inputting data output from the seventh flip-flop and being operated by the third clock.

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Preferably, the first separating means comprises first and second multiplexers which input data output from the eighth and ninth flip-flops and operates with a fourth clock as an address signal.

Preferably, the second separating means comprises:

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a tenth flip-flop which inputs data output from the second multiplexer and is operated by a rising edge of the fifth clock; and

5 an eleventh flip-flop which inputs data output from the second multiplexer and is operated by a falling edge of the fifth clock.

The invention extends to a video memory provided with a data read device according to any of the preceding aspects of the invention.

10 The invention extends also to a digital image processing device comprising a video memory or video memory arrangement as above.

For a better understanding of the invention, and to show how the same may be carried into effect, reference will now be made, by way of example, 15 to the accompanying diagrammatic drawings, in which:

Figure 1 is a block diagram of one example of a data read device of a video memory in accordance with the present invention;

20 Figure 2 is a more detailed diagram of one example of an image data separating means as illustrated in Figure 1;

Figure 3a through 3g are data maps of an example of an image signal in an embodiment of the present invention; and

25 Figure 4a through 4f are timing diagrams of one example of a data read device of a video memory in accordance with the present invention.

The data read device of Figure 1 in accordance is provided with means comprising:

5 reading means for reading data from a video memory in which a composite image signal of luminance signal data and chrominance signal data is mixedly recorded in a predetermined ratio; and

10 separating means for separating the read data respectively into luminance data and chrominance data.

Figure 1 is a block diagram of a data read device of a video memory in accordance with the present invention.

15 The data read device of Figure 1 comprises:

a first and a second video memory 10 and 11 wherein the luminance signal data and chrominance signal data of the composite image signal are mixedly recorded in a predetermined ratio;

20 clock generating means 12 for generating a clock signal CKn and control signal SC having a predetermined frequency by inputting a reference clock signal, horizontal synchronizing signal and vertical synchronizing signal;

25 address generating means 13 for generating address signals of the first and second video memories 10 and 11 in response to the control signal generated from the clock generating means 12;

image data separating means 14 for separating respectively and outputting the luminance signal data and chrominance signal data in response to the clock signal CK_n output from the clock generating means 12 by receiving an input of data output from the first and second video memories 10 and 11; and

a Digital-to-Analog (D/A) converter 15 for converting the luminance signal data and chrominance signal data separated from the image data separating means 14.

As shown in Figure 2, the circuit of the image data separating means comprises:

first delay means 200 which inputs data output from the first and second video memories 10 and 11, and operates in response to a first clock signal;

first latch means 201 which inputs data output from the first delay means 200 and operates in response to a second clock signal;

second latch means 202 which inputs data output from the first latch means 201 and operates in response to a third clock signal;

first separating means 203 which inputs data output from the second delay means 202 and operates in response to a fourth clock signal; and

a second separating means 204 which inputs data output from the first separating means 203 and operates in response to a fifth clock signal.

The D/A converter 15 converts digital data output from the first and second separating means 203 and 204 to analog signals thereafter to output the same.

5 The first delay means 200 comprises a first flip-flop 21 which receives data from the first video memory and is operated by the first clock signal, a second flip-flop 22 which receives output data from the first flip-flop 21 and is operated by the first clock signal, and a third flip-flop 23 which receives data output from the second video memory 11 and is operated by the first
10 clock signal.

 The first latch means 201 comprises a fourth flip-flop 24 which receives output data from the second flip-flop and is operated by the second clock signal, and a fifth flip-flop 25 which receives output data from the third
15 flip-flop 23 and is operated by the second clock signal.

 The second delay means 202 comprises: a sixth flip-flop 26 which is operated by the third clock signal and receives output data from the fourth flip-flop 204; a seventh flip-flop 27 which is operated by the third clock signal and receives output data from the fifth flip-flop 25; an eighth flip-flop 28
20 which is operated by the third clock signal and receives output data from the seventh flip-flop 27; and a ninth flip-flop 29 which is operated by the third clock signal and receives output data from the eighth flip-flop 28.

25 The first separating means 203 comprises a first and a second multiplexer 32 and 33 which receive output data from the sixth and ninth flip-flops 26 and 29 and output the data selectively in response to the fourth clock signal.

The second separating means 204 comprises a tenth and an eleventh flip-flop 30 and 31 which receive output data of the second multiplexer 33 and output the data selectively in response to the fifth clock signal.

5 Figure 3a through 3g are data maps of an image signal.

Figure 3a represents a state of an image signal data map stored in the first and second video memories 10 and 11.

10 Figure 3b through 3g are image signal data maps output respectively from the first and second video memories 10 and 11, the first delay means 200, the first latch means 201, the second delay means 202, the first separating means 203 and the second separating means 204.

15 Figure 4a through 4f are examples of timing diagrams of the data read device.

Figure 4a is a waveform drawing of a serial clock SC which is output from the clock generating means 12 thereafter to be supplied to the first and
20 second video memories 10 and 11.

FIG 4b through 4f are waveform drawings of the first, second, third, fourth and fifth clocks, CK1, CK2, CK3, CK4 and CK5 output from the clock generating means 12 thereafter to be supplied to the image data separating
25 means 14.

Accordingly, the clock generating means 12 into which the reference clock, horizontal and vertical synchronizing signals are input as illustrated in

Figure 1 generates a serial clock as illustrated in Figure 4a, a first, second, third, fourth and fifth clock (CKn CK1, CK2, CK3, CK4 and CK5) as illustrated in Figure 4b, 4c, 4d, 4e and 4f, and a control signal thereby to output the same.

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At this moment, the first and second video memories 10 and 11, in which the composite image signals of luminance signal Y, and chrominance signals R-Y and B-Y data are mixedly recorded in Yn, Cm forms (n; 1-682, m; 1-340) output data in response to an address output from the address generating means 13 and a serial clock SC output from the clock generating means 12.

In other words, the luminance signal Yn and chrominance signal Cm are recorded respectively in the forms of Y1, Y2, C2, Y5, Y6, C4 and C1, Y3, Y4, C3, Y7, Y8 at the first and second video memories 10 and 11 as illustrated in Figure 3a.

When the serial clock SC which has a repeated period form of 2:1:1 as illustrated in Figure 4a is input into the first and second video memories 10 and 11, data is output having a form as illustrated in Figure 3b.

Here, a variable n (1 ~ 682) of luminance signal Yn recorded in the first and second video memories 10 and 11 is a number wherein $52 \mu s$, which is an image signal period of the horizontal synchronizing signal period, is divided by 76ns, which is an inverse number of sampling rate designed to make a chrominance subcarrier suitable for sampling theory.

In other words, $52 \mu s / 76ns \approx 682$.

Furthermore, in the composite image signal, because a data ratio 4:1:1 of the luminance signal Y and chrominance signals R-Y and B-Y becomes 682:170:170, a variable m (1~340) of chrominance signal Cm is an aggregate data value of chrominance signals R-Y and B-Y. The data address of the image signal comes to 1022 in rows and because a data address corresponding to 512 scanning lines suffices, when signals which have nothing to do with the image signals are subtracted from 525 scanning lines, only data address corresponding to 512 scanning lines remain, so that a memory capacity of 4Mbit is needed in case 8-bit data is necessary to display one pixel.

Meanwhile, the luminance signal and chrominance signal data output from the first and second memories 10 and 11 in a repeated period form of 2:1:1 as illustrated in Figure 3b are input to the image data separating means 14.

The luminance signal and chrominance signal data output from the first video memory 10 thereafter to be input to the image data separating means 14 as illustrated in Figure 3b are input to a first flip-flop 21 of the first delay means 200 as illustrated in Figure 2.

An output of the first flip-flop 21 is input to a second flip-flop 22 which is operated by the first clock CK1 as illustrated in Figure 4b.

Likewise, the luminance signal and chrominance signal data output from the second video memory 11 as illustrated in Figure 3b are input to a third flip-flop 23 of the first delay means as illustrated in Figure 2.

Here, because the first and second flip-flop 21 and 22 operated by the first clock CK1 as illustrated in Figure 4b are connected in series, an output of the second flip-flop 22 is output, being delayed more than that of the third flip-flop 23 by one clock.

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In other words, the luminance signal and chrominance signal data output from the second and third flip-flop 22 and 23 of the first delay means 200, as illustrated in Figure 3C, are output with the output data of the first video memory 10 being delayed more than that of the second video memory 11 by one clock.

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The luminance signal and chrominance signal data output from the second and third flip-flop 22 and 23 of the first delay means 200 as illustrated in Figure 3C are input to the first latch means 201.

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The luminance signal and chrominance signal data input to the first latch means 201, as illustrated in Figure 4C, are input to a fourth and fifth flip-flop 24 and 25 operated by the second clock signal having a repeated period form of 2:1:1.

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The data input to the fourth and fifth flip-flop 24 and 25 of the first latch means 201 as illustrated in Figure 3C is output in a form as illustrated in Figure 3d by the second clock signal as mentioned above.

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In other words, an output of fourth flip-flop 24 is output in a form delayed more than the output of the fifth flip-flop 25 by 2 clocks.

The kind of data output from the fourth and fifth flip-flops 24 and 25 of the first latch means 201 as illustrated in Figure 3d is respectively input to a sixth and seventh flip-flop 26 and 27 of the second delay means 202.

5 An output of the seventh flip-flop 27 is input to an eighth flip-flop 28.

 An output of the eighth flip-flop 29 is input to a ninth flip-flop 29.

 At this moment, a third clock having a constant period as illustrated in
10 Figure 4d is input to respective flip-flops 26, 27, 28 and 29 of the second delay means 202.

 Accordingly, the data which has gone through the seventh, eighth and ninth flip-flop 27, 28 and 29 is output in a form delayed more than that of the
15 sixth flip-flop 26 by 2 clocks.

 Figure 3e represents a data form output from the sixth flip-flop 26 and ninth flip-flop 29.

20 In other words, an output of the fifth flip-flop 25 which is running ahead by 2 more clocks than that of the fourth flip-flop 24 at the first latch means is output from the second delay means 202 with 2 clocks delayed.

 The data output from the sixth and ninth flip-flop 26 and 29 of the
25 second delay means 202 as illustrated in Figure 3e is input to the first and second multiplexers (MUX) 32 and 33 of the first separating means 203.

The first and second multiplexers 32 and 33, as illustrated in Figure 4e, choose one of the two inputs with the fourth clock as an address signal thereby to output the same.

5 In other words, the first multiplexer 32 receives as respective inputs D1 and D2 the outputs of the sixth and ninth flip-flops 26 and 29 as illustrated in Figure 3e, and the second multiplexer 33 receives as respective inputs D1 and D2 the outputs of the ninth and sixth flip-flops 29 and 26.

10 Therefore, the first multiplexer 32, when the fourth clock is in a high state, outputs the luminance signal Y1, Y2 which is input D1 in Figure 3e, and when in a low state, the first multiplexer 32 outputs the luminance signal Y3, Y4 which is an input D2 as illustrated in Figure 3e.

15 As seen in the foregoing, the first multiplexer 32 selectively outputs luminance signals Y1, Y2, Y3, Y4, Y5, as illustrated in Figure 3f.

The second multiplexer 33 selects one of the inputs D1 and D2 which are inverted by an inverter I1 thereby to output the same.

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Accordingly, the second multiplexer 33, when the fourth clock is in a high state, outputs a chrominance signal C1 which is the input D2 as illustrated in Figure 3e, and when in a low state, the second multiplexer 33 outputs a chrominance signal C2 which is the input D1 as illustrated in Figure 3e.

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As seen in the foregoing, the second multiplexer 33 selectively outputs chrominance signals C1, C2, C3 as illustrated in Figure 3f.

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Meanwhile, the signal output from the second multiplexer 33 is input to the second separating means 204.

5 The second separating means 204 comprises a tenth flip-flop 30 which is operated at a rising edge of a fifth clock signal and an eleventh flip-flop 31 which is operated at a falling edge, as illustrated in Figure 4f.

Therefore, the tenth flip-flop 30, whenever the chrominance signal C1 is input, delays the chrominance signal by 4 clocks thereafter to output the same, and the eleventh flip-flop 31, whenever the chrominance signal C2 is input, delays the chrominance signal by 4 clocks thereafter to output the same.

Figure 3g represents a data form input to the D/A converter 15.

15 In other words, the luminance signal Y_n output from the first multiplexer 32 of the first separating means 203 and the chrominance signal C_m output from the tenth and eleventh flip-flops 30 and 31 of the second separating means 204 are input to the D/A converter 15.

20 In Figure 3g, the luminance signals, $Y_1, Y_2, Y_3 \dots$ are the luminance signals of the composite image signal.

The chrominance signals $C_1, C_3 \dots$ are R-Y signals, of the composite image signal and the chrominance signals $C_2, C_4 \dots$ are B-Y signals of the composite image signal.

The D/A converter 15, as explained in the above, converts the separated luminance signal and chrominance signal to analog signals thereby to output the same.

5 As depicted in the foregoing, the described embodiments of the present invention have an effect of outputting and processing the composite image signal data mixedly recorded in the video memory in the same form as it is stored in the initial video memory in order to reduce waste of memory.

10 Although presently preferred embodiments of the invention have been described in detail above, it will be understood by one of ordinary skill in the art that various modifications can be made, without departing from the scope of the invention.

CLAIMS

1. A data read device for a video memory, the device comprising:

5 video memory means wherein luminance signal data and chrominance signal data of a composite image signal are mixedly recorded in a predetermined ratio;

10 clock generating means for generating a clock signal and a control signal having predetermined frequencies by inputting a reference clock signal, a horizontal synchronizing signal and a vertical synchronizing signal;

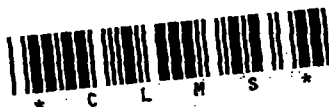
15 address generating means for generating an address signal of the video memory means in response to the control signal generated from the clock generating means;

20 image data separating means for respectively separating and outputting the luminance signal data and chrominance signal data in response to the clock signal output from the clock generating means by receiving an input of data output from the video memory means wherein the image data separating means comprises:

25 first delay means for delaying by one clock data read out from the video memory means;

first latch means for conforming an output time of clock-delayed data from the first delay means to that of undelayed data;

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second latch means for delaying data output from the first latch means thereby to conform the output time;

5 first separating means for separating the luminance signal and chrominance signal data from the data output from the second delay means thereafter to output the same; and

second separating means for separating data of R-Y and B-Y from the chrominance signal data output from the first separating means; and

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a Digital-to-Analog converter for converting the luminance signal data and chrominance signal data from the image data separating means to an analog signal.

15 2. A data read device according to claim 1, wherein the first delay means comprises:

a first flip-flop which inputs data output from one of two video memories and is operated by a clock signal having a first frequency;

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a second flip-flop which inputs data output from the first flip-flop and is operated by a first clock and

25 a third flip-flop which inputs data other than the data input to the first flip-flop out of the video memories and is operated by a clock signal having said first frequency.



3. A data read device according to claim 2, wherein the first latch means comprises:

a fourth flip-flop for inputting data output from the second flip-flop and
5 being operated by the second clock; and

a fifth flip-flop for inputting data output from the third flip-flop and
being operated by the second clock.

10 4. A data read device according to claim 3, wherein the second delay means comprises:

a ninth flip-flop for inputting data output from the fourth flip-flop and
being operated by a third clock;

15 a sixth flip-flop for inputting data output from the fifth flip-flop and
being operated by the third clock;

a seventh flip-flop for inputting data output from the sixth flip-flop and
20 being operated by the third clock; and

an eighth flip-flop for inputting data output from the seventh flip-flop
and being operated by the third clock.

25 5. A data read device according to claim 4, wherein the first separating means comprises first and second multiplexers which input data output from the eighth and ninth flip-flops and operates with a fourth clock as an address signal.



6. A data read device according to claims 1 and 3, or to claim 4 or 5 as
appendant thereto, wherein the second separating means comprises:

a tenth flip-flop which inputs data output from the second multiplexer
5 and is operated by a rising edge of the fifth clock; and

an eleventh flip-flop which inputs data output from the second
multiplexer and is operated by a falling edge of the fifth clock.

10 7. A data read device substantially as hereinbefore described with
reference to Figure 1 of the accompanying drawings.

8. A data read device substantially as hereinbefore described with
reference to Figures 1 and 2 or Figures 1 to 4 of the accompanying drawings.

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9. A video memory provided with a data read device according to any of
the preceding claims.

10. A digital image processing device comprising a video memory or video
20 memory arrangement according to claim 9.

