

-1-

METHODS, STRUCTURES AND DEVICES FOR INCREASING MEMORY DENSITY

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PRIORITY CLAIM

This application claims the benefit of the filing date of United States Patent Application Serial Number 12/610,922, filed November 2, 2009, for "METHODS, STRUCTURES AND DEVICES FOR INCREASING MEMORY DENSITY."

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TECHNICAL FIELD

Embodiments of the present invention relate to methods, structures, and devices for increasing memory density and, more specifically, to methods for forming multi-layer semiconductor structures and resulting structures and devices incorporating such structures.

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BACKGROUND

Non-volatile memory devices are used to store digital data for computer systems and other electronic devices. Non-volatile memory does not change state upon removal or failure of power applied thereto and, thus, retains stored data even for subsequent retrieval despite interruptions in power supply. Examples of non-volatile memory cells include magnetic random access memory (MRAM), ferroelectric random access memory (FRAM), phase-change random access memory (PCRAM), or resistance random access memory (RRAM).

Due to the ever-increasing demand for non-volatile memory, developers and manufacturers are constantly attempting to increase the density of non-volatile memory cells beyond the capability of current technologies. To reach high storage densities, manufacturers typically focus on scaling down semiconductor devices to submicron dimensions. However, conventional non-volatile memory cells utilize a significant amount of real estate on a semiconductor substrate and, thus, the density of non-volatile memory cells is limited.

There is a need for methods, structures and devices for increasing density and reliability in non-volatile memory devices.

-2-

DISCLOSURE

Various embodiments of the present disclosure are directed toward embodiments of a non-volatile memory device, a semiconductor structure and a method for forming a semiconductor structure comprising a plurality of diodes. In at least one embodiment, present disclosure includes non-volatile memory devices that comprise a plurality of transistors disposed on a substrate, a plurality of memory strings disposed over the plurality of memory cells, each comprising a plurality of diodes and an electrode electrically connecting at least two of the plurality of memory strings to the at least one node, the plurality of diodes arranged at locations spaced along a length of the electrode. Each transistor of the plurality of transistors may be electrically coupled to a word line and a bit line, the word line and the bit line intersecting one another at at least one node.

In further embodiments, the present disclosure includes semiconductor structures that comprise a plurality of diodes overlying a substrate and vertically superimposed over one another to form a plurality of columns, each of the plurality of diodes comprising an intrinsic region disposed between oppositely doped regions. The plurality of diodes of adjacent columns may be mirror images of one another.

In yet further embodiments, the present disclosure includes methods of forming a semiconductor structure comprising forming a plurality of alternating first regions and second regions to form a cell stack over a foundation material overlying a transistor array, the transistor array comprising a plurality of transistors electrically coupled to a plurality of cell plugs, removing portions of the first regions and second regions exposed through a mask to form a plurality of first slots therethrough, each of the plurality of first slots overlying one of the plurality of cell plugs, introducing a dopant to exposed portions of the first regions to form a plurality of first doped regions, forming a silicide material over each of the plurality of first doped regions, forming a fill material over the semiconductor structure to at least fill the plurality of first slots, removing portions of the first regions and second regions exposed through another mask to form a plurality of second slots laterally spaced apart from each of the plurality of first slots and introducing a dopant to exposed portions of the first regions to form a plurality of second doped regions, an intrinsic region of the first

-3-

region disposed between the plurality of second doped regions and the plurality of first doped regions.

BRIEF DESCRIPTION OF THE DRAWINGS

5 FIG. 1A is a top down view illustrating one embodiment of a memory device of the present invention;

 FIG. 1B is a partial cross-sectional view of the memory device shown in FIG. 1A taken along section line 1-1;

 FIG. 2 is an electrical circuit diagram of the memory device of FIGS. 1A
10 and 1B;

 FIGS. 3A-32B are top down and cross-sectional views illustrating an embodiment of a method of the present invention used to form the memory device shown in FIGS. 1A and 1B;

 FIG. 33A is a top down view illustrating another embodiment of a memory
15 device of the present invention;

 FIG. 33B is a partial cross-sectional view of the memory device shown in FIG. 33A taken along section line 33-33;

 FIGS. 34-36 are partial cross-sectional views of a semiconductor structure and illustrate an embodiment of a method of the present invention used to form the
20 memory device shown in FIGS. 33A and 33B;

 FIG. 37A is a top down view illustrating yet another embodiment of a memory device of the present invention;

 FIG. 37B is a partial cross-sectional view of the memory device shown in FIG. 37A taken along section line 37-37; and

25 FIGS. 38 and 39 are partial cross-sectional views of a semiconductor structure and illustrate an embodiment of a method of the present invention used to form the memory device shown in FIGS. 37A and 37B.

MODE(S) FOR CARRYING OUT THE INVENTION

30 The illustrations presented herein are not meant to be actual views of any particular device or system, but are merely idealized representations that are

-4-

employed to describe the present invention. Additionally, elements common between figures may retain the same numerical designation. It will be appreciated that for simplicity and clarity of illustration, reference numerals for elements common between figures are not necessarily shown in each of the figures.

5 FIGS. 1A and 1B show an embodiment of a portion of memory device 100 of the present invention. FIG. 1B is a cross-sectional view of the memory device 100 shown in FIG. 1A, taken along section line 1-1 therein. The memory device 100 includes at least one memory string 102 in which a plurality of diodes 104 are electrically coupled to and spaced along a length of an electrode 110. The memory
10 device 100 may be disposed on a conventional multi-gate memory device formed on a substrate 108, such as, a conventional MOSFET array 106. As used herein, the term “substrate” means and includes a structure that includes semiconductor type material including, for example, silicon, germanium, gallium arsenide, indium phosphide, and other III-V or II-VI type semiconductor materials. Substrates
15 include, for example, not only conventional substrates but also other bulk semiconductor substrates such as, by way of non-limiting example, silicon-on-insulator (SOI) type substrates, silicon-on-sapphire (SOS) type substrates, and epitaxial silicon supported by a base material. Semiconductor type materials may be doped or undoped. When reference is made to a “substrate” in the following
20 description, previous process acts may have been utilized to at least partially form elements or components of an integrated circuit or device in or over a surface of the substrate 108.

 The diodes 104 of each memory string 102 may be electrically coupled to one another and to the underlying MOSFET array 106 via the electrode 110. Active
25 elements of the memory device 100 (*i.e.*, elements through which charge carriers travel), or materials used to form such active elements, are cross-hatched to simplify the figures herein. Each memory string 102 may be isolated from an adjacent memory string 102 by dielectric studs 196. The dielectric studs 196 may include, for example, an oxide material or a nitride material. The diodes 104 may be arranged in a
30 predetermined number of rows 114 and columns 116, the rows 114 and columns 116 being aligned in two, intersecting planes. In each of the columns 116, the diodes 104

-5-

may be vertically superimposed in a first direction, Y, substantially perpendicular to a major plane of the substrate 108. Each of the diodes 104 in the column 116 is separated from adjacent diode(s) 104 by an interlayer dielectric material 118. By way of non-limiting example, the interlayer dielectric material 118 may include an oxide material, such as, silicon dioxide. The diodes 104 within each of the rows 114 may be aligned with the diodes 104 of laterally adjacent rows 114 in a second direction, X, substantially parallel to the major plane of the substrate 108. Although the memory device 100 is shown with three (3) rows 114, any number, n, of rows 114 may be formed.

Each electrode 110 effectively forms a node at a point of contact between the diodes 104 of each of the memory strings 102. In some embodiments, a contact plug 132 may be electrically coupled to the underlying MOSFET array 106 via a cell plug 158 (shown in broken lines) to provide electrical communication between the diodes 104 of the memory string 102 and the MOSFET array 106, as will be described in further detail below.

The memory device 100 may include a contact structure 134 positioned above an isolation region 136 in the substrate 108. The contact structure 134 may provide electrical communication between the memory device 100 and conductive elements of a higher level substrate (not shown), such as a circuit board. The contact structure 134 may include semiconductive paths 138, contacts 140, line interconnects 142 and a metal line 144. Each of the semiconductive paths 138 extends between at least one of the electrodes 110 and one of the contacts 140 of the contact structure 134. Optionally, the first doped region 122 and the barrier material 128 may be disposed between each of the semiconductive paths 138 and the electrode 110. Each of the line interconnects 142 may extend between one of the contacts 140 and the metal line 144 to electrically couple each memory string 102 with the metal line 144. As shown in FIG. 1A, portions of the metal line 144 may be exposed through an optional passivation material 146.

Each of the diodes 104 may include an intrinsic region 120 disposed between a first doped region 122 and a second doped region 124, a silicide region 126 adjacent the first doped region 122 and a barrier material 128 adjacent the second

-6-

doped region 124. The intrinsic region 120, the first doped region 122, the second doped region 124, the silicide region 126 and the barrier material 128 may extend in a direction perpendicular to a major plane of the substrate 108. The intrinsic region 120 may include a semiconductor material such as, for example, polysilicon, germanium, gallium arsenide or silicon germanium. Each of the first and second doped regions 122 and 124 may include polysilicon that is doped with an n-type dopant, such as phosphorous or arsenic, (i.e., p-type polysilicon) or a p-type dopant, such as boron or aluminum (i.e., n-type polysilicon). The first doped region 122 and the second doped region 124 may be oppositely doped. As used herein, the term “oppositely doped” means that one of the first and second doped regions 122 and 124 includes a surplus of negative charge carriers (n-type), while the other includes a surplus of positive charge carriers (p-type). For example, first doped region 122 (i.e., the doped region 122 adjacent the silicide region 126) may include p-type polysilicon while the second doped region 124 (i.e., the doped region 124 adjacent the barrier material 128) may include n-type polysilicon. The barrier material 128 may include, for example, a dielectric material, such as an oxide material or a nitride material. By way of non-limiting example, the silicide region 126 may be a non-transition metal silicide, such as cobalt silicide (CoSi_2), which is often referred to as “ CoSi_x ,” titanium silicide (TiSi_2), tungsten silicide (TiSi_2) or nickel silicide (NiSi_2). The barrier material 128 may be in contact with the electrode 110. Diodes 104 on opposing sides of the electrode 110 may be mirror images of one another, wherein the intrinsic region 120, the first doped region 122, the second doped region 124, the silicide region 126 and the barrier material 128 are reversed in position relative to an axis electrode. Each of the electrodes 110 may include, for example, a sidewall spacer 130 and a contact plug 132. Each of the sidewall spacers 130 may be disposed over sidewalls of the interlayer dielectric material 118 and the barrier material 128.

FIG. 2 is a circuit diagram illustrating the memory device 100 shown in FIGS. 1A and 1B. The memory device 100 includes the plurality of memory strings 102, each of the diodes 104 of which is electrically coupled to access lines, for example, a first word line 161 and a second word line 163. The first word

-7-

line 161 and the second word line 163 may be electrically coupled to a data/sense line, for example, a bit line 162 and another access line, for example, another word line 160. The first word line 161 and the second word line 163 provide two distinct addresses for each of the memory strings 102 such that the memory device 100 may
5 include, for example, two bits per node.

FIG. 3A is a top down view of a semiconductor structure 101 having the conventional MOSFET array 106 shown in FIGS. 1A and 1B formed on a substrate 108. To form the semiconductor structure 101, a plurality of cell plugs 158, an upper surface of which is exposed and positioned lateral to an
10 electrically insulative material 164, may be aligned in the second direction X and in a third direction Z. FIG. 3B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 3A is taken along section line 3-3. As shown in FIG. 3B, each of the cell plugs 158 is positioned laterally to the electrically insulative material 164 and nitride caps 166. The MOSFET array 106 may include a
15 plurality of transistors, such as, MOSFET devices 148, each of which includes a gate region 150 overlying an oxide region 151 and a semiconductive material 153 and is positioned between insulative spacers 152. The MOSFET devices 148 are each disposed between a source region 154 and a drain region 156 in the substrate 108. Cell plugs 158 are disposed between the MOSFET devices 148. Each gate
20 region 150 of the MOSFET devices 148 may be electrically coupled to the word line 160 while each source region 154 may be electrically coupled to the bit line 162 by a polysilicon plug 152. The electrically insulative material 164, such as an oxide material, overlies portions of the gate regions 150 exposed through the cell plugs 158 and a surface of the substrate 108. Each bit line 162 is covered, for
25 example, by a nitride cap 166. The MOSFET device 106 may be formed using conventional methods which are known in the art and, thus, are not described in detail herein.

As shown in FIG. 4, a foundation material 168 may be formed over the MOSFET array 106. As a non-limiting example, the foundation material 168 may
30 include a doped or undoped polysilicon material, or an oxide material. The foundation material 168 may be deposited using, for example, a conventional CVD

-8-

process. A cell stack 170 including a plurality of alternating first regions 172a, 172b and 172c and second regions 174a, 174b, and 174c may be formed over the foundation material 168. The cell stack 170 shown in FIG. 4 includes three (3) first regions 172a, 172b and 172c and three (3) second regions 174a, 174b and 174c.

5 However, the cell stack 170 may be formed to include any number of first regions 172a, 172b and 172c and second regions 174a, 174b and 174c based on a desired number of diodes 104 to be formed in each memory string 102. Each of the first regions 172a, 172b and 172c and second regions 174a, 174b and 174c of the cell stack 170 is formed from a material that may be selectively etched with respect to underlying materials. In some embodiments, the first regions 172a, 172b and 172c and second regions 174a, 174b and 174c may each be formed from a material that may be selectively etched with respect to overlying materials. By way of non-limiting example, each of the first regions 172a, 172b and 172c of the cell stack 170 may be formed from a doped or undoped polysilicon material, germanium, gallium arsenide or silicon germanium and may have a thickness of from about 20 nm to about 40 nm. For example, the second regions 174a, 174b and 174c may be formed from a doped or undoped polysilicon material and the first regions 172a, 172b and 172c may be formed from a doped or undoped polysilicon material selectively etchable with respect to an underlying one of the second regions 174a, 174b, and 174c. As another non-limiting example, the second regions 174a, 174b and 174c may be formed from a semiconductive material, such as, a polysilicon material, and the first regions 172a, 172b and 172c may be formed from a dielectric material, such as, an oxide material. Each of the second regions 174a, 174b and 174c of the cell stack 170 may be formed from, for example, a doped or undoped polysilicon, an oxide material, a nitride material or an oxynitride material and may have a thickness of from about 20 nm to about 50 nm. In some embodiments, the first regions 172a, 172b and 172c and the second regions 174a, 174b, and 174c may be deposited over one another using a conventional chemical vapor deposition (CVD) process.

In another embodiment, the second regions 174a, 174b and 174c may be formed from an oxide material, and the first regions 172a, 172b and 172c may be formed from crystalline silicon. In such an embodiment, each of the first

-9-

regions 172a, 172b and 172c formed from crystalline silicon may be placed on a dielectric material, such as the foundation material 168 or one of the second regions 174a, 174b, and 174c, by a process described herein using a modification of the so-called SMART-CUT® technology. Such processes are described in detail in, for example, U.S. Patent No. RE 39,484 to Bruel, U.S. Patent No. 6,303,468 to Aspar et al., U.S. Patent No. 6,335,258 to Aspar et al., U.S. Patent No. 6,756,286 to Moriceau et al., U.S. Patent No. 6,809,044 to Aspar et al., U.S. Patent No. 6,946,365 to Aspar et al., and U.S. Patent Application Publication No. 2006/0099776 to Dupont. However, other processes suitable for manufacturing a semiconductor material on the surface of a logic device may also be used, if sufficiently low process temperatures are maintained. In conventional implementation of SMART-CUT® technology, donor and acceptor wafers are bonded together using a high temperature anneal, on the order of about 100⁰⁰C to about 130⁰⁰C. However, an additional plasma activation act may be integrated into a conventional SMART-CUT® technology fabrication process to lower a required bonding temperature, as described in detail below.

As shown in FIG. 5, a plurality of ions (*e.g.*, hydrogen or inert gas ions) may be implanted into a donor wafer 600 formed from crystalline silicon to form an implanted region 602. As represented by directional arrows 604, an ion source (not shown) may be used to implant the plurality of ions into the donor wafer 600 in a direction substantially perpendicular to a major surface 606 of the donor wafer 600 to create the implanted region 602 which may also be characterized as a transfer region, an inner boundary 608 of which is shown in the donor wafer 600 in broken lines. As known in the art, the depth to which the ions are implanted is at least partially a function of the energy with which the ions are implanted into the donor wafer 600. Generally, ions implanted with less energy will be implanted at relatively shallow depths, while ions implanted with higher energy will be implanted at relatively deep depths. The inner boundary 608 of implanted region 602 lies substantially parallel to the major surface 606 of the donor wafer 600 and is at a predetermined depth which is dependent on selected parameters of the atomic species implant process, as is known to one of ordinary skill in the art. As a

-10-

non-limiting example, ions may be implanted into the donor wafer 600 with an energy selected to form the inner boundary 608 at depth D2 of between about 20 nm and about 50 nm, and more particularly, about 30 nm.

5 The inner boundary 608 includes a layer of microbubbles or microcavities (not shown) including the implanted ion species, and provides a weakened structure within donor wafer 600. The donor wafer 600 may then be thermally treated at a temperature above that at which implantation is effected, in accordance with the disclosures of the patent documents in the preceding paragraph, to effect crystalline rearrangement in the wafer and coalescence of the microbubbles or microcavities.

10 An attachment surface (not shown) may be formed by exposing the major surface 606 of the donor wafer 600 to a reactive ion etching (RIE) plasma including an inert gas (e.g., argon, oxygen, or nitrogen) to form a plasma-activated material. The plasma-activated material increases the kinetics of a subsequent bonding act in the form of an oxide reaction with adjacent material of the foundation material 168 or one of the second regions 174a and 174b, due to the increased mobility of the ionic species (e.g., hydrogen) created on the major surface 606 thereof. By utilizing a plasma-activated material, the wafer bonding process may be performed at temperatures of less than about 400°C. One embodiment of plasma-activated bonding is described in U.S. Patent 6,180,496 to Farrens et al., assigned to Silicon 20 Genesis Corporation.

As shown in FIG. 6, the donor wafer 600 is disposed on a surface of the foundation material 168 and may be bonded to the foundation material 168 using an annealing process as described above. The hydrogen or other ions implanted in ion implanted region 602 to the depth of inner boundary 608 makes the silicon in the 25 thermally treated donor wafer 600 susceptible to breakage along inner boundary 608 when a shear force is applied substantially parallel to the major surface of the donor wafer 600. After attaching the donor wafer 600 to the semiconductor structure 101, the portion of the donor wafer 600 on the side of the inner boundary 608 opposing the major surface of the foundation material 168 (the portion of the donor wafer 600 30 furthest away from the semiconductor structure 101) may be cleaved or fractured by applying a shearing force to the donor wafer 600. The portion of the donor

-11-

wafer 600 below the inner boundary 608, having a thickness, for example, of between about 20 nm and about 50 nm, is detached from the donor wafer 600 and remains bonded to the semiconductor structure 101 to form first region 172a including crystalline silicon as shown in FIG. 8.

5 Referring still to FIG. 7, after the implanted region 602 is separated from the donor wafer 600 and bonded over the foundation material 168, forming first region 172a, an exposed surface thereof may be undesirably rough. To remedy this deficiency, the exposed surface of the first region 172a may be smoothed to a desired degree in order to facilitate further processing as described below, according to
10 techniques known in the art such as, for example, one or more of grinding, wet etching, and chemical-mechanical polishing (CMP). After placing the first region 172a on the foundation material 168, second region 174a may be formed on the first region 172a, as described above. Alternating first regions 172b, 172c and second regions 174b, 174c may be formed to produce the cell stack 170 shown in
15 FIG. 5, with each of the first regions 172b, 172c and second regions 174b, 174c formed as described above. Thus, the cell stack 170 may include polysilicon, germanium, gallium arsenide or silicon germanium, or crystalline silicon, as the first regions 172a, 172b and 172c.

Referring to FIG. 8, a mask material 176 may be formed over semiconductor
20 structure 101. The mask material 176 may include a material having a different etch selectivity than the second regions 174a, 174b and 174c and the first regions 172a, 172b and 172c of the cell stack 170. By way of non-limiting example, the mask material 176 may include a nitride material, such as silicon nitride (Si_3N_4), having a thickness of between about 80 nm to about 200 nm and, more particularly, about
25 120 nm. A conventional chemical vapor deposition (CVD) process, or any other process known in the art of semiconductor fabrication, may be used to form the mask material 176 over the cell stack 170. As another non-limiting example, the mask material 176 may include a hard mask material, such as amorphous carbon or a metal, and may be formed by a conventional chemical vapor deposition (CVD)
30 process, a conventional physical vapor deposition process (i.e., sputtering), or an electroless deposition process.

-12-

Referring to FIGS. 9A and 9B, portions of each of the mask material 176, the second regions 174a, 174b and 174c and the first regions 172a, 172b and 172c may be removed from a peripheral region 181 of the semiconductor structure 101 to form a plurality of tiers 182a, 182b and 182c. Each of the tiers 182a, 182b and 182c may expose respective portions of the first regions 172a, 172b and 172c that will later be used to form the semiconductive paths (FIG. 1). Referring to FIG. 9B, which is a cross-sectional view of the semiconductor structure 101 shown in FIG. 9A taken along section line 9-9 therein, the semiconductor structure 101 may include a lower tier 182a, an intermediate tier 182b and an upper tier 182c.

As a non-limiting example, the tiers 182a, 182b and 182c may be formed as shown in FIG. 9B1. A first photoresist material 184 may be deposited over the mask material 176 and patterned to expose a surface of the mask material 176 overlying a region of the semiconductor device 101 in which the lower tier 182a (FIG. 9B) will be formed. After removing the portions of the mask material 176, portions of the second region 174c exposed through the mask material 176 may be selectively removed with respect to the mask material 176. For example, if the second region 174c includes silicon dioxide, a reactive ion etching (RIE) process using a nitrogen trifluoride (NF₃)-based gas, a chlorine (Cl)-based gas or a bromide (Br)-based gas may be performed to selectively remove the silicon dioxide with respect to the mask material 176. As another non-limiting example, if the second region 174c includes a doped or undoped polysilicon material, a wet etching process may be used to selectively remove the doped or undoped polysilicon material with respect to the mask material 176 and the underlying first region 172c. After removing the portions of the second region 174c, portions of the first region 172c may be exposed through the mask material 176 and the second region 174c. The exposed portions of the first region 172c may then be selectively removed with respect to the mask material 176. As a non-limiting example, if the first region 172c includes polysilicon, a reactive ion etching (RIE) process using a tetrafluoromethane (CF₄)-based plasma, hydrogen bromide (HBr)-based plasma or hydrochloric acid (HCl)-based plasma may be performed to remove the polysilicon with respect to the mask material 176. As another non-limiting example, if the first region 172c

-13-

includes a doped or undoped polysilicon material, a wet etching process may be performed to selectively remove the doped or undoped polysilicon material with respect to the mask material 176 and the underlying second material 174b. The second regions 174b and 174a and the first region 172b exposed through the mask material 176 may be removed, as shown in broken lines, to form the lowermost tier 182a, which is defined by a surface of the first region 172a. As represented by the broken lines designated as 186, an additional portion of the first photoresist material 184 may be removed to expose another portion of the mask material 176 overlying a region of the cell stack 170 in which the intermediate tier 182b will be formed. Thereafter, portions of the mask material 176, the second regions 174c and 174b and the first region 172c exposed through the first photoresist material 184 may be removed, as shown in broken lines, to form the intermediate tier 182b which is defined by a surface of the first region 172b. Another portion of the first photoresist material 184 may be removed overlying a region of the semiconductor structure 101 in which the upper tier 182c will be formed, as represented by the broken lines designated as 188. A portion of the second region 174c exposed through the first photoresist material 184 may be removed to form the upper tier 182c defined by a surface of the first region 172c.

Alternatively, the plurality of tiers 182a, 182b and 182c may be formed as shown in FIG. 9B2. The first photoresist material 184 may be deposited over the mask material 176 and may be patterned to expose a surface of the mask material 176 overlying a region of the semiconductor device 101 in which the upper tier 182c (FIGS. 10A and 10B) will be formed. A portion of the second region 174c exposed through the mask material 176 may be removed to define the upper tier 182c, as shown in broken lines designated as 191, using methods such as those described with respect to FIG. 9B1. A second photoresist material 192 may be deposited and patterned to expose remaining portions of mask material 176 overlying a region of the semiconductor device 101 in which the intermediate tier 182b will be formed. A portion of each of the first region 172c and the second region 174b exposed through the second photoresist material 192 may be removed to form the intermediate tier 182b, as shown in broken lines designated as 193. A third

-14-

photoresist material 194 may be deposited and patterned to expose remaining portions of the cell stack 170 that will form the lower tier 182a. A portion of each of the first region 172b and the second region 174a exposed through the third photoresist material 194 may be removed to form the lower tier 182c, as shown in
5 broken lines designated as 195.

Referring to FIGS. 10A and 10B, the contacts 140 may be formed on the semiconductor structure 101 after forming the plurality of tiers 182a, 182b and 182c. Exposed portions of the first regions 172a, 172b and 172c on the tiers 182a, 182b and 182c may be doped with a desired concentration of a dopant to form doped
10 material 121 and, then, portions of the doped material may be converted to a silicide to form the contacts 140. Exposed portions of the first regions 172a, 172b and 172c may be doped using conventional methods, such as an ion implantation process or a high temperature diffusion process. By way of non-limiting example, if the first regions 172a, 172b and 172c include polysilicon, the semiconductor structure 101
15 may be exposed to a boron- or an aluminum-containing plasma such that a p-type polysilicon is formed. As another example, a thin film of a p-type material (not shown) may be deposited over surfaces of the semiconductor structure 101 and a thermal anneal may be performed during which p-type dopants migrate into the first regions 172a, 172b and 172c to form p-type polysilicon.

20 Portions of the doped material of the first regions 172a, 172b and 172c may be converted to a silicide to form the contacts 140. In some embodiments, the contacts 140 may be formed by depositing a non-transition metal, such as cobalt, titanium, tungsten or nickel, over the doped material and heating to temperature sufficient to cause the non-transition metal to react with the doped material 121,
25 forming the silicide regions 126 and the contacts 140. Remaining portions of the doped material 121 may be disposed between the silicide regions 126 and the first regions 172a, 172b and 172c. For example, if the doped material includes a p-type polysilicon, cobalt may be deposited into the p-type polysilicon and annealed at a temperature of between about 400°C to about 600°C to form cobalt silicide.

30 FIG. 11A is a top down view of the semiconductor structure 101 after first slots 178 are formed between the cell plugs 158, each of which is shown in broken

-15-

lines for the purpose of illustrating the underlying structure. FIG. 11B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 11A taken along the section line 11-11 therein. After forming the contacts 140, a first fill material may be deposited over the peripheral region 181 of the semiconductor structure 101 to form a dielectric rim 197. For example, the first fill material may be an oxide material that is deposited over the semiconductor structure 101 using a conventional process, such as a chemical vapor deposition (CVD) process or a physical vapor deposition (PVD) process. A chemical-mechanical polishing (CMP) process may then be used to remove portions of the oxide material overlying the mask material 176 so that exposed surfaces of the dielectric rim 197 and the mask material 176 are substantially coplanar.

As shown in FIG. 11B, a portion of each of the mask material 176 and the cell stack 170 may be removed to form the first slots 178. As a non-limiting example, the mask material 176 (FIG. 9) may be patterned by providing a photoresist material (not shown) over the mask material 176 and removing portions of the mask material 176 overlying regions of the cell stack 170 that are to be removed (e.g., regions of the cell stack 170 that do not overlie the cell plugs 158). An anisotropic etching process (e.g., a dry reactive ion or plasma etching process) then may be used to etch the regions of the mask material 176 (FIG. 9) exposed through the photoresist material to form openings (not shown) that expose regions of the second region 174c. The photoresist material may then be removed using a conventional ashing process.

After removing the portions of the mask material 176, portions of the second region 174c exposed through the mask material 176 may be selectively removed with respect to the mask material 176 using methods such as those described with respect to FIG. 10B1. For example, if the second region 174c includes silicon dioxide, a reactive ion etching (RIE) process using a nitrogen trifluoride (NF₃)-based gas, a chlorine (Cl)-based gas or a bromide (Br)-based gas may be performed to selectively remove the silicon dioxide with respect to the mask material 176. After removing the portions of the second region 174c, portions of the first region 172c may be exposed through the mask material 176 and the second region 174c. The

-16-

exposed portions of the first region 172c may then be selectively removed with respect to the mask material 176. As a non-limiting example, if the first region 172c includes polysilicon, a reactive ion etching (RIE) process using a tetrafluoromethane (CF₄)-based plasma, hydrogen bromide (HBr)-based plasma or hydrochloric acid (HCl)-based plasma may be performed to remove the polysilicon with respect to the mask material 176. The second regions 174b and 174a and the first regions 172b and 172a may be alternately removed as described above to form the first slots 178 extending through the cell stack 170. The foundation material 168 underlying the cell stack 170 may be used as an etch stop during removal of the overlying first region 172a. For example, the remaining portion of the foundation material 168 exposed during the formation of the first slots 178 may have a thickness of about 30 nm.

The first slots 178 may be defined by sidewalls 180 that are perpendicular with the substrate 108 or, alternatively, may taper inward as they extend toward the substrate 108. Optionally, only a selected amount of the foundation material region 168 overlying the MOSFET array 106, if any at all, is removed during the removal of the first first region 172a.

As shown in FIGS. 12A and 12B, exposed portions of the first regions 172a, 172b and 172c (FIGS. 11A and 11B) within the first slots 178 may be doped with a desired concentration of a dopant to form the first doped regions 122. FIG. 12B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 12A taken along the section line 12-12 therein. Exposed portions of the first regions 172a, 172b and 172c may be doped using conventional methods, such as an ion implantation process or a high temperature diffusion process. For example, if the first regions 172a, 172b and 172c include polysilicon, the semiconductor structure 101 may be exposed to a boron- or an aluminum-containing plasma such that a p-type polysilicon is formed. As another example, a thin layer of a p-type material (not shown) may be deposited over surfaces of the semiconductor structure 101 and a thermal anneal may be performed during which p-type dopants migrate into the first regions 172a, 172b and 172c such that the first doped regions 122 include p-type polysilicon.

-17-

Referring to FIGS. 13A and 13B, exposed portions of the first doped regions 122 may be converted to a silicide to form the silicide regions 126. FIG. 13B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 13A taken along section line 13-13 therein. In some embodiments, the silicide regions 126 and contacts 140 may be formed by depositing a non-transition metal, such as cobalt, titanium, tungsten or nickel, over the first doped regions 122 (FIGS. 12A and 12B) and heating to temperature sufficient to cause the non-transition metal to react with the first doped regions 122, forming the silicide regions 126 and the contacts 140. For example, if the first doped regions 122 include a p-type polysilicon, cobalt may be deposited into the p-type polysilicon and annealed at a temperature of between about 400°C to about 600°C to form cobalt silicide. Alternatively, the first doped regions 122 may be undercut using a conventional etchant, such as a mixture of chloropentane (C_2ClF_5) and sulfur hexafluoride (SF_6). A metal may then be deposited in the undercut region (not shown) and annealed using conventional methods to form the silicide regions 126 and the contacts 140.

As shown in FIGS. 14A and 14B, another fill material may be deposited in the first slots 178 to form dielectric studs 196. FIG. 14B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 14A taken along section line 14-14 therein. For example, the fill material may be an oxide material that is deposited over the semiconductor structure 101 using a conventional process, such as a chemical vapor deposition (CVD) process or a physical vapor deposition (PVD) process. A chemical-mechanical polishing (CMP) process may then be used to remove portions of the oxide material overlying the mask material 176 so that an upper surface of the semiconductor device 101 is substantially planar.

As shown in FIGS. 15A and 15B, the mask material 176 may be removed from the semiconductor structure 101, exposing surfaces of remaining portions of the second region 174c. The mask material 176 may be removed using a conventional wet etching process that selectively removes the mask material 176 with respect to the dielectric studs 196, the dielectric rim 197 and remaining portions of the second region 174c. For example, if the mask material 176 is a nitride

-18-

material, a phosphoric acid (H_3PO_4) etchant having a temperature of between about 140°C and about 150°C may be applied to remove the nitride material from the semiconductor structure 101. FIG. 15B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 15A taken along section line 15-15 therein. As shown in FIG. 15B, after removing the mask material 176, portions of the dielectric studs 196 and the dielectric rim 197 protrude above exposed surfaces 198 of the second region 174c and have a height about equal to a thickness of the mask material 176 (i.e., between about 80 nm to about 200 nm and, more particularly, about 120 nm).

Referring to FIGS. 16A and 16B, spacers 200 may be formed on exposed sidewalls of the dielectric studs 196 and a sidewall of the dielectric rim 197 using a conventional spacer etching process. FIG. 16B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 16A taken along section line 16-16 therein. A base of each of the spacers 200 abutting the second regions 174c may have a width W sufficient to substantially cover the underlying first doped regions 122 such as, for example, from about 35 nm to about 100 nm. The spacers 200 may be formed from a hard mask material, such as, for example, tungsten, titanium nitride (TiN_2) or tungsten silicide. For example, tungsten having a substantially conformal thickness may be formed over the exposed surfaces of the second region 174c and the dielectric studs 196 and the dielectric rim 197, and a reactive ion etching (RIE) process using chlorine (Cl_2) as an etchant may be used to form the spacers 200.

As shown in FIG. 17, a first liner 202 may be deposited over the surface of the semiconductor structure 101, followed by deposition of a sacrificial material 204 over the first liner 202. The first liner 202 may be formed from a material that is resistant to an etchant capable of etching the sacrificial material 204 and the spacers 200 such as, for example, silicon nitride or tantalum nitride (TaN). The first liner 202 may be deposited to a thickness of between about 5 nm to about 10 nm using a conventional chemical vapor deposition (CVD) process. The sacrificial material 204 may be an oxide material, such as, silicon dioxide. The sacrificial material 204 may be deposited to a thickness sufficient such that a gap 206 between

portions of the sacrificial material 204 covering protruding regions of the dielectric studs 196 and the dielectric rim 197 is about 50 nm. For example, the sacrificial material 204 may be deposited to a thickness of from about 25 nm to about 35 nm using a conventional chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process.

As shown in FIGS. 18A and 18B, another mask material 208 may be formed over the sacrificial material 204 and may be patterned to include openings 210 that expose portions of the sacrificial material 204 between each of the dielectric studs 196 and overlying the cell plugs 158. For the purposes of illustrating the underlying structure, the dielectric studs 196 and the cell plugs 158 are shown in broken lines in FIG. 18A. The mask material 208 may include, for example, a photoresist material, transparent carbon or amorphous carbon, methods for forming that are known in the art. FIG. 18B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 18A taken along section line 18-18 therein. As shown in FIG. 18B, the mask material 208 has been formed over protruding portions of the sacrificial material 204 overlying dielectric studs 196, while the openings 210 expose portions of the sacrificial material 204 in the recesses positioned above the cell plugs 158.

FIG. 19A is a top down view of the semiconductor structure 101 after a plurality of second slots 212 have been formed therein. The underlying cell plugs 158 and the underlying dielectric studs 196 are shown in broken lines in FIG. 19A for the purposes of illustrating the underlying structure. FIG. 19B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 19A taken along section line 19-19 therein. Each of the second slots 212 may circumscribe one of the dielectric studs 196 and may be positioned over one of the cell plugs 158. To form the second slots 212, portions of the sacrificial material 204, the first liner 202, the second regions 174c, 174b and 174a and the first regions 172c, 172b and 172a overlying the cell plugs 158 may be removed through the openings 210 in the mask material 208. For example, a dry (i.e., plasma) etching process may be used to remove the sacrificial material 204 and the first liner 202 selective to the mask material 208. The processing parameters for such a dry etching process will depend

-20-

upon the compositions of the sacrificial material 204 and the first liner 202 selective to the mask material 208, and various anisotropic plasma etching processes are known in the art for etching many dielectric materials. The second regions 174c, 174b and 174a and the first regions 172c, 172b and 172a may be respectively
5 removed with respect to the mask material 208 using methods such as those described with respect to FIGS. 10B1 and 10B2 to expose a portion of the foundation material 168. The mask material 208 may be removed after forming the second slots 212.

FIG. 20 shows the semiconductor structure 101 after formation of the second
10 doped regions 124. The second doped regions 124 may be formed by doping portions of the first regions 172a, 172b and 172c exposed within the second slots 212 with a desired concentration of a dopant. The second doped regions 124 may be formed by a conventional process, such as an ion implantation process or a high temperature diffusion process. For example, the second doped regions 124 may
15 be formed by a plasma doping process, often referred to as a PLAD process, during which a desired dopant is ionized in an ion source, the resultant ions are accelerated to form an ion beam of prescribed energy, and the ion beam is then directed at a surface of a material, such as polysilicon, so that the ions penetrate into the material. As a non-limiting example, if the first regions 172a, 172b and 172c are polysilicon, a
20 PLAD process may be used to implant phosphorous or arsenic such that the second doped regions 124 comprise n-type polysilicon. As another example, a thin layer of a n-type material may be deposited over surfaces of the semiconductor structure 101 and a thermal anneal may be performed during which n-type dopants migrate into the first regions 172a, 172b and 172c such that the second doped regions 124 include
25 n-type polysilicon.

After forming the second doped regions 124, a second liner 214 may be formed over exposed sidewalls of the second slots 212 and the remaining portion of the second slots 212 may be filled with a polysilicon material to form sacrificial plugs 216, as shown in FIGS. 21A and 21B. FIG. 21B is a cross-sectional view of
30 the semiconductor structure 101 shown in FIG. 21A taken along section line 21-21 therein. The second liner 214 may be formed from a material that prevents

-21-

migration of dopants from the second doped regions 124 into the sacrificial plugs 216, such as, for example, a nitride material or an oxide material, and may be deposited using a conventional chemical vapor deposition (CVD) process. As a non-limiting example, the second liner 214 may have a thickness of between about 3
5 nm to about 8 nm. The sacrificial plugs 216 may be formed by depositing polysilicon using, for example, a conventional chemical vapor deposition (CVD) process or physical vapor deposition (PVD) process followed by an anisotropic dry reactive ion (i.e., plasma) etching process to recess the sacrificial plugs 216 within the second slots 212. The sacrificial material 204 and the first liner 202 may prevent
10 material from being deposited outside of the second slots 212, such as on surfaces of the second region 174c, during deposition of polysilicon to form the sacrificial plugs 216.

As shown in FIG. 22, the sacrificial material 204 may be removed to expose the first liner 202 using a conventional etching process that selectively removes the
15 sacrificial material 204. As a non-limiting example, if the sacrificial material 204 is an oxide material and the first liner 202 and the second liner 214 are a nitride material, a wet etchant including aqueous hydrochloric acid may be introduced to the semiconductor structure 101 to selectively remove the oxide material with respect to the nitride material.

Referring to FIGS. 23A and 23B, after removing the sacrificial material 204, a third mask material 218 may be deposited and patterned to cover a portion of the peripheral region 181 of the semiconductor structure 101 and portions of the sacrificial plugs 216 overlying the cell plugs 158 (broken lines). Portions of the spacers 200, the sacrificial plugs 216, and the cell plugs 158 underlying the mask
25 material 218 are shown in broken lines in FIG. 23A for the purposes of illustrating the underlying structure. FIG. 23B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 23A taken long section line 23-23 therein.

FIG. 24A is a top down view of the semiconductor structure 101 after the material exposed through the mask material 218 and the spacers 200 has been
30 removed. For the purposes of illustrating the underlying structure, the cell plugs 158 are shown in broken lines in FIG. 24A. FIG. 24B is a cross-sectional view of the

-22-

semiconductor structure 101 shown in FIG. 24A taken along section line 24-24 therein. For example, the first liner 202 may be silicon nitride and exposed portions thereof may be removed using an anisotropic reactive ion (i.e., plasma) etching process. The sacrificial plugs 216 may be removed using, for example, a reactive ion etching (RIE) process. After removing the sacrificial plugs 216, the second liner 214 may be removed using an anisotropic reactive ion (i.e., plasma) etching process. The second regions 174a, 174b and 174c and the second doped regions 124 may be alternately removed using methods such as those described above with respect to FIGS. 10B1 and 10B2 to expose underlying portions of the foundation material 168. At least a portion of the dielectric studs 196 may also be removed to form a plurality of pillars 220. In FIG. 24A, the cell plugs 158, remaining portions of the spacers 200 and remaining portions of the sacrificial plugs 216 (i.e., portions of the sacrificial plugs 216 overlying the cell plugs 158) are shown in broken lines for the purposes of illustrating the underlying structure. Portions of the second doped regions (not shown) between the cell plugs 158 have been removed to singulate the second doped regions overlying each of the cell plugs 158.

Referring to FIGS. 25A and 25B, FIG. 25B being a cross-sectional view of the semiconductor structure 101 shown in FIG. 25A taken along the section line 25-25 therein, the mask material 218 may be removed to expose the spacers 200 and remaining portions of the first liner 202 overlying the peripheral region 181. For example, the mask material 218 may be removed using a conventional ashing process or a wet etching process using a mixture of ammonium hydroxide (NH_4OH), hydrogen peroxide (H_2O_2) and water (H_2O).

FIGS. 26A and 26B, show the semiconductor structure 101 after the spacers 200 and remaining portions of the first liner 202 have been removed. FIG. 26B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 26A, a portion 203a of which is taken along the section line 26'-26' bisecting the cell plugs 158, and another portion 203b of which is taken along section line 26''-26'' extending between the cell plugs 158. The second region 174c has been omitted from the portion 203a for the purposes of illustrating the underlying structure. As a non-limiting example, if the spacers 200 include tungsten, a

-23-

conventional wet etching process using a mixture of hydrofluoric acid (HF) and nitric acid (HNO₃) may be used to remove the tungsten. As shown in FIG. 26A, the sacrificial plugs 216 are positioned over the cell plugs 158, each of which is shown in broken lines. The pillars 220 are disposed between remaining portions of the dielectric studs 196 and the foundation material 168. The second doped regions 124
5 extend along the sacrificial plugs 216. The first doped regions 122 and the silicide regions 126 circumscribe the fill material 196 in the first slots 178. The intrinsic regions 120 are each disposed between one of the first doped regions 122 and one of the second doped regions 124 to form the diodes 104 between each of the underlying
10 cell plugs 158 (broken lines).

FIGS. 27A and 27B show the semiconductor structure 101 after an upper surface thereof has been planarized and a lower dielectric material 222, a third liner 224, and an intermediate dielectric material 226 have been deposited thereover. FIG. 27B is a cross-sectional view of the semiconductor structure shown in
15 FIG. 27A taken along section line 27-27 therein. The upper surface of the semiconductor structure 101 may be planarized using a chemical-mechanical polishing (CMP) process. The lower dielectric material 222 may include, for example, an oxide material. The lower dielectric material 222 may be deposited over the semiconductor structure 101 to fill recesses therein and may then be
20 planarized using, for example, a chemical-mechanical polishing (CMP) process such that the upper surface of the lower dielectric material 222 is substantially planar. The third liner 224 may include a material capable of being selectively etched with respect to the lower dielectric material 222 and may have a thickness of between about 10 nm and about 30 nm. For example, if the lower dielectric material 222 is
25 silicon dioxide, the third liner 224 may include silicon nitride. The intermediate dielectric material 226 may then be formed over the third liner 224. As a non-limiting example, the intermediate dielectric material 226 may include an oxide material. The lower dielectric material 222, the third liner 224 and the intermediate dielectric material 226 may each be formed using a conventional deposition process
30 such as, for example, a chemical vapor deposition (CVD) process.

-24-

As shown in FIGS. 28A and 28B, line interconnects 142 may be formed, each of which extends through the intermediate dielectric material 226, the third liner 224 and lower dielectric material 222 to one of the contacts 140. FIG. 28B is a cross-sectional view of the semiconductor structure shown in FIG. 28A taken along section line 28-28 therein. The sacrificial plugs 216 and the cell plugs 158 are shown in broken lines in FIG. 28A for the purposes of illustrating the underlying structure. Each of the line interconnects 142 may be formed using conventional lithographic processes. For example, a photoresist (not shown) may be formed over the semiconductor structure 101 and patterned to include apertures (not shown) therein, each of the apertures overlying a location at which it is desired to form one of the line interconnects 142. Portions of the intermediate dielectric material 226, the third liner 224 and the fill material 196 may be removed through each of the apertures using, for example, a conventional anisotropic reactive ion (i.e., plasma) etching process, to expose a surface of the underlying contacts 140. The photoresist may be removed and a conductive material, such as tungsten, aluminum, or copper, may be deposited using a conventional chemical vapor deposition (CVD) process and may be etched back using a conventional chemical mechanical polishing (CMP) process to form the line interconnects 142.

As shown in FIGS. 29A and 29B, the metal lines 144 may be formed over and in contact with the line interconnects 142. FIG. 29B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 29A taken along section line 29-29 therein. The sacrificial plugs 216 and the cell plugs 158 are shown in broken lines in FIG. 29A for the purposes of illustrating the underlying structure. To form the metal lines 144, an upper dielectric material 228 may be formed over a surface of the intermediate dielectric material 226 and exposed surfaces of the line interconnects 142. The metal lines 144, each electrically coupled to one of the line interconnects 142 may be formed using conventional lithographic processes. For example, a photoresist (not shown) may be formed over the upper dielectric material 228 and apertures (not shown) may be formed therein, each aperture overlying one of the line interconnects 142. A portion of the upper dielectric material 228 may be removed through the apertures to form openings, each exposing

a surface of the underlying line interconnect 142. The openings may be filled with metal using a conventional chemical vapor deposition (CVD) process and may be etched back using a conventional chemical mechanical polishing (CMP) process to form the metal lines 144.

5 The passivation material 146 may, optionally, be formed over the semiconductor structure 101 and portions of the passivation material 146, the upper dielectric material 228, the intermediate dielectric material 226, and the third liner 224 may be removed, as shown in FIGS. 30A and 30B. FIG. 30B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 30A taken
10 along section line 30-30 therein. The cell plugs 158 are shown in broken lines in FIG. 30A for the purposes of illustrating the underlying structure. The passivation material 146 may be formed and patterned to cover the peripheral region 181 of the semiconductor structure 101 using conventional lithographic processes. Portions of the passivation material 146, the upper dielectric material 228, the intermediate
15 dielectric material 226 and the third liner 224 may be removed with respect to the passivation material 146 and the third liner 224 using a conventional anisotropic reactive ion (i.e., plasma) etching process. Portions of the third liner 224 exposed through the passivation material 146 may then be removed to expose surfaces of the fill material 196, the lower dielectric material 222 and the sacrificial plugs 216.

20 Referring to FIGS. 31A and 31B, the sacrificial plugs 216 and the second liner 214 may be removed from the semiconductor structure 101 to expose sidewalls of the second slots 212. FIG. 31B is a cross-sectional view of the semiconductor structure 101 shown in FIG. 31A taken along section line 31-31 therein. The cell plugs 158 are shown in broken lines in FIG. 30A for the purposes of illustrating the
25 underlying structure. As a non-limiting example, the sacrificial plugs 216 may be removed selective to the second liner 214 using an anisotropic etching process (e.g., a dry reactive ion or plasma etching process). As a non-limiting example, if the sacrificial plugs 216 are polysilicon and the second liner 214 is a nitride material, a tetramethylammonium hydroxide (TMAH) etchant may be introduced to the
30 semiconductor structure 101 to selectively remove the polysilicon without removing the nitride material. The second liner 214 may then be removed using a

-26-

conventional anisotropic etching process (e.g., a dry reactive ion or plasma etching process) to expose portions of the second doped regions 124, the second regions 174a, 174b and 174c and the foundation material 168 defining the second slots 212.

5 FIGS. 32A and 32B show the semiconductor structure 101 after formation of the barrier material 128 and the sidewall spacers 130. FIG. 32B is a cross-sectional view of the semiconductor shown in FIG. 32A taken along section line 32-32, which bisects the cell plugs 158. As a non-limiting example, the barrier material 128 may include a dielectric such as an oxide material or a nitride material. The barrier
10 material 128 may be formed over the exposed portions of the second doped region 124 using a conventional chemical vapor deposition (CVD) process or oxidation process. The sidewall spacers 130 may be formed from, for example, a metal or a ceramic material, such as titanium nitride (TiN), titanium (Ti) or platinum (Pt). The sidewall spacers 130 may be formed over the sidewalls of the second
15 slots 212 using a conventional chemical vapor deposition (CVD) process. The sidewalls spacers 130 may include a material that substantially reduces diffusion of metals into the second doped regions 124. After forming the sidewall spacers 130, an etching process (e.g., an anisotropic dry reactive ion or plasma etching process) may be used to etch through the foundation material 168 exposing underlying
20 portions of the cell plugs 158. A conductive material such as, for example, tungsten, may be deposited to fill remaining portions of the second slots using a conventional chemical vapor deposition (CVD) process and etched back to form the electrodes 110, each of which is electrically coupled to one of the cell plugs 158 as shown in FIGS. 1A and 1B. Two memory strings 102 may be electrically coupled to
25 each of the nodes at intersecting points of the bit lines 162 and the column lines 160. As shown in FIG. 1A, each of the electrodes 110 effectively forms a dual-node having diodes 104 on opposite sides thereof.

 Another embodiment of a memory device 300 is shown in FIGS. 33A and 33B. The memory device 300 may be, for example, a resistive random access
30 memory (RRAM) device that includes another silicide region 302 and a memory element 304 disposed between the electrode 110 and the diodes 104 of each memory

-27-

string 102. An embodiment of a method that may be used to form the memory device 300 is described below with reference to FIGS. 34-36.

As shown in FIG. 34, a semiconductor structure 301 including a plurality of vertically superimposed diodes 104 overlying a conventional MOSFET array 106
5 disposed on a substrate 108 may be formed in the manner previously described with reference to FIGS. 4A-31B. A conventional anisotropic reactive ion etching process may be performed to remove an exposed portion of each of the second doped regions 124 forming a plurality of recesses 306 therein.

Referring to FIG. 35, the another silicide region 302 may be deposited in the
10 recesses 306 (FIG. 34) in each of the second doped regions 124. As a non-limiting example, the another silicide region 302 may include cobalt silicide (CoSi_2), titanium silicide (TiSi_2), tungsten silicide (TiSi_2) or nickel silicide (NiSi_2) and may be deposited using a conventional chemical vapor deposition (CVD) process.

As shown in FIG. 36, a memory element 304 and the sidewall spacer 130
15 may be formed over each of the sidewalls of the second slots 212. The memory element 304 may include a dielectric material such as, for example, and oxide material or a nitride material. The memory element 304 may be formed using, for example, a conventional chemical vapor deposition (CVD) process. The sidewall spacer 130 may include titanium oxide (TiO_2), copper oxide (Cu_xO_y), tungsten oxide
20 (W_xO_y), nickel oxide (Ni_xO_y) or gallium oxide (Ga_2O_3) and may be formed using methods such as those described with respect to FIGS. 32A and 32B. After forming the memory element 304 and the sidewall spacer 130 over each of the sidewalls, an exposed region of the foundation material 168 may be removed using an etchant that selectively etches away the foundation material 168 selective to the memory
25 element 304 and the sidewall spacer 130. For example, the foundation material 168 may be removed using a conventional anisotropic dry reactive ion or plasma etching process to expose a portion of each of the underlying cell plugs 158. Contact plugs 132 that include, for example, tungsten, may then formed in remaining portions of the second slots 212 over the sidewall spacers 130 using a conventional
30 chemical vapor deposition (CVD) process to form the memory device 300 shown in FIGS. 33A and 33B.

-28-

Another embodiment of a memory device 400 is shown in FIGS. 37A and 37B. FIG. 37B is a cross-sectional view of the memory device 400 shown in FIG. 37A taken along section line 37-37 therein. The memory device 400 may be, for example, a phase-change random access memory (PCRAM) device that includes
5 the another silicide 302 and a phase change material 402 disposed between the diodes 104 and the contact plugs 132 of the at least one memory string 102. An embodiment of a method that may be used to form the memory device 400 is described below with reference to FIGS. 38 and 39.

As shown in FIG. 38, a semiconductor structure 401 may be formed in the
10 manner previously described with reference to FIGS. 4A-31B and a conventional anisotropic reactive ion etching process may be performed to form the recesses 306 in the second doped regions 124.

Referring to FIG. 39, a phase change material 402 may be formed over the sidewalls exposed within each of the second slots 212. The phase change
15 material 402 may also be deposited on sidewalls of the passivation material 146, the upper dielectric material 228 and the intermediate dielectric material 226. As a non-limiting example, the phase change material 402 may include a chalcogenide such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ (GST). The phase change material 402 may be deposited using, for example, a conventional sputtering process. After forming the phase change
20 material 402 over each of the sidewalls, an exposed region of the foundation material 168 may be removed using an etchant that etches away the foundation material 168 selective to the phase change material 402. For example, the foundation material 168 may be removed using a conventional anisotropic dry reactive ion or plasma etching process to expose a portion of each of the underlying
25 cell plugs 158.

Contact plugs 132 may then be formed in remaining portions of the second slots 212 to form the memory device 400 as shown in FIGS. 37A and 37B. As a non-limiting example, the contact plugs 132 may include a conductive material such as, for example, tungsten. The contact plugs 132 may be formed by depositing the
30 conductive material using a conventional chemical vapor deposition (CVD) process and then etching the conductive material back.

-29-

Although the vertically superimposed diodes 104 are shown herein as part of vertical non-volatile memory devices, they may also be utilized in various other memory applications as will be recognized by one of ordinary skill in the art. The memory strings 102 each include two diodes 104 per cell and, thus, provide a higher density arrangement of diodes 104 that may be easily integrated with existing devices. By using a conventional MOSFET device as an address selector, memory devices including the vertically superimposed diodes 104 provide a substantially increased I_{off} . The methods of forming the vertically superimposed diodes 104 as described above enable formation of temperature-sensitive elements, such as, phase change materials, as a final act after completion of processes requiring increased temperatures. The arrangement of diodes 104 described herein provides increased memory density at a reduced cost.

In view of the above description, some embodiments of the present invention include a non-volatile memory device that includes an electrode and at least one memory string disposed over a substrate and including a plurality of diodes arranged at different locations along a length of the electrode. The electrode may include, for example, a metal contact plug having at least one of a metal or a ceramic material disposed on opposite sides or, alternatively, a phase change material. Each of the plurality of diodes may include an intrinsic region disposed between a p-type doped region and an n-type doped region. The p-type doped region, the n-type region, and the intrinsic region may extend along a length of the substrate substantially perpendicular to the length of the electrode. The at least one memory string is disposed on a memory device comprising a plurality of memory cells and may be electrically coupled thereto by the electrode.

Additional embodiments of the present invention include an intermediate semiconductor structure that includes a plurality of diodes overlying a substrate and vertically superimposed over one another in a plurality of columns, each of the plurality of diodes being spaced apart from one another by a dielectric material. The plurality of diodes may be disposed on a plurality of memory cells, each of which is electrically coupled to a cell plug. At least one of the plurality of columns may at least partially overlie a portion of the cell plug.

-30-

Further embodiments include methods of fabricating a semiconductor structure. A plurality of alternating first regions and second regions may be deposited over a foundation material overlying a transistor array to form a cell stack, the transistor array comprising a plurality of transistors, each of which is electrically coupled to a cell plug. Portions of the cell stack exposed through a mask may be removed to form a plurality of first slots, each of which at least partially overlies the cell plug. A dopant may be introduced to exposed portions of the first regions to form a plurality of p-type doped regions and a silicide material may be deposited over each of the plurality of p-type doped regions. A fill material may be deposited over the semiconductor structure to at least fill the plurality of first slots. Portions of the cell stack exposed through another mask may form a plurality of second slots laterally spaced apart from each of the plurality of first slots. Exposed portions of the first regions may be introduced to a dopant to form a plurality of n-type doped regions, an intrinsic region disposed between the plurality of n-type doped regions and the plurality of p-type doped regions.

While the present invention has been described in terms of certain illustrated embodiments and variations thereof, it will be understood and appreciated by those of ordinary skill in the art that the invention is not so limited. Rather, additions, deletions and modifications to the illustrated embodiments may be effected without departing from scope of the invention as defined by the claims that follow, and their legal equivalents.

-31-

CLAIMS

What is claimed is:

- 5 1. A non-volatile memory device, comprising:
a plurality of transistors disposed on a substrate, each transistor of the plurality of
transistors electrically coupled to a word line and a bit line, the word line and
the bit line intersecting one another at at least one node;
a plurality of memory strings disposed over the plurality of memory cells, each
10 comprising a plurality of diodes; and
an electrode electrically connecting at least two of the plurality of memory strings to
the at least one node, the plurality of diodes arranged at locations spaced
along a length of the electrode.
- 15 2. The non-volatile memory device of claim 1, wherein the electrode
comprises a metal contact plug having at least one of a metal or a ceramic material
disposed on sidewalls thereof.
- 20 3. The non-volatile memory device of claim 1, wherein the electrode
comprises a phase change material.
- 25 4. The non-volatile memory device of claim 1, wherein each of the
plurality of memory strings further comprises at least one barrier material disposed
between the plurality of diodes and the electrode.
- 30 5. The non-volatile memory device of claim 1, wherein each of the
plurality of diodes comprises an intrinsic region disposed between oppositely doped
regions, the intrinsic region and the oppositely doped regions extending
perpendicular to a major plane of the substrate.

6. The non-volatile memory device of claim 1, wherein the plurality of diodes are aligned in a first direction to form a plurality of columns and are aligned in a second direction substantially perpendicular the first direction to form a plurality of rows.

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7. A semiconductor structure comprising a plurality of diodes overlying a substrate and vertically superimposed over one another to form a plurality of columns, each of the plurality of diodes comprising an intrinsic region disposed between oppositely doped regions, the plurality of diodes of adjacent columns being mirror images of one another.

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8. The semiconductor structure of claim 7, further comprising an electrode disposed between at least two of the plurality of columns.

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9. The semiconductor structure of claim 7, further comprising a transistor array underlying the plurality of diodes and comprising a plurality of transistors, each of the plurality of transistors disposed between a source region and a drain region in the substrate and electrically coupled to a cell plug.

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10. The semiconductor structure of claim 7, wherein each of the plurality of diodes in one of the plurality of columns is substantially horizontally aligned with each of the plurality of diodes in another of the plurality of columns.

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11. The semiconductor structure of claim 7, wherein at least one of the oppositely doped regions and the intrinsic region extend along a length of the substrate in a direction substantially perpendicular to the plurality of columns.

-33-

12. A method of forming a semiconductor structure, comprising:
forming a plurality of alternating first regions and second regions to form a cell stack
over a foundation material overlying a transistor array, the transistor array
comprising a plurality of transistors electrically coupled to a plurality of cell
5 plugs;
removing portions of the first regions and second regions exposed through a mask to
form a plurality of first slots therethrough, each of the plurality of first slots
overlying one of the plurality of cell plugs;
introducing a dopant to exposed portions of the first regions to form a plurality of
10 first doped regions;
forming a silicide material over each of the plurality of first doped regions;
forming a fill material over the semiconductor structure to at least fill the plurality of
first slots;
removing portions of the first regions and second regions exposed through another
15 mask to form a plurality of second slots laterally spaced apart from each of
the plurality of first slots; and
introducing a dopant to exposed portions of the first regions to form a plurality of
second doped regions, an intrinsic region of the first region disposed between
the plurality of second doped regions and the plurality of first doped regions.
20
13. The method of claim 12, wherein forming a plurality of alternating
first regions and second regions to form a cell stack over a foundation material
overlying a transistor array comprises:
attaching a wafer comprising crystalline silicon to the foundation material; and
25 separating a portion of the wafer to leave a first semiconductive region overlying the
foundation material.

-34-

14. The method of claim 12, wherein removing portions of the first regions and second regions exposed through another mask to form a plurality of second slots comprises:

forming spacers on protruding regions of the fill material;

5 forming at least one material over the spacers, the at least one material having a plurality of openings exposing portions of the cell stack between the first slots; and

removing the exposed portion of the cell stack to form the plurality of second slots.

10 15. The method of claim 14, wherein forming spacers on protruding regions of the fill material comprises forming the spacers having a width sufficient to overlie the first doped regions.

15 16. The method of claim 12, wherein removing portions of the first regions and second regions exposed through another mask to form a plurality of second slots comprises removing portions of the first regions and second regions exposed through the another mask to form the plurality of second slots, each of which circumscribes at least one of the plurality of first slots.

20 17. The method of claim 12, further comprising removing portions of the first regions and second regions to form a plurality of tiers in a peripheral region of the cell stack, each of the plurality of tiers comprising an exposed surface of one of the plurality of first regions.

25 18. The method of claim 17, further comprising:
introducing a dopant to exposed portions of the first regions on the plurality of tiers to form doped material; and
converting at least a portion of the doped material to a silicide material to form contacts.

30

-35-

19. The method of claim 12, further comprising forming at least one of a ceramic material, a conductive material, and a phase change material over sidewalls defining the plurality of second slots.

5 20. The method of claim 12, further comprising removing a portion of the foundation material to expose surfaces of the plurality of cell plugs.