

VOLTAGE REGULATOR AND CONSTANTCURRENT CIRCUITS

The present invention relates generally to voltage regulator and constant current circuits and more particularly to such circuits which can suppress fluctuations of its output voltage.

Japanese Published Patent Gazette No. 53-18694 (corresponding to Japanese Laid-Open Patent Application Gazette No. 46-3527) or the like discloses a voltage regulator circuit in which a reference voltage is set to be equal to an energy gap voltage (1.205 V) of silicon so as to reduce a temperature coefficient to zero. Fig. 1 illustrates an example of such a conventional voltage regulator circuit. This conventional voltage regulator circuit will be described hereinafter with reference to Fig. 1.

As Fig. 1 shows, there is provided a transistor 11 of which the collector and base are both connected to a base of a transistor 12. The collector of the transistor 12 is connected to a base of a transistor 13. The emitters of both the transistors 11 and 13 are directly grounded and the emitter of the transistor 12 is grounded through a resistor 14. The collector of the transistor 13 is connected in common to a current source 15 and a base of a buffer transistor 16. The emitter of the transistor 16 and the collectors of the transistors 11 and 12 are connected together through resistors 17 and 18. The current source 15 and the collector of the transistor 16 are both connected to a voltage source terminal 1 (Vcc). An output terminal 2 is

led out from the emitter of the transistor 16.

As is well known, between a base-emitter voltage V_{BE} and a collector current I_C of a transistor, there is established a relationship expressed by the following equation (1) or (2).

$$I_C = I_S \cdot \exp \left(\frac{q}{kT} \cdot V_{BE} \right) \quad \dots (1)$$

$$V_{BE} = \frac{kT}{q} \cdot \ln \left(\frac{I_{C2}}{I_S} \right)$$

$$= V_T \ln \left(\frac{I_C}{I_S} \right) \quad \dots (2)$$

where I_S is the saturation current, q the electron charge, T the absolute temperature and k the Boltzman's constant.

In the known voltage regulator circuit shown in Fig. 1, I_{C1} and I_{C2} assume collector currents of the transistors 11 and 12, V_{BE1} and V_{BE2} assume base-emitter voltages thereof and R_{14} assumes a resistance value of the resistor 14. Then, the following equation (3) is established.

$$V_{BE1} = V_{BE2} + I_{C2}R_{14} \quad \dots (3)$$

Applying the equation (2) to the equation (3) yields the following equations (4a) and (4b)

$$V_T \ln \left(\frac{I_C}{I_S} \right) = V_T \ln \left(\frac{I_{C2}}{I_S} \right) + I_{C2}R_{14} \quad \dots (4a)$$

$$I_{C2} = \frac{V_T}{R_{14}} \ln \left(\frac{I_{C1}}{I_{C2}} \right) \quad \dots (4b)$$

If a base-emitter voltage of the transistor 13 is taken as V_{BE3} and a resistance value of the resistor 18 is taken as R_{18} , the reference voltage V_{REF} developed at the output terminal 2 is expressed as in the following equation (5) by utilizing the equation (4b).

$$V_{REF} = I_{C2} \cdot R_{18} + V_{BE3}$$

$$= \frac{R_{18}}{R_{14}} V_T \ln \left(\frac{I_{C1}}{I_{C2}} \right) + V_{BE3}$$

$$= K \cdot V_T + V_{BE3}$$

$$K \equiv \frac{R_{18}}{R_{14}} \cdot \ln \left(\frac{I_{C1}}{I_{C2}} \right) \quad \dots (5)$$

From the foregoing equation (2), it is thus apparent that V_T (thermal voltage) has a positive temperature coefficient of about 1/300. Meanwhile, the base-emitter voltage V_{BE3} of the transistor 13 fluctuates in the negative direction with a ratio of about -2 mV/°C. In the voltage regulator circuit shown in Fig. 1, by properly selecting the resistance value of the resistor 18, it is possible to balance the base-emitter voltage of negative temperature coefficient of the transistor 13 and the voltage of positive temperature coefficient produced across the resistor 18 due to the collector current of the transistor 12. Thus, as described above, it is possible to obtain the reference voltage V_{REF} of zero temperature coefficient equal to the energy-gap voltage of the silicon. If a voltage across the resistor 18 at that time is taken as $K_0 \cdot V_T$, V_T is nearly equal to 26 mV ($V_T \approx 26$ mV) so that K_0 becomes substantially equal to 23 ($K_0 \approx 23$).

A voltage regulator circuit mounted on the integrated circuit (IC) is required to have small fluctuation of the output voltage, in addition to the excellent temperature characteristic.

As will be clear from the equation (5), the output voltage from the conventional voltage regulator circuit

shown in Fig. 1 depends on the base-emitter voltage V_{BE} of the transistor 13. This base-emitter voltage V_{BE} is dependent on the saturation current I_s of the transistor 13 as will be apparent from the equation (2).

5 In the manufacturing process of the integrated circuit, however, if impurity concentration in the base of a transistor is fluctuated upward or downward, the saturation current I_s is decreased or increased dependent on this fluctuation, while on the contrary the base-emitter voltage
10 V_{BE} is increased or decreased.

As earlier noted, when the output constant voltage from the voltage regulator circuit is set to be $V_{REF} = 1.205V$, the fluctuation of the base-emitter voltage V_{BE} in the general manufacturing process reaches, for example, about $\pm$
15 40 mV, i.e., about $\pm 3.3\%$. For this reason, in order to control the output voltage to fall in a predetermined range, the administration of the manufacturing process must be made more strict and the trimming of the resistor or the like must be carried out.

20

25

30

According to the present invention, there is provided a voltage regulator circuit comprising:

- a) a first current source for generating a predetermined current;
- 5 b) a first transistor supplied to its base with the predetermined current from said first current source and for generating an emitter current which is β times as large as said predetermined current;
- 10 c) a second transistor having a collector connected to said emitter of said first transistor and of which the emitter is grounded;
- d) a second current source connected at its one end

to the base of said second transistor and one end of a resistor which generates a reference voltage; and

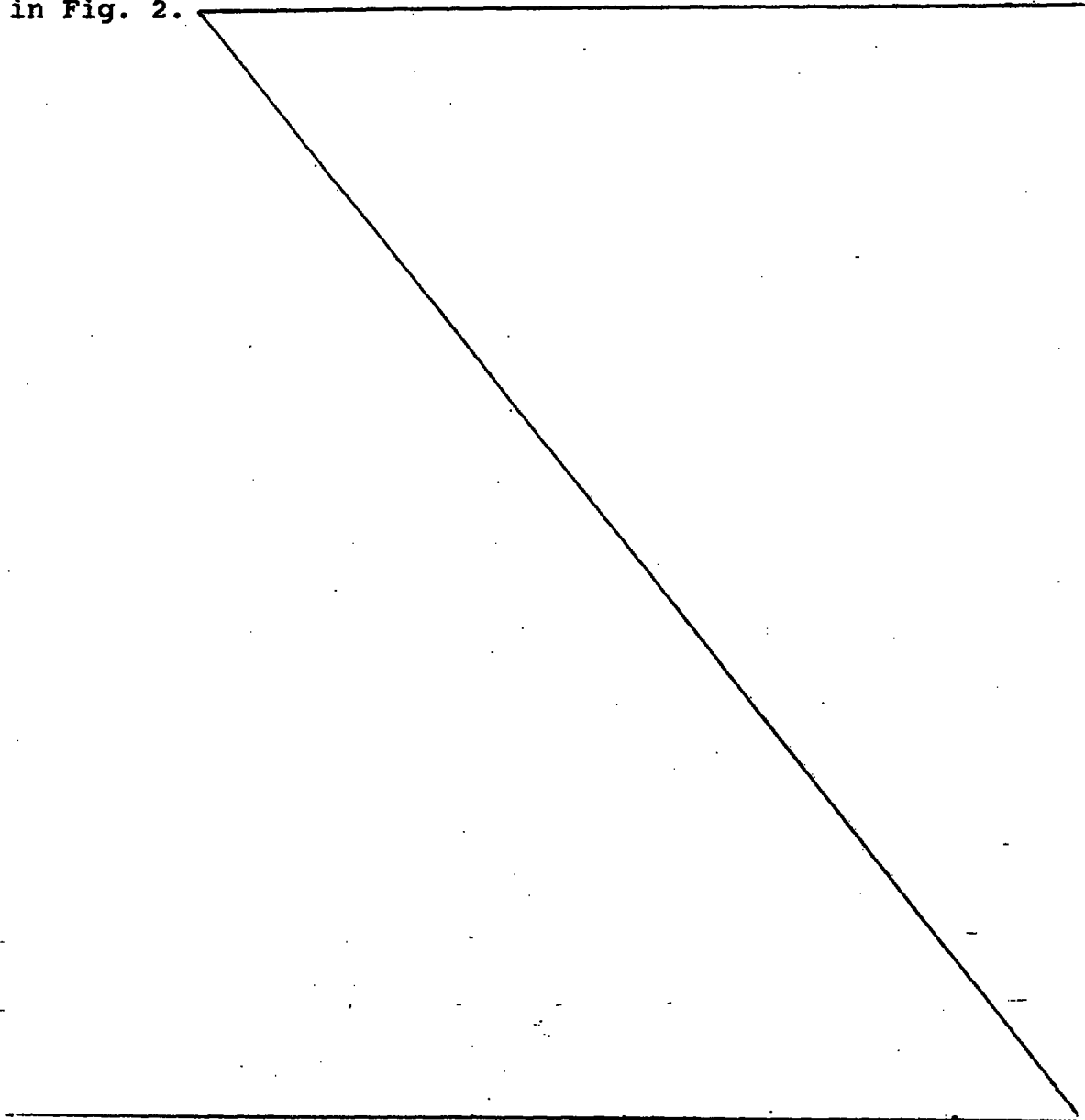
e) a buffer amplifier connected between the emitter of said first transistor and the other end of said resistor, 5 wherein a predetermined voltage is derived at the other end of said resistor.

The above and other features and advantages of the present invention will become apparent from the following detailed description of the preferred embodiments to be taken 10 in conjunction with the accompanying drawings, in which like reference numerals identify like elements and parts. In the drawings:-

Fig. 1 is a diagram showing an example of an arrangement of a conventional voltage regulator circuit;

Fig. 2 is a connection diagram showing a fundamental arrangement of an embodiment of a voltage regulator circuit
5 according to the present invention; and

Fig. 3 is a connection diagram showing a practical arrangement of the embodiment of the present invention shown in Fig. 2.



5 An embodiment of a voltage regulator circuit according to the present invention will now be described with reference to Figs. 2 and 3. Throughout the following embodiments of the present invention, the transistors are each bi-polar transistors. Fig. 2 illustrates a
10 fundamental arrangement of the embodiment of the present invention.

 As Fig. 2 shows, one end of a current source 21 is connected to a base of a transistor 22, and the other end of the current source 21 and the emitter of the transistor 22
15 are grounded. The collector of the transistor 22 is connected to an emitter of a second transistor 23, and the base of the transistor 23 is connected to one end of a second current source 24. The collector of the transistor 23 and the other end of the second current source 24 are
20 connected together to the voltage source 1 (V_{cc}). The junction between the collector of the transistor 22 and the emitter of the transistor 23 is connected to an input terminal of a buffer 27. The output terminal of the buffer 27 is directly connected to an output terminal 2 and is also
25 connected commonly through a resistor 28 to the current source 21 and the base of the transistor 22.

 The operation of the embodiment shown in Fig. 2 is as follows.

I_1 and I_2 are the currents that flow through the first
30 and second current sources 21 and 24, respectively. Also,

$\beta (>> 1)$ is the current amplification factor of each of the transistors 22 and 23. Then, the current I_2 is applied to the base of the transistor 23 so that the collector current of the transistor 23 becomes βI_2 and that the collector current of the transistor 22 connected to the transistor 23 in series also becomes βI_2 . To the base of the transistor 22, there is applied a current which is $1/\beta$ of the collector current, i.e. the current I_2 from the buffer 27 through the resistor 28. Accordingly, due to the constant current I_1 and the base current I_2 of the transistor 22, the voltage across the resistor 28 is presented as $(I_1 + I_2) R_{28}$ where R_{28} is the resistance value of the resistor 28.

In order that the output voltage V_0 derived from the terminal 2 becomes equal to the afore-mentioned energy-gap voltage V_{REF} in Fig. 2, the following relationship has to be established.

$$(I_1 + I_2) R_{28} = K_0 V_T$$

The currents I_1 and I_2 of the respective current sources 21 and 24 are expressed by the following equation

$$(6) \text{ where } K_0 = K_1 + K_2$$

$$\left. \begin{aligned} I_1 &= K_1 V_T / R_{28} \\ I_2 &= K_2 V_T / R_{28} \end{aligned} \right\} \dots (6)$$

How to determine the coefficients K_1 and K_2 will be described with reference to an example of a practical arrangement shown in Fig. 3.

The output voltage V_0 thus produced at the terminal 2 is expressed by the following equation (7).

$$V_0 = V_{REF} = K_0 V_T + V_{BE} (\beta I_2) \dots (7)$$

Although the base-emitter voltage V_{BE} of the transistor

22 depends on the saturation current I_S as will be from the equation (2), if the ratio between the current amplification factor β and the saturation current I_S is taken as A , since the correlation between the current amplification factor β and the saturation current I_S is approximately 1, $A = \beta/I_S$ becomes a constant value regardless of fluctuations of the base impurity concentration.

Thus, the equation (2) yields

$$V_{BE} = V_T \ln (A I_2) \quad \dots (8)$$

Therefore, the base-emitter voltage V_{BE} of the transistor 22 depends on a base current which is equal to the current I_2 of the second current source 24. As will be clear from the equation (6), although this current I_2 fluctuates in response to the fluctuation of the resistance value R_{28} of the resistor 28, the fluctuation of the resistance value R_{28} is as small as being negligible as compared with the fluctuation of the saturation current I_S so that according to this embodiment, the fluctuation of the base-emitter voltage V_{BE} of the transistor 22, and hence the fluctuation of the output voltage V_0 at the terminal 2 can be suppressed.

The practical arrangement of the embodiment shown in Fig. 2 will be described with reference to Fig. 3.

In Fig. 3, reference numeral 30 generally designates a constant current circuit. In the constant current circuit 30, as shown in Fig. 3, emitters of a pair of PNP transistors 31 and 32 are both connected to a voltage source terminal 1 (V_{CC}), and the bases thereof are coupled to each other. The collector of the transistor 32 is connected to

the base thereof, thus a so-called current mirror circuit configuration being established. The collector of the PNP transistor 31 and a collector of an NPN transistor 33 of which the emitter is grounded are coupled together and a collector of an NPN transistor 34 whose base is connected to the above junction P is connected to the collector of the PNP transistor 32.

A transistor 35_N is what might be called an NPN multi-emitter transistor in which the emitter thereof has an area N times as large as that of the transistor 33. In other words, the multi-emitter transistor 35_N has a current capacity N times as large as that of the transistor 33. The multi-emitters of the transistor 35_N are commonly connected and then grounded through a resistor 36. The collector of the transistor 35_N is connected to the emitter of the transistor 34 through a load resistor 37, while the base of the transistor 35_N is connected in common to the base of the transistor 33 and the emitter of the transistor 34.

A base of a transistor 41 is connected in common to the bases of the transistors 33 and 35_N in the constant current circuit 30. The collector of the transistor 41 is connected to a base of a transistor 42 and the emitters of both the transistors 41 and 42 are grounded. The collector of the transistor 42 and an emitter of a transistor 43 are connected to each other and the collector of the transistor 43 is connected to the voltage source terminal 1.

Emitters of a pair of PNP transistors 44 and 45 are connected to the voltage source terminal 1, the bases thereof are connected to each other and the collector of the transistor 45 is connected to the base thereof, thus forming

a current mirror circuit configuration. The collector of the PNP transistor 44 and the base of the NPN transistor 43 are connected together. A collector of an NPN transistor 46 with its emitter grounded is connected to the collector of the PNP transistor 45. The base of the transistor 46 is connected to the collector of the multi-emitter transistor 35_N in the constant current circuit 30.

To a junction Q between the collector of the transistor 42 and the emitter of the transistor 43, there is connected a base of a PNP transistor 71 in a buffer 70. The emitter of the transistor 71 is directly connected to a base of an NPN transistor 72 and is also connected through a resistor 73 to the voltage source terminal 1. The collector of the transistor 71 is grounded. The collector of the transistor 72 is connected to the voltage source terminal 1 and the emitter thereof is directly connected to the output terminal 2 and is also connected through a resistor 48 to the collector of the transistor 41.

The transistors 41 and 44 in Fig. 3 are corresponding to the current sources 21 and 24 in Fig. 2, respectively.

A current I_{35} supplied to the multi-emitter transistor 35_N is equally divided to each of unit transistors which are presented as N emitters in Fig. 3. Thus, in the constant current circuit 30 shown in Fig. 3, if respective base-emitter voltages of the transistors 33 and 35_N are taken into consideration, the following equation (9) is established similarly to the equation (4b).

$$I_{35} = \frac{V_T}{R_{36}} \ln \left(\frac{N \cdot I_{33}}{I_{35}} \right) \quad \dots (9)$$

The PNP transistors 31 and 32 of current mirror circuit configuration can keep the collector currents I_{33} and I_{35} of the transistors 33 and 35_N in a relationship expressed as $I_{33} = I_{35}$. The application of this relationship to the equation (9) yields the following equation (10)

$$I_{35} = \frac{V_T}{R_{36}} \ln N \quad \dots (10)$$

Since the bases of the transistors 33, 35_N and 41 are connected to one another, the respective collector currents thereof are kept equal to one another in magnitude so that the constant current I_1 equal to the current I_{35} expressed by the equation (10) is flowed into the transistor 41.

In Fig. 3, if the respective base-emitter voltages of the transistors 33 and 46 are taken into consideration, the following equation (11) is established where R_{37} is the resistance value of the load resistor 37.

$$V_T \ln \left(\frac{I_{33}}{I_S} \right) = V_T \ln \left(\frac{I_2}{I_S} \right) + I_{35} R_{37} \quad \dots (11)$$

To arrange the equation (11) yields the following equation (12)

$$\frac{I_{33}}{I_2} = \exp \left(\frac{I_{35} R_{37}}{V_T} \right) \quad \dots (12)$$

Since the collector current I_{35} of the multi-emitter transistor 35_N is obtained as in the equation (10), to substitute the equation (10) to the equation (12) and arrange the same yield the following equation (13)

$$\frac{I_{33}}{I_2} = \exp \left(\frac{R_{37}}{R_{36}} \right) = N^m$$

where $m = R_{37}/R_{36}$

... (13)

$$\therefore I_2 = I_{33}/N^m$$

5 where $m = R_{37}/R_{36}$

While the constant current I_2 expressed by the equation (13) is flowed into the transistor 46, the transistors 45 and 44 of the current mirror circuit configuration cause a current of which the magnitude is the same as that of the constant current I_2 expressed by the equation (13) to be
10 flowed into the base of the transistor 43. Thus, similarly to the embodiment shown in Fig. 2, the current $8I_2$ from the transistor 43 is supplied to the collector of the transistor 42 and the transistor 72 in the buffer 70 supplies the
15 current I_2 through the resistor 48 to the base of the transistor 42.

Through the resistor 48 the current is the sum of the collector current I_1 of the transistor 41 and the base current I_2 of the transistor 42. In the embodiment shown in Fig. 3, in
20 order to derive the energy-gap voltage V_{REF} from the output terminal 2, from the equations (6), (10) and (13), the coefficients K_1 and K_2 must be defined as expressed by the following equation (14)

$$25 \quad \left. \begin{aligned} K_1 &= \ln N \\ K_2 &= \frac{\ln N}{N^m} \end{aligned} \right\} \quad \dots (14)$$

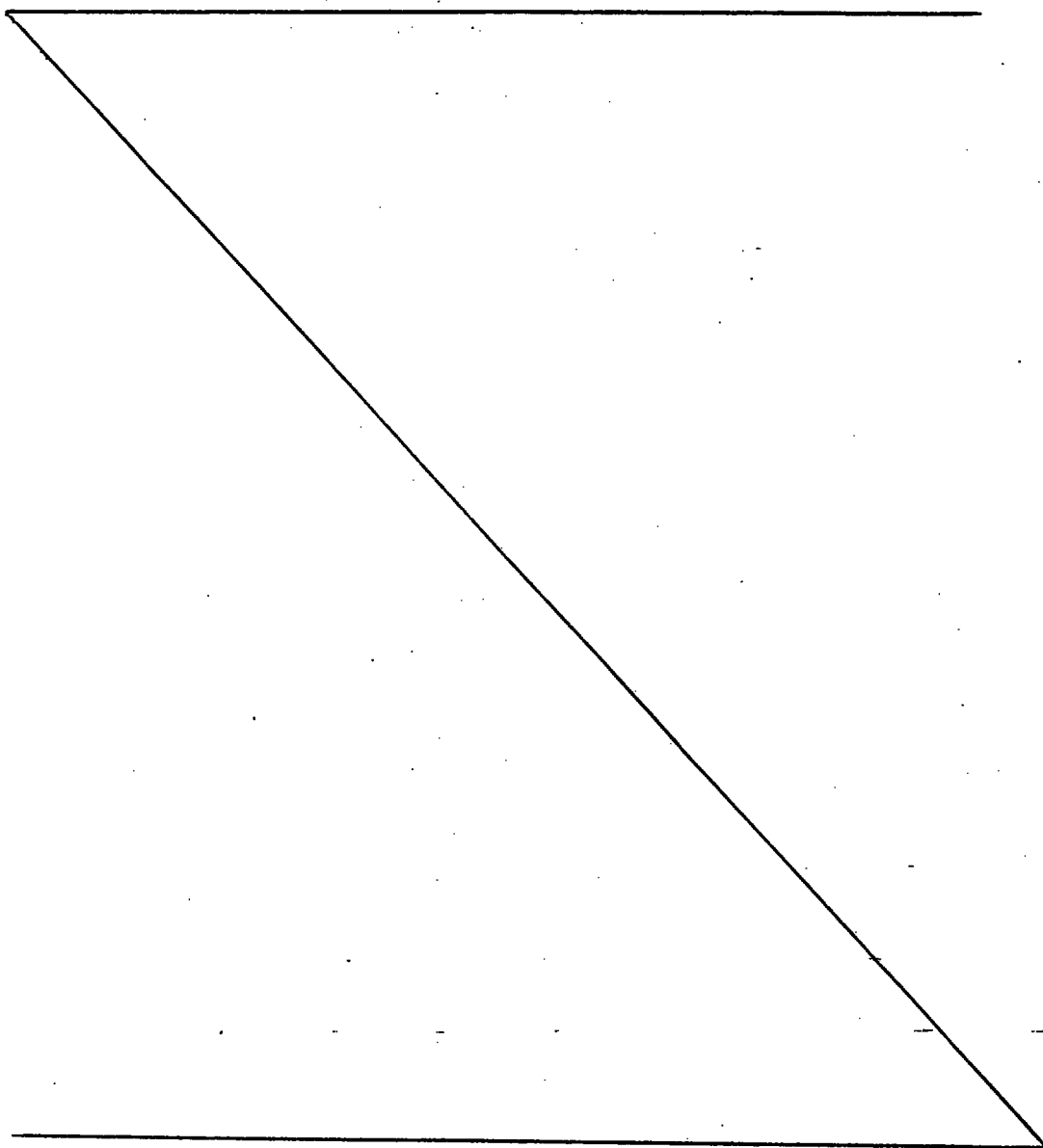
where $m = R_{37}/R_{36}$.

In this embodiment, when the emitter area ratio of the multi-emitter transistor 35_N is selected so as to satisfy N
30 $= 8$, the resistance values of the emitter resistor 36 and

the resistors 37 and 48 are determined as, for example, $R_{36} = 1.2 \text{ K}\Omega$, $R_{37} = 2.4 \text{ K}\Omega$ and $R_{48} = 12 \text{ K}\Omega$, respectively.

In this case, it should be noted that from the equation (13), the equality, $I_2 = I_1/8^2$ be established. In this embodiment, since there is provided a very small constant current output, the resistance value of the resistor can be selected to be relatively low. Thus, it is possible to employ the constant current circuit 30 which is suitably fabricated into an integrated circuit (IC).

10



According to the present invention, as set forth above, since the constant current source, through which a current flows which has a magnitude which is an integral multiple of the reference current, is connected to the collector-emitter current path of the transistor in series, it is possible to obtain the voltage regulator circuit which can suppress fluctuations of the base-emitter voltage of the transistor due to the fluctuation of the base impurity concentration in the manufacturing process.

The above description is given of preferred embodiments of the invention and it will be apparent that many modifications and variations thereof could be effected by one with ordinary skill in the art without departing from the scope of the invention as defined in the appended claims.



17

CLAIMS

1. A voltage regulator circuit comprising:
 - a) a first current source for generating a predetermined current;
 - 5 b) a first transistor supplied at its base with the predetermined current from said first current source and for generating an emitter current which is β times said predetermined current;
 - c) a second transistor having a collector connected
10 to said emitter of said first transistor and of which the emitter is grounded;
 - d) a second current source connected at its one end to the base of said second transistor and one end of a resistor which generates a reference voltage; and
15 e) a buffer amplifier connected between the emitter of said



18

first transistor and the other end of said resistor, wherein a predetermined voltage is derived at the other end of said resistor.

2. A voltage regulator circuit according to claim 1,
5 wherein said second current source is supplied with a bias voltage from a current mirror circuit.

3. A voltage regulator circuit according to claim 2,
wherein said current mirror circuit includes:
10 first and second transistors of a first conductivity type of which the emitters are connected together to a first reference potential and of which the bases are connected to each other;

a third transistor of a second conductivity type of which the collector is connected to the collector and base of said
15 second transistor and of which the base is connected to the collector of said first transistor;

an emitter-grounded fourth transistor of the second conductivity type of which the collector is connected to the base of said third transistor and of which the base is
20 connected to the emitter of said third transistor and a fifth transistor of the second conductivity type having a base connected to the base of said fourth transistor; and a collector connected through a resistor to the emitter of said third transistor and an emitter connected through a
25 resistor to a second reference potential, wherein the bias voltage is derived from the base or collector of said fourth transistor.

4. A voltage regulator circuit according to claim 3,
wherein an emitter area of said fifth transistor in said
30 current mirror circuit is selected to be an integral



19

multiple of that of said fourth transistor.

5. A voltage regulator circuit constructed and arranged to operate substantially as hereinbefore described with reference to and as illustrated in Figures 2 and 3 ~~or Figures 4 and 5~~ of the accompanying drawings.

6. A constant current circuit constructed and arranged to operate substantially as hereinbefore described with reference ^{and} to ~~as~~ illustrated in Figures 2 and 3 ~~or Figures 4 and 5~~ of the accompanying drawings.
