SPECIFICATION

Integrated logic circuits

The invention relates to integrated circuits having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled via a diode to a collector of the bipolar transistor.

Pages 168 and 169 of the Digest of Technical Papers, February 1975 of the "1975 I.E.E.E. International Solid-State Circuits Conference" describe an integrated logic circuit having a signal input which is formed by a base of bipolar transistor and having several signal outputs which are each coupled, *via* a diode, to the collector of the bipolar transistor. The signal input comprises current supply means. The integrated circuit comprises a semiconductor body having a major surface adjoined by several surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first. At least one of the said surface regions belongs to a collector region of the first conductivity type which forms part of the bipolar transistor. Said collector region has a high-ohmic and a low-ohmic part, the low-ohmic part extending at and along the interface with the substrate region. The bipolar transistor furthermore comprises an emitter zone of the first conductivity type which adjoins the major surface and which in the semiconductor body is separated from the collector region by a base zone of the second conductivity type extending up the major surface. The base zone is formed in the collector region and is situated above a portion of the collector region. An electrically insulating layer is present on the major surface and has a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and several third apertures which are situated beside the base zone and above the collector region.The insulating layer separates from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures. Each of the conductor tracks which extend into a third aperture is coupled to the collector region *via* a rectifying junction which adjoins the collector region; these rectifying junctions from the said diodes. The bipolar transistor is surrounded at the major surface by an isolation zone by means of which the bipolar transistor is isolated electrically, at least during operation, from adjacent surface regions of the first conductivity type.

This circuit known from the said Digest of Technical Papers is described as being very attractive for large-scale integration. (LSI). The basic cell is a NAND gate in which the coupling diode at the signal outputs are provided as Schottky diodes. In addition the cell also comprises a Schottky diode which is connected in parallel with the collector-base junction of the transistor. This latter Schottky diode (clamp diode) has a larger diode forward voltage than the coupling diodes. The swing of the logic signal (that is the voltage difference between the signals representing a logic 1 and a logic 0, respectively) is equal to the difference in diode forward voltage of the two mutually different types of Schottky diodes. As a result, this swing can be comparatively small, which improves the switching speed of the cell. The minimum delay time of the cell is comparable to that of the transistor-transistor logic version with Schottky diode clamping and low dissipation which is sometimes referred to by the abbreviation LS TTL. Furthermore, the cell is particularly compact and the product of delay time and power dissipation is also attractively low.

Although this attractive LSI logic was announced nearly three years ago now, it has up till now not resulted in commercial products which have found acceptance on the market, at least in as far as the inventor is aware.

The present invention is based on a realization by the inventor that the integrated circuit described can be modified so that it can be manufactured in a simpler and cheaper manner, while the attractive electrical properties and the high packing density desired for the integration can be maintained for the greater part.

Surprisingly the Applicants have found experimentally that, by means of special measures in the semiconductor structure which need not require any extra operations during the manufacture, it is possible to omit the clamp diode without the switching time of the cell being increased in an inadmissable manner.

According to the invention, such an integrated logic circuit is characterized in that means are present to restrict storage of charge-carriers in the high-ohmic part of the collector region, and in addition there is incorporated in the semiconductor structure of the bipolar transistor a further surface zone of the first conductivity type which is provided with an electrical connection and is separated from the said collector region by the base zone, which collector region, base zone and said further surface zone of the first conductivity type serve as emitter, base, and collector, respectively, of an auxiliary transistor so that, if the bipolar transistor is overdriven, a considerable part of the current flowing through the base connection of the bipolar transistor can be dissipated in the auxiliary transistor and the storage of mobile charge carriers in the overdriven transistor can be reduced considerably.

The current dissipated by the auxiliary transistor reduces the current flowing through the base connection so that the base current available for the actual inverter transistor is reduced.

Such an integrated logic circuit with an inverter transistor having coupling diodes integrated on or in the collector region and an effective built-in auxiliary transistor can have switching speeds which are equal to or are better than those of LS TTL, while the dissipated power can be considerably smaller. In addition, the packing density may be a factor two to six larger than for LS TTL. The electrical connection of the further

surface zone of one conductivity type is preferably formed by the conductor track which extends into the second aperture situated above the base zone of the bipolar transistor. At the major surface substantially no extra space is necessary for the further surface zone of the first conductivity type when it is provided below the base contact in such manner that the *p-n* junction formed between said further zone and the base zone in the second aperture extends up to the major surface and is short-circuited at that area by the electrical connection of the base zone.

The means to restrict storage of charge-carriers in the high-ohmic part of the collector region may have various forms, as described hereinafter. In one form said means may comprise a complementary auxiliary transistor as described hereinafter. In another form, said means may comprise an isolation zone of insulating material extending from the major surface to a large depth in the semiconductor body than the base zone of the bipolar transistor, said zone of insulating material separating said base zone from the high-ohmic collector part adjoined by said rectifying junctions.

The isolation zone by means of which the bipolar transistor is isolated from said adjacent surface regions may comprise zones of insulating material extending from the major surface to a larger depth in the semiconductor body than the base zone of the bipolar transistor, and the base zone adjoins the insulating material at least over a considerable part of its periphery. In this manner small bipolar transistors having small capacitances and low charge storage can be obtained while the auxiliary transistor further reduces and controls the storage of charge.

In an important form of the integrated circuit according to the invention a complementary auxiliary transistor is also incorporated. The extent of the low-ohmic part of the collector region of the first conductivity type in a direction substantially parallel to the major surface is preferably restricted so that said low-ohmic part extends below the said emitter zone and below the rectifying junctions of the signal-output diodes but does not extend below the part of said base zone underlying the second aperture in the insulating layer whereby a region of the high-ohmic part of the collector region directly adjoins the substrate region to form a *p-n* junction, the part of the substrate region adjoining the high-ohmic part of the collector region cooperating as a collector of a complementary auxiliary transistor with the adjoining collector region and the base zone of the bipolar transistor. In this embodiment the thickness of the high-ohmic part of the collector region measured between the second and the third *p-n* junction preferably is smaller than 5 microns (5×10^{-6}) metres).

In another important form of the integrated circuit according to the invention in which a complementary auxiliary transistor is also incorporated, a further surface zone of the second conductivity type adjoining the collector region of the first conductivity type is present at the major surface beside the base zone and extends from the major surface to substantially the same depth in the semiconductor body as the base zone, said further zone serving as a collector of the complementary auxiliary transistor and being connected to the substrate region.

Said further surface zone of the second conductivity type can simply be provided simultaneously with the base zone so that the distance between said zones can be comparatively small. Preferably the distance at the major surface between the base zone and the further surface zone of the second conductivity type is at most 5 microns.

These vertical and horizontal complementary auxiliary transistors may also be combined advantageously in the same bipolar transistor of an integrated circuit in accordance with the invention.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which

Fig. 1 is the electrical circuit diagram of the known NAND gate;

Fig. 2 is a part of a diagrammatic plan view of a first integrated circuit in accordance with the invention;

Fig. 3 is a diagrammatic cross-sectional view of this part of the first circuit taken on the line III—III of Fig. 2;

Fig. 4 shows diagrammatically a part of a second integrated circuit in accordance with the invention, and

Fig. 5 is a diagrammatic cross-sectional view associated with the said second circuit and taken on the line VI—VI of Fig. 4.

The electrical circuit diagram of the above-mentioned known NAND gate, shown in Fig. 1, has a signal input 1 which is formed by the base of a bipolar transistor T and several signal outputs 2, 3, 4 and 5 which are each coupled to the collector of the bipolar transistor T *via* a diode 6. The signal input 1 has current supply means which are denoted by the current source I.

The transistor T is a planar transistor, the collector-base junction of which is shunted by a Schottky diode 7. Due to said clamp diode the transistor has the high switching speed which is desired nowadays for logic circuits. If the clamp diode 7 were omitted, the transistor in the conductive state will become highly saturated. The transistor then comprises a large amount of stored charge, mainly in the form of minority charge carriers, which are situated in the collector region. The switching off of the transistor would then occur only slowly. The clamp diode 7 prevents the transistor from becoming saturated so that this charge storage is avoided.

If during operation the signal input 1 is not connected, the signal input 1 will be charged by the supplied current I to the emitter-base voltage of the transistor T associated with the conductive state. This diode forward voltage of junction voltage V_{BE} is, for example, approximately 700 to

750 mv for a silicon transistor.

When the voltage at the signal input reaches the diode forward voltage V_{BE}, the transistor T becomes conductive and the current I is used as a base current. The current available at one or more of the signal outputs is then dissipated *via* transistor T, the voltage at the relevant signal output being equal to the diode forward voltage V_{D1} of the coupling diodes 6 augmented by the collector-emitter voltage of the conductive transistor T. This collector-emitter voltage is equal to the voltage V_{BE} reduced by the diode forward voltage V_{D2} of the clamp diode 7. If the voltage V_{D2} is larger than the voltage V_{D1}, the signal output voltage is smaller than V_{BE} and the transistor of a following NAND gate connected to the relevant signal output will be kept in the non-conductive state.

The swing of the logic signal, that is the difference between the high and the low signal level, is equal to the difference between the diode forward voltages V_{D2} of the clamp diode 7 and V_{D1} of the coupling diode 6.

The Schottky clamp diode 7 is a PtSi/Si contact with a diode forward voltage V_{D2} of approximately 500 mV. The Schottky coupling diodes 6 are Ti/Si contacts with a diode forward voltage of approximately 350 mV. The logic swing then is approximately 150 mV. This comparatively small logic swing has a favourable effect on the delay time of the gate circuit. When switching from the high to the low signal state, or conversely, only a small voltage difference need be bridged. So the switching can be realised in a correspondingly short period of time.

Thus, the described known logic circuit owes its attractive circuit properties to two things. In the first place there is the use of a high speed planar transistor T which is freed from saturation by means of the Schottky diode 7, and in the second place there are the metal-to-semiconductor contacts having different compositions of metallisation which provide Schottky diodes with a favourably small difference in diode forward voltage of approximately 150 mV. Hence both in the switching transistor T and in determining the desired logic swing the metallisation chosen plays an essential and decisive part.

The present invention makes it possible to use, instead of this choice of complex metallisation which necessarily is constructed from conductive layers of different materials, a much simpler metallisation which, may, for example, have been used already in existing products.

The first embodiment which will be described further with reference to Figs. 2 and 3 has a semiconductor body 20 a major surface 21 of which is adjoined by several surface regions 22, 23 and 24 of a first conductivity type which are situated on a common substrate region 29 of a second conductivity type opposite to the first. The substrate region 29 may be a semiconductor layer provided, for example, on any suitable substrate. In the present example the region 29 is a *p*-type semiconductor substrate of silicon having a resistivity of, for example, 10 to 15 Ohm-cm.

At the major surface 21 the surface regions 22, 23 and 24 are each surrounded by an isolation zone 30 by means of which the surface regions are isolated electrically from each other at least during operation. In this example the isolation zones consist entirely of insulating material. Alternatively, *p*-type zones may be used extending from the major surface 21 into an *n*-type surface layer. The isolation zones 30 extend over a part of the thickness of the surface layer or penetrate through the surface layer entirely so that they reach down into the substrate 29. By applying a voltage in the reverse direction across the *p-n* junctions formed between the *p*-type isolation zones and the surface regions 22, 23 and 24 and/or between the substrate 29 and the surface regions 22, 23 and 24, electric isolation between the surface regions 22, 23 and 24 can be ensured in the usual manner during operation. Alternatively, the isolation zones may consist partly of insulating material and partly of *p*-type semiconductor material.

As illustrated by region 22 in Figures 2 and 3 at least one of the surface regions 22, 23 and 24 serves as a collector region of a bipolar transistor. This collector region 22 has a high-ohmic part 31 and a low-ohmic part 32. The low-ohmic part 32 extends at and along the interface between the collector region 32 and the substrate region 29.

The bipolar transistor furthermore has an emitter zone 33 of the first conductivity type which adjoins the major surface 21 and which is separated in the semiconductor body 20 from the collector region 22 by a base zone 34 of the second conductivity type extending up to the major surface 21. The *n*-type emitter zone 33 forms, with the *p*-type base zone 34, a first *p-n* junction 35 having a first diode forward voltage V_{BE}. The *p*-type base zone 34 forms, with the *n*-type collector region 22, a second *p-n* junction 36.

Present at the major surface 21 is an electrically insulating layer 37 which in the plan view shown in Fig. 2 is considered to be transparent. The layer 37 consists of an insulating material, for example silicon dioxide or silicon-nitride or a combination thereof. A first aperture 38 in the insulating layer 37 is situated above the emitter zone 33. A second aperture 39 is situated beside the emitter zone 33 and above the base zone 34. In addition, beside the base zone 34 and above the collector region 22 several third apertures 40 are present. In Fig. 2, the apertures shown in the insulating layer 37 are illustrated in broken lines.

The insulating layer 37 separates conductor tracks 11, 12, 13, 14, 15 and 41 from the semiconductor body 20; these tracks extend into the first, second and third apertures 38, 39 and 40, respectively, for electrical connection. For clarity, not all conductor tracks of the integrated circuit are shown in Fig. 2. Those conductor tracks which are shown are shaded.

The conductor tracks 12, 13, 14 and 15 extending into the third apertures 40 are each

coupled to the collector region 22 *via* a rectifying junction 16 which adjoins said collector region. In this example the rectifying junctions 16 are metal-to-semiconductor junctions or Schottky junctions. These Schottky junctions may be formed as platinel silicide contacts as described in, for example, United States Patent Specification 3,855,612. The rectifying junctions 16 have a diode forward voltage V_{D1}. For the operation of the circuit it is desirable that junctions 16 used have a diode forward voltage V_{D1} which is smaller than the diode forward voltage V_{BE} of the emitter-base *p-n* junction 35 of the transistor.

In a direction substantially parallel to the major surface 21, the low-ohmic part 32 of the collector region 22 extends from below the emitter zone 33 to below the rectifying junctions 16.

In accordance with the invention, means which will be described hereinafter are present to restrict storage of charge-carriers in the high-ohmic part 32 of the collector region 22, and a further surface zone 80 of the first conductivity type is incorporated in the semi-conductor structure of the bipolar transistor 33, 34, 22 and is separated from the collector region 31, 32 by the base zone 34. The collector region (and in particular the low-ohmic part 32p), the base zone 34 and the *n*-type further surface zone 80 serve as emitter, base, and collector, respectively, of an auxiliary transistor. This auxiliary transistor is of the same type as the bipolar switching or inverter transistor. In this example the inverter transistor and the auxiliary transistor are both *n-p-n* transistors.

The further surface zone 80 is preferably provided simultaneously with the emitter zone 33 so that the depth of penetration into the base zone 34 and the doping concentration profile of the zones 80 and 33 are the same.

The further surface zone 80 which serves as collector of the auxiliary transistor comprises an electrical connection. This connection may be a separate connection to which a suitable reference potential can be applied during operation. Preferably, however, as in the example, this connection is combined with the connection for the base zone 34. The *p-n* junction 81 between the further zone 80 and the base zone 34 extends in the second aperture 39 up to the semiconductor surface 21 and is short-circuited in the aperture 39 by means of the conductor track 11. The conductor track 11 is connected both directly to the base zone 34 and directly to the further surface zone 80.

In the circuit described, the auxiliary transistor 32, 34, 80 proves to be a means to improve the switching speed, which is surprisingly effective. Minimum delay times of a few nanoseconds (n.sec) can be realised with this integrated logic gate circuit in accordance with the invention. Hence the minimum delay time is comparable with or more favourable than that of the conventional LS TTL. The packing density and the product of delay time and power dissipation can both be more favourable than for LS TTL. These favourable properties of the integrated circuit in accordance with the invention are also remarkable in particular because in contrast with LS TTL in which the inverter transistor in the conductive state is not saturated, the inverter transistor in the present circuit is saturated. However, as soon as the base-collector junction 36 becomes biased in the forward direction, a part of the base current of the overdriven inverter transister will be used as a base current for the auxiliary transistor. In addition, when the surface zone 80 is connected to the base zone 34, usually a considerably larger part of the base current will be able to flow through the main current path of the auxiliary transistor directly to the collector of the inverter transistor.

Minority charge carriers are collected from the base zone 36 across the rectifying junction 81 which is not biased in the forward direction. As a result of this the storage of said charge carriers in itself is already reduced. An important effect, however, is also that, since a considerable part of the current flowing through the connection 11 is dissipated in the auxiliary transistor, less base current is available for the inverter transistor itself. As a result of this the inverter transistor is less overdriven so that the base-collector junction 36 is biased less far in the forward direction and the voltage across the emitter-base junction 35 will also be smaller. As a result of this the storage of minority charge carriers in the inverter transistor as a whole can also be accordingly smaller.

As in the present example, the isolation zones 30 preferably comprise insulating material, said insulating material extending from the major surface 21 down to a larger depth into the semiconductor body 20 than the base zone 34 of the bipolar inverter transistor. The base zone adjoins the insulating material at least over a considerable part of its periphery. In the example the base zone 34 on three sides adjoins the isolation zone 30 which separates the transistor from the other transistors. A zone 82 of insulating material is also present on the fourth side, the side of the base zone 34 facing the coupling diodes. This part 82 of the pattern of insulating material does not serve for electric insulation of the transistor but serves to limit the base zone 34. By using the pattern of insulating material the surface of the base-collector junction 36 is kept comparatively small and the possibility of storage of charge carriers in the collector region 22 is restricted and the storage of charge carriers in the high-ohmic part 31 of the collector region 22 situated beside the base zone 34 is avoided.

It is to be noted that, although the zone 82 of insulating material is preferably present, this zone 82 is not necessary. The zone 82 may be omitted entirely so that the high-ohmic part 31 of the collector region adjoins the base zone 34 at that area. In that case also the storage of charge carriers in the collector region will be comparatively small due to the suctorial effect of in particular the coupling diode situated nearest. This suctorial effect will be further described with reference to the second example.

Furthermore, instead of the zone 82 of insulating material, a highly doped *n*-type zone may be used which restricts the injection of holes from the base zone 34 in the lateral direction substantially parallel to the major surface.

In the example the base zone 34 of the inverter transistor reaches down to the low-ohmic part 32 of the collector region 22 and said base zone is separated from the substrate region 29 by said part 32. The doping concentration on the collector side of the junction 30 will hence be comparatively high so that the depletion capacity of said junction is comparatively large. It is more important, however, that, due to said comparatively high concentration, comparatively little storage of minority charge carriers will occur in the collector region.

The emitter zone 33 adjoins the insulating material 30 only on two sides. This has for its advantage that the surface area of the emitter zone 33 is not so dependent on deviations in location which may result from non-ideal alignment of masks during the manufacture. In applications in which the size of the surface area of the emitter zone is not very critical, however, the emitter zone may also be provided against the insulating material 82 so that the emitter is bounded by insulating material on three sides. In that case the inverter transistor may be smaller.

Fig. 2 also shows surface regions 23 and 24 which comprise identical, or at least similar, circuit elements. Thus these regions 23 and 24 each serve as a collector region of a planar *n-p-n* transistor having a number of signal output tracks which are coupled to the relevant collector region *via* a diode. The number of diodes may vary for each individual transistor between one and, for example, four or five and will depend on the logic function to be generated by the integrated circuit.

The collector regions or islands 22, 23 and 24 are arranged beside each other along an elongate surface region 28 from which the signal inputs 11 are provided with current. In this region 28 a number of lateral *p-n-p* transistors are provided which have a common *p*-type emitter zone 43. The region 28 serves as a common *n*-type base zone. The *p-n-p* transistors each have a separate *p*-type collector zone 44 which is connected to a signal input 11 *via* an aperture 45 in the insulating layer 37. The common emitter zone 43 is connected, *via* an aperture 46, to a conductor track 47 which has a diagrammatically shown connection 48 for a supply source.

The common base zone 28 has a high-ohmic part 49 and a low-ohmic part 50 in the form of a buried layer. Furthermore, a low-ohmic *n*-type surface region 51 is present in the base zone 28 which may be provided, for example, simultaneously with the emitter zone 34. The buried layer 50 and the surface region 51 serve to reduce the base series resistance. The buried layer 50 also serves to suppress parasitic transistor action to the substrate. Above the surface region 51 and aperture 52 in the insulating layer 37 is present through which the common base zone 28 is connected to a conductor track 53.

The integrated circuit is constructed with a metallisation which comprises several layers, as is common for complex LSI circuits nowadays. For that purpose, the insulating layer 37 consists of a first or lowermost layer 55 having the apertures 38, 39, 40, 45, 46 and 52 and a second or uppermost layer 56. A first level of conductor tracks which comprises *inter alia* the conductor tracks 12 to 15, 47 and 53 is situated on the lowermost layer 55. The conductor tracks 11 consist of two parts of which first parts 57 lie at the first level and extend into the apertures 39 and 45 and of which a second part 58 lies at a second level which is separated from the first level by the uppermost layer 56; the second part 58 is directly connected to the first parts 57 *via* apertures 59.

Connections between signal inputs 11 and signal outputs 12 to 15 can also be realised by means of the second level of conductor tracks. For example, the base zone of the inverter transistor in the island 24 may be connected to the conductor track 12. The second part 58 of the conductor track 11 then extends in the direction shown horizontally in Fig. 2 from the contact with the base zone across the emitter zone of the inverter transistor and the conductor track 41 to above the conductor track 12 and at that area it is connected through an aperture 59 (not shown) in the second insulating layer 56 to the end shown of the conductor track 12.

In a modified embodiment of this example the conductor track which interconnects the emitters is moved to the second level of conductor tracks and the intermediate spaces between the inverter transistors are slightly enlarged so that the first parts 57 of the conductor tracks 11 can be connected to the conductor tracks 12 to 15 at the first level *via* conductor tracks situated at the first level and extending between the inverter transistors. The conductor track 53 may be connected to a connection 54 which is shown diagrammatically.

The conductor tracks 12 to 15, 47 and 57 of the first level may be, for example, aluminium or another suitable conductive material. If desired, a barrier layer may be used to avoid direct contact between the aluminium and the platinel silicide formed in the apertures in the insulating layer. As a barrier layer may be used, for example, titanium-platinum or titanium-tungsten or rhodium.

The conductor tracks 58 of the second level are, for example, of aluminium or titanium-platinum-gold.

Preferably, the same material is in direct contact with the semiconductor body in all apertures 38, 39, 40, 45, 46 and 52 in the first insulating layer 37 and particularly in the first, the second and the third apertures 38, 39 and 40. In the present example this material is the said platinel silicide which in the apertures 40 forms a Schottky diode and which, in the other apertures, forms a readily conductive junction between the conductor tracks and the adjoining semiconductor regions in said apertures.

The conductor track 41 connected to the emitter zone 33 is provided with a connection 60, shown diagrammatically, and the substrate region 29 has a connection 61 which may be connected to the connection 60 to form a common connection 62 for a supply source.

The connection 62 may be connected to a suitable reference potential, for example earth potential. A suitable current or voltage supply source is connected between the connections 62 and 48. The connection 54 is connected to a suitable reference potential, the *p-n-p* transistors being conductive. The integrated circuit furthermore has one or more signal inputs, not shown, *via* which input signals can be supplied to one or more conductor tracks 11, and one or more signal outputs, not shown, *via* which output signals generated by the integrated circuit can be derived. For the sake of completeness it is to be noted that the second level of conductor tracks may be covered entirely or partly with a further insulating layer, if so desired.

The embodiment described can be manufactured entirely by means of methods known in semiconductor technology. For example, the method may be used which is described in Netherlands Patent Application 7709363 (PHN 8870). As a result of this reference the specification of said Patent Application 7709363 is to be considered to be incorporated in the present Specification. This method is of advantage *inter alia* when the current supply to the base zones of the inverter transistors is realised by means of lateral complementary transistors. A second embodiment will be described with reference to Figs. 4 and 5. In this embodiment, the same reference numerals are used as in the first example for corresponding components of particularly the inverter transistor and the coupling diodes.

In the plan view shown in Fig. 4 the conductor tracks at the first level are shown only partly. This concerns *inter alia* the conductors 11, 12 and 57. For clarity, the conductor tracks shown are shaded in this Figure also.

The second embodiment comprises a number of *n*-type surface regions 22 to 26 and 72 which are separated from each other in the usual manner by means of *p*-type isolation zones. The surface regions 22 to 26 serve as collector regions of bipolar inverter transistors. the transistor in the collector region 22 will be described in greater detail hereinafter.

Said transistor comprises an emitter zone 33 and a base zone 34 which from a first *p-n* junction 35. The base zone 34 furthermore forms a second junction 36 with the collector region 22. A further *n*-type surface zone 80 which is connected to the conductor track 11 is provided in the base zone. This transistor also comprises a vertical auxiliary transistor 22, 34, 80 which is of the same type as the inverter transistor. Both transistors are *n-p-n* transistors. In this example a few further measures are taken in addition to improve the switching speed.

In this embodiment, the extent of the low-ohmic part 32 of the collector region 22 in a direction substantially parallel to the major surface 21 is restricted so as to form a complementary auxiliary transistor. The said part 32 is situated below the emitter zone 33 and below the rectifying junctions 16 but does not extend below part of the base zone 34 underlying the second aperture 39; in this way a region of the high-ohmic part 31 of the collector region directly adjoins the substrate region 29 to form a third *p-n* junction 42. The thickness of the high-ohmic part 31 of the collector region 22 measured between the second and third *p-n* junctions 36 and 42, respectively, is preferably smaller than 5 microns. As a result of this additional measure, by which below the base contact the substrate region extends up to a comparatively small distance from the base-collector junction 36, the relevant part of the substrate region cooperates effectively as a collector of a complementary (*p-n-p*) auxiliary transistor with the adjoining high-ohmic part 31 which is situated between the two *p-n* junctions 36 and 42, and with the base zone 34. A vertical complementary (*p-n-p*) auxiliary transistor 34, 31 29 is also incorporated in the *n-p-n* transistor structure in an effective manner and substantially without this requiring more semiconductor surface area for the transistor. As a result of this, when the inverter transistor is overdriven, a part of the current flowing in the base zone 34 flows through the complementary auxiliary transistor 34, 31, 29 so that the storage of mobile charge carriers in the overdriven inverter transistor is further restricted.

In the present example the emitter zone 33 is, for example, 12 microns x 12 microns. The associated contact aperture 38 is approximately 6 microns x 6 microns and for the distance at the semiconductor surface between the emitter-base junction 35 and the base-collector junction 36 a minimum value of 3 microns is used. The active part of the base zone required for the emitter zone is 18 microns x 18 microns. However, at least one contact aperture for contacting the base is necessary beside the emitter zone.

In this connection, the active part of the base zone 34 is to be understood to mean that part which is necessary to be able to accommodate an emitter zone 33. Adjoining said active part a non-active part of the base zone 34 is necessary for electrical connection of the conductor track 11.

The dimensions of the base zone 34 are, for example, 37 microns x 18 microns. The size of the non-active part in this case is 18 microns x 19 microns and it thus has a larger area than the active part. Within the scope of the present invention the non-active part of the base zone 34 which provides the emitter of the vertical complementary auxiliary transistor is preferably at least equally large as the active part.

The comparatively large non-active part of the base zone 34 in this example facilitates the placing of the further surface zone 80 and the short circuit of the *p-n* junction 81 in the aperture 39. The aperture 39 is, for example, 10 microns x

12 microns and the surface zone 90 is approximately 6 microns x 12 microns. The area occupied at the major surface 21 by the surface zone 80 is preferably at least one third of that of the emitter zone 33 and the surface zone 80 is at most two to three times as large as the emitter zone 33. Good results were obtained in particular with a surface zone 80 which is at least half as large as the emitter zone 33.

Since the non-active part of the base zone 34 in this example is comparatively large and the low-ohmic part 32 of the collector region 22 does not substantially reach further than to below the emitter zone 33, the oppositely located parts of the *p-n* junctions 36 and 42 also have a comparatively large area. This means that the incorporated vertical *p-n-p* auxiliary transistor is comparatively large. According as the *n-p-n* auxiliary transistor and/or the *p-n-p* auxiliary transistor is larger, excessive base current of the conductive inverter transistor is dissipated more effectively and at a lower forward voltage across the *p-n* junction 36. The conductive inverter transistor is then less overdriven and the charge storage in said transistor is correspondingly reduced.

The apertures 40 have dimensions of, for example, 5 microns x 22 microns.

For completeness' sake it is to be noted that the above-given dimensions simply relate to the masks which are necessary for the various photolithographic treatments during the manufacture. In the integrated circuits themselves the actual dimensions, as is known, differ slightly *inter alia* because upon exposure and development of the photosensitive lacquer an exact reproduction of the masks is not obtained because during the etching treatments undercutting often occurs and because upon diffusion of impurities lateral diffusion also occurs.

In the above description it is assumed that the inverter transistor has a single emitter zone 33 and a single base contact aperture 39. Alternatively, for example, two conductively interconnected emitter zones may be used dependent *inter alia* on the desired current level. Several base contact apertures may also be present, for example, two contact apertures on oppositely located sides of a single emitter zone. When several base contact apertures are used it is not necessary to incorporate an auxiliary transistor below each of the base contacts. The collector region 22 of the inverter transistor preferably is substantially rectangular and the apertures 38, 39 and 40 in the insulating layer are situated beside each other in the same direction, the emitter contact aperture or apertures 38 and the associated emitter zone or zones 33 being situated between the apertures 40 for the coupling diodes on one side and the or at least one of the apertures 39 for the base contact on the other side. The incorporated vertical complementary auxiliary transistor is preferably situated below the last mentioned outermost base contact aperture. The buried layer 32 preferably continues in an uninterrupted manner from below the emitter zone 33 to below the coupling diodes 16. A further surface zone 80 is preferably situated at least near said outermost base contact aperture. Because in this place the vertical complementary auxiliary transistor is incorporated, the space available for the further surface zone 80 usually is comparatively large. If other second apertures 39 are also present above the base zone 34, surface zones 80 may also be provided advantageously near said base contact apertures. In this connection it is to be noted that by incorporating a vertical complementary auxiliary transistor below a surface zone 80, the favourable effect of the surface zone 80 in itself can be reduced. The fact that in that case the low-ohmic part 32 of the collector region 22 does not extend to below the surface zone 80, may result in the collector region 22 constituting a less efficient emitter for the *n-p-n* auxiliary transistor. The overall favourable effect of the two auxiliary transistors together (*n-p-n* and *p-n-p*), however, will be larger than that of a single auxiliary transistor.

Another measure to improve the switching speed is that an improved lateral complementary auxiliary transistor is incorporated by the addition of a further surface zone 71 which during the manufacture can be obtained simultaneously with the base zone 34. In contrast with the surface zone 80, the zone 71 has the same conductivity type as the base zone 34 and as the isolation zone 30. At the semiconductor surface the zone 71 coincides partly with the isolation zone 30. The zones 71 and 30 overlap each other. The base zone 34 and isolation zone 30 are obtained with different diffusion treatments. As a result their mutual distance at the semiconductor surface is comparatively large. The base zone 34 and the zone 71 on the contrary are obtained simultaneously with the same diffusion treatment so that their mutual distance can be comparatively small. They have substantially the same depth of penetration in the semiconductor body and they has substantially the same doping concentration profile in a direction transverse to the major surface. A usual distance between the base zone 34 and the isolation zone 30 would be, for example approximately 10 microns. The distance between the base zone 34 and the further surface zone 71 need not be more than 5 microns. The zones 34 and 71 constitute the emitter and the collector or an effective lateral complementary auxiliary transistor the base thickness of which is 5 microns or less. If the inverter transistor is conductive, said auxiliary transistor also dissipates current so that the inverter transistor is less overdriven.

As stated, the base width of the lateral complementary auxiliary transistor is preferably at most 5 microns. In the present example the indicated distances of 10 and 5 microns apply to the masks to be used in the manufacture and the corresponding dimensions in the integrated circuit are smaller, in particular due to the occurrence of lateral diffusion. The distance between the base

zone 34 and the isolation zone 30 will be on an average be approximately 7 microns. The base width of the lateral auxiliary transistor actually is approximately 3 microns.

In this embodiment having a lateral complementary auxiliary transistor the additional surface zone 71 constitutes the region of the second conductivity type which effectively serves as collector of the complementary auxiliary transistor.

The further surface zone 71 may have a closed geometry and surround the base zone 34 as a ring, which extends between the base zone 34 on the one side and the coupling diodes 16 on the other side. Preferably, however, the further zone 71 is open on the side of the coupling diodes 16 and surrounds the base zone 34 only at the part of the edge of the base zone not facing the coupling diodes. Therefore in the present example the zone 71 is in the form of a U.

The use of a zone 71 having a non-closed geometry is based on the realization of the fact that such a zone is substantially superfluous on the side of the base zone 34 facing the coupling diodes 16. Particularly if the coupling diodes are Schottky diodes, the life time of the minority charge carriers in the collector region 22 at the rectifying junctions 10 is very small. In particular the first coupling diode situated nearest to the base zone 34 will draw minority charge carriers from the collector region and thus fulfils substantially the same faction as the zone 71. As a result of this, a slightly larger current will flow through the first coupling diode than through the remaining coupling diodes which are situated farther away. This difference in current level, however, is so small that the proper electrical operation of the circuit is not endangered. The inverter transistors have amply sufficient gain to be able to absorb said current differences.

The above-described effect of the coupling diode on the storage of minority charge carriers will also occur in the first example if the zone 81 of insulating material between the base zone 34 and the coupling diodes 16 is omitted.

The U-shaped selected for the further surface zone 71 has the important advantage that no extra area is necessary at the semiconductor surface. A closed shape or ring surrounding the whole collector region would restrict the area available for the coupling diodes. A closed shape or ring surrounding the base zone 34 and extending between the base zone 34 and the first coupling diode 16 would necessitate a larger distance between said base zone 34 and the first coupling diode 16.

Another measure by which the switching speed can be increased is to replace the lateral *p-n-p* transistor 43, 28, 44 of the first example used for the supply of current by a resistor in combination with an as low as possible supply voltage of 1 V or less. The supply voltage preferably is at most equal to the sum of the diode forward voltage V_{BE} of the inverter transistor and the swing of the logic signal, or in other words, at most equal to approximately $2V_{BE}-V_{D1}$, were D_{D1} is the diode forward voltage of the coupling diodes.

The last-mentioned measure has also been realised in the second example. The collector regions 22 to 26 of the inverter transistors are arranged on the oppositely located sides of a common surface region or island 72. Said island 72 comprises a number of resistors 73 which are each connected to a signal input conductor 11. The resistors 73 furthermore comprise connection contacts in the form of a conductive layer 74 which, as the conductor layers 82 connected to the emitter zones 33, belong to the first level of conductor tracks. The conductive layers 74 serve for the connection to a supply line 75 which is not shown in Fig. 4 and extends horizontally in the plane of the drawing of Fig. 4 substantially centrally above the resistors 73. This horizontal supply line 75 belongs to the conductor tracks of the second level and has projections which in the plane of Fig. 4 are directed alternately upwards and downwards and which are connected to the layers 74 through an aperture in the insulating layer 56 which separates the conductor tracks of different levels from each other.

The second supply line 83 also belongs to the conductor tracks of the second level and is not shown in the drawing of Fig. 4. The supply line 83 extends substantially parallel to the supply line 75 and overlies the emitter zones 33.

Fig. 4 finally shows a few signal input conductors 11 and signal output conductors 12 which belong to the first level of conductor tracks. In so far as signals of other parts of the integrated circuit situated further away are to be supplied to the inverter transistors shown, at least two positions situated between the electrical connections of the resistors 73 in a direction parallel to the supply lines are available. In addition, a position may sometimes be used between the resistors and the inverter transistors as is shown at the bottom of Fig. 4. Furthermore, signal conductors crossing each other can also be realised by means of the second level of conductor tracks.

The resistors 73 have a structure which is usual for integrated circuits. They are *p*-type zones which can be obtained simultaneously with the base zones 34. Said zones 73 are situated in the common island 72 above a buried layer 76 belonging to the island 72. A more highly doped *n*-type surface zone 77 is provided at the end of the resistors 73 connected to the supply line 75, simultaneously with the emitter zones 33. The *p-n* junction 78 formed at the boundary of the zones 73 and 77 is short-circuited by the overlying conductive layer 74. The supply line 75 is connected directly to the common island 72 *via* the surface zones 77.

It will be clear that not all resistors need be connected on one side to the common island 72 *via* an adjoining surface zone 77 and a short-circuited *p-n* junction 78. For example, one single connection between the supply line 75 and the common island 72 will in itself often suffice. Only

the leakage currents of the various *p-n* junctions need be dissipated *via* the connection to the supply line, so that the current through said connection is comparatively small.

The sheet resistance of the zones 73 is, for example, approximately 200 Ohm. The resistors each have a value of, for example, approximately 800 Ohm.

The supply line 75 is connected to a connection 48; the supply line 83, as well as the substrate region 29, is connected to the connection 62. Between the connections 48 and 62 a supply voltage can be applied of, for example, approximately 920 mV. This voltage supply is shown diagrammatically in Fig. 5 by the voltage source 79.

The selected supply voltage is equal to the sum of the diode forward voltage V_{BE} of the inverter transistor and the logic swing. The logic swing is equal to the voltage V_{BE} decreased by the diode forward voltage V_{D1} and the collector-emitter voltage V_{CE} of the conductive inverter transistor.

During operation, the output of a first gate circuit having a conductive inverter transistor is connected to the input of a second gate circuit whose inverter transistor then is non-conductive. A voltage drop equal to the logic swing will occur across the resistor associated with the first gate circuit. In fact, the input signal is high and equals the base-emitter forward voltage V_{BE}. A voltage drop which is twice as large as the logic swing will occur across the resistor associated with the second gate circuit. In this case the input signal is low and is approximately equal to the sum of the diode forward voltage V_{D1} and the voltage V_{CE} of the conductive transistor. The current which flows through the second resistor and which is dissipated *via* the collector of the conductive transistor thus is approximately twice as large as the current which flows through the first resistor and which is supplied to the conductive transistor as a base current. Thus the conductive transistor clearly is less overdriven than would have been the case with a more ideal current supply source. In the latter case the base and collector currents would have been substantially equally large while in this example as a result of the low supply voltage in combination with the resistors 73, a factor of two differences occurs. The charge storage in the inverter transistor is decreased accordingly.

Also when a higher supply voltage is used it may be of advantage to supply the currents *via* resistors to the bases of the inverter transistors. The resistance values of the resistors will then have to be larger. If necessary, the resistors may be manufactured in known manner by means of ion implantation. In that case resistance zones having a sheet resistance of, for example, approximately 2 kOhm can simply be obtained. Alternatively, instead of being provided in the semiconductor body, the resistors may be provided on the body, for example, with a layer of resistance material, such as titanium, tantalum or polycrystalline semiconductor material, obtained by deposition or otherwise.

In the second example described, current is dissipated to the connection 61 *via* the vertical and/or the horizontal complementary auxiliary transistor. This electrical connection 61 constitutes the connection of the collector of the auxiliary transistor. In order to reduce the series resistance another arrangement may be favourable in which this connection either does not contact the lower side of the substrate 29 or is connected to it not only at the lower side of the substrate; in this other arrangement on the upper side of the semiconductor body, the deep *p*-type zones 30 are connected to a conductor track and, for example, to the supply line 83 at locations preferably situated at regular mutual distances. If the isolation zones consist of insulating material through out their depth or over a part of their depth, and a complementary auxiliary transistor is used, the provision of deep semiconductor zones at locations regularly arranged between or beside the gate circuit is recommended, which zones extend from the semiconductor surface down to the substrate region and are connected at the semiconductor surface to a conductor track so that in this manner they may serve for the desired dissipation of current.

The integrated circuit according to this second embodiment can also be manufactured entirely in the usual manner by means of methods known in semiconductor technology.

The embodiments described have a combination of properties which are particularly suitable for LSI circuits. First of all, the manufacturing process necessary for this integrated circuit is considerably simpler than for the described known circuit. This integrated circuit in accordance with the invention can be manufactured with the same available process steps by which, for example, LS TTL and I^2L can also be manufactured. In contrast with the known circuit described, LS TTL and I^2L are both on the market as commerical products.

In the second example an *n*-type epitaxial layer was used in a thickness of approximately 3 microns and a resistivity of approximately 0.7 Ohm-cm. As stated, the Schottky coupling diodes were of a type which is also usual in LS TTL having a platinel silicide junction. The diode forward voltage of said diodes was approximately 0.48 V.

As is known, the conventional I^2L is comparatively slow as compared with LS TTL. The minimum delay time of an I^2L inverter having a single output is approximately 10 to 20 nanoseconds (nsec), whereas for LS TTL the minimum delay time is in the proximity of approximately 5 to 7 nsec. The switching times given here are realised in I^2L and LS TTL integrated circuits, respectively, with an epitaxial layer having a thickness of approximately 3 microns. The resistivity of the epitaxial layer for I^2L circuits is approxmately 0.7 Ohm-cm, whereas for LS TTL circuits a value of approximately 0.3 Ohm-cm has been assumed.

It is very surprising that the minimum delay time for the second circuit embodiment in accordance with the invention may be approximately 2 to 3 nsec. At a current level of, for example, approximately 400 micro Amps (μA) the emitter-base diode forward voltage is, for example, approximately 760 milli Volts (mV) and the collector-emitter voltage V_{CE} of the conductive inverter transistor may be approximately 60 mV. The swing of the logic signal then is approximately 220 mV.

In spite of the fact that the inverter transistor in LS TTL is kept from saturation by means of a Schottky clamp diode and the inverter transistor in the circuit in accordance with the invention does become saturated, the latter circuit nevertheless has a delay time which is approximately half as short. The comparable I^2L inverter which also becomes saturated has, on the contrary a 3 to 6 times longer delay time. Apparently, the incorporation of one or more auxiliary transistors as indicated is an unexpectedly effective means in which the consequences of the fact that the inverter transistor becomes saturated are drastically reduced and in which the extent to which the inverter transistor becomes saturated is readily controlled.

For LS TTL τD product, that is the product of the delay time τ and the power dissipation D associated with said delay time in a usual construction is approximately 19 pJ. For I^2L and the circuit in accordance with the invention the τD product is of approximately the same value, namely 0.3 to 2 pJ.

A third quantity which is extremely important for LSI circuits is the packing density or the number of gate circuits which can on an average be realised per mm^2 of semiconductor surface area. In this respect, as is known I^2L with a packing density of approximately 200 to 250 gates/mm^2 is superior to LS TTL which has a packing density of 15 to 20 gates/mm^2. The packing density of the integrated circuit in accordance with the invention is for the second embodiment 120 to 180 gates/mm^2. So this is approximately a factor of 6 more favourable than for LS TTL and less than a factor of 2 worse than for I^2L.

Thus, the present invention can provide a considerable improvement with respect to LS TTL, and the resulting circuit can be of advantage with respect to I^2L for applications in which a switching speed is necessary which is too high for conventional I^2L.

It will be apparent that the invention is not restricted to the embodiments described but that many variations are possible to those skilled in the art without departing from the scope of this invention. For Example, other semiconductor materials, such as germanium or $A_{III}B_V$ compounds, may be used. Furthermore, the conductivity types in the examples may be interchanged, the electric voltages and current directions being adapted accordingly.

In the first embodiment the thickness of the *n*-type surface layer is preferably not larger than approximately 2 microns. An *n*-type epitaxial layer is preferably used and the base zone 34 preferably is obtained by locally converting the epitaxial layer into *p*-type by diffusion and/or ion implantation by overdoping up to the more highly doped *n*-type buried layer.

Other forms of dielectric isolation, for example V grooves or polysilicon-filled grooves may alternatively be used.

In the second embodiment the thickness of the surface layer is preferably not larger than approximately 6.5 microns. Advantageously a thickness of at most approximately 3.5 microns is used. The surface layer will usually be an epitaxial layer, but may also be obtained differently, for example, by diffusion or ion implantation. The collector regions can also be provided as separate regions by doping in a substrate of the opposite conductivity type. The resistivity or in general the doping concentration of the surface layer may be adapted within wide limits. For example, instead of the epitaxial layer of 0.7 Ohm.cm an epitaxial layer of approximately 0.3 Ohm.cm may alternatively be used. Such a change in resistivity influences *inter alia* the series resistance of the coupling diodes.

Both for the vertical and for the lateral complementary auxiliary transistor, the base width of the auxiliary transistor between the, emitter and the collector is preferably approximately 3 microns or less.

The inverter transistor may alternatively be constructed so as to be symmetrical with respect to the non-active part of the base zone. In that case the base contact which comprises the emitter of the auxiliary transistor will, for example, be situated centrally, an emitter zone and one or more coupling diodes being present on two opposite sides of said contact. On each of the said sides a buried layer will be present which continues uninterruptedly from below the emitter zone to below the coupling diode(s). If a lateral complementary auxiliary transistor is incorporated in such a symmetrical transistor, the region which serves as collector thereof will consist of two parts which are situated beside the two other opposite sides of the base zone not facing coupling diodes.

The active dopant concentration in the part of the substrate region which is situated as collector of the vertical complementary auxiliary transistor opposite to the base zone of the inverter transistor is preferably at least a factor of 10 and advantageously at least a factor of 100 lower than the active dopant concentration in the low-ohmic part of the collector region of the inverter transistor.

The coupling diodes 16 may be obtained by means of materials other than the said platinel silicide; thus for example, aluminium, platinum-silicide, cobalt silicide or titanium may be used. This material may be present only in the apertures in the insulating layer, as with the described platinel-silicide junctions, or may form a continuous layer as part of the conductor tracks,

as is often the case with titanium. Such a layer of titanium is then coated with a readily conductive layer of, for example, gold and if necessary, a barrier layer of, for example, platinum may be interposed between the titanium and such a gold layer.

CLAIMS

1. An integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled *via* a diode to a collector of the bipolar transistor, the signal input comprising current supply means, the integrated circuit comprising a semiconductor body having a major surface adjoined by surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first, at least one of the said surface regions belonging to a collector region of the first conductivity type which forms part of the bipolar transistor, said collector region having a high-ohmic and a low-ohmic part, the low-ohmic part extending at and along the interface between the collector region and the substrate region, the bipolar transistor furthermore having an emitter zone of the first conductivity type, which emitter zone adjoins the major surface and in the semiconductor body is separated from the collector region by a base zone of the second conductivity type extending up to the major surface, which base zone is formed in the collector region and is situated above a portion of the collector region, an electrically insulating layer being present at the major surface and having a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and third apertures which are situated beside the base zone and above the collector region, the insulating layer separating from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures, each of the conductor tracks which extends into a third aperture being each coupled to the collector region *via* a rectifying junction which adjoins the collector region, said rectifying junctions forming the said diodes, the bipolar transistor at the major surface being surrounded by an isolation zone by means of which the bipolar transistor is isolated electrically at least during operation from adjacent surface regions of the first conductivity type, characterized in that means are present to restrict shortage of charge-carriers in the high-ohmic part of the collector region, and in addition there is incorporated in the semiconductor structure of the bipolar transistor a further surface zone of the first conductivity type which is provided with an electrical connection and is separated by the base zone from the said collector region, which collector region, base zone and said further surface zone of the first conductivity type serve as emitter, base and collector, respectively of an auxiliary transistor so that, if the bipolar transistor is overdriven, a considerable part of the current flowing through the base connection of the bipolar transistor can be dissipated in the auxiliary transistor and the storage of mobile charge carriers in the overdriven transistor can be considerably restricted.

2. An integrated circuit as claimed in Claim 1, in which said means to restrict storage of charge carriers in the high-ohmic part of the collector region comprises an isolation zone of insulating material extending from the major surface to a larger depth in the semiconductor body than the base zone of the bipolar transistor, said zone of insulating material separating said base zone from the high-ohmic collector part adjoined by said rectifying junctions.

3. An integrated circuit as claimed in Claim 1 or 2, in which the isolation zone by means of which the bipolar transistor is isolated from said adjacent surface regions comprises zones of insulating material extending from the major surface to a larger depth in the semiconductor body than the base zone of the bipolar transistor, the base zone adjoining the insulating material at least over a considerable part of its periphery.

4. An integrated circuit as claimed in Claim 3, in which the base zone of the bipolar transistor at the major surface is surrounded entirely by and adjoins the insulating material.

5. An integrated circuit as claimed in any of the preceding Claims, in which the base zone of the bipolar transistor extends down to the low-ohmic part of the collector region and is separated from the substrate by said low-ohmic part.

6. An integrated circuit as claimed in any of the preceding Claims, in which in the semiconductor structure of the bipolar transistor additonal measures have been taken so that a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone of the second conductivity type and the said collector region of the first conductivity type so that a complementary auxiliary transistor is incorporated to provide means to restrict the storage of charge-carriers in the collector region, which complementary auxiliary transistor has the said base zone as emitter, has the said collector region as base, and has the said region of the second conductivity type as collector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the complementary auxiliary transistor and the storage of mobile charge carriers in the overdriven bipolar transistor can be restricted considerably.

7. An integrated logic circuit as claimed in Claim 6, in which the extent of the low-ohmic part of the collector region in a direction substantially parallel to the major surface is restricted so that said low-ohmic part extends below the said emitter zone and below the said rectifying junctions but does not extend below the part of said base zone underlying the second aperture in the insulating layer whereby a region of the high-ohmic part of the collector region directly adjoins

as is often the case with titanium. Such a layer of titanium is then coated with a readily conductive layer of, for example, gold and if necessary, a barrier layer of, for example, platinum may be interposed between the titanium and such a gold layer.

CLAIMS

1. An integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled *via* a diode to a collector of the bipolar transistor, the signal input comprising current supply means, the integrated circuit comprising a semiconductor body having a major surface adjoined by surface regions of a first conductivity type which are situated on a common substrate region of a second conductivity type opposite to the first, at least one of the said surface regions belonging to a collector region of the first conductivity type which forms part of the bipolar transistor, said collector region having a high-ohmic and a low-ohmic part, the low-ohmic part extending at and along the interface between the collector region and the substrate region, the bipolar transistor furthermore having an emitter zone of the first conductivity type, which emitter zone adjoins the major surface and in the semiconductor body is separated from the collector region by a base zone of the second conductivity type extending up to the major surface, which base zone is formed in the collector region and is situated above a portion of the collector region, an electrically insulating layer being present at the major surface and having a first aperture which overlies the emitter zone, a second aperture which is situated beside the emitter zone and above the base zone, and third apertures which are situated beside the base zone and above the collector region, the insulating layer separating from the semiconductor body conductor tracks which extend for electrical connection into the first, second and third apertures, each of the conductor tracks which extends into a third aperture being each coupled to the collector region *via* a rectifying junction which adjoins the collector region, said rectifying junctions forming the said diodes, the bipolar transistor at the major surface being surrounded by an isolation zone by means of which the bipolar transistor is isolated electrically at least during operation from adjacent surface regions of the first conductivity type, characterized in that means are present to restrict shortage of charge-carriers in the high-ohmic part of the collector region, and in addition there is incorporated in the semiconductor structure of the bipolar transistor a further surface zone of the first conductivity type which is provided with an electrical connection and is separated by the base zone from the said collector region, which collector region, base zone and said further surface zone of the first conductivity type serve as emitter, base and collector, respectively of an auxiliary transistor so that, if the bipolar transistor is overdriven, a considerable part of the current flowing through the base connection of the bipolar transistor can be dissipated in the auxiliary transistor and the storage of mobile charge carriers in the overdriven transistor can be considerably restricted.

2. An integrated circuit as claimed in Claim 1, in which said means to restrict storage of charge carriers in the high-ohmic part of the collector region comprises an isolation zone of insulating material extending from the major surface to a larger depth in the semiconductor body than the base zone of the bipolar transistor, said zone of insulating material separating said base zone from the high-ohmic collector part adjoined by said rectifying junctions.

3. An integrated circuit as claimed in Claim 1 or 2, in which the isolation zone by means of which the bipolar transistor is isolated from said adjacent surface regions comprises zones of insulating material extending from the major surface to a larger depth in the semiconductor body than the base zone of the bipolar transistor, the base zone adjoining the insulating material at least over a considerable part of its periphery.

4. An integrated circuit as claimed in Claim 3, in which the base zone of the bipolar transistor at the major surface is surrounded entirely by and adjoins the insulating material.

5. An integrated circuit as claimed in any of the preceding Claims, in which the base zone of the bipolar transistor extends down to the low-ohmic part of the collector region and is separated from the substrate by said low-ohmic part.

6. An integrated circuit as claimed in any of the preceding Claims, in which in the semiconductor structure of the bipolar transistor additonal measures have been taken so that a region of the second conductivity type provided with an electrical connection co-operates effectively with the said base zone of the second conductivity type and the said collector region of the first conductivity type so that a complementary auxiliary transistor is incorporated to provide means to restrict the storage of charge-carriers in the collector region, which complementary auxiliary transistor has the said base zone as emitter, has the said collector region as base, and has the said region of the second conductivity type as collector, and as a result of which, if the bipolar transistor is overdriven, a considerable part of the current flowing in the base zone of the bipolar transistor can flow through the complementary auxiliary transistor and the storage of mobile charge carriers in the overdriven bipolar transistor can be restricted considerably.

7. An integrated logic circuit as claimed in Claim 6, in which the extent of the low-ohmic part of the collector region in a direction substantially parallel to the major surface is restricted so that said low-ohmic part extends below the said emitter zone and below the said rectifying junctions but does not extend below the part of said base zone underlying the second aperture in the insulating layer whereby a region of the high-ohmic part of the collector region directly adjoins

the substrate region to forming a *p-n* junction, the part of the substrate region adjoining the high-ohmic part of the collector region cooperating as a collector of the complementary auxiliary transistor with the adjoining collector region and base zone of the bipolar transistor.

8. An integrated logic circuit as claimed in Claim 7, in which the base zone of the second conductivity type has an active part which surrounds the emitter zone of the first conductivity type and an adjoining non-active part which serves for the electrical connection of the base zone and above which a second aperture is present, which adjoining non-active part is at least equally large as the said active part, adjoins the said further surface zone of the first conductivity type and provides the emitter of the complementary auxiliary transistor.

9. An integrated logic circuit as claimed in any of Claims 6, 7 or 8, in which, as viewed on the major surface, the first, second and third apertures are arranged in a row in which at least a first aperture overlying an emitter zone is present between one or more third apertures on the one hand and a second aperture on the other hand which overlies a part of the base zone providing the emitter of the complementary auxiliary transistor.

10. An integrated logic circuit as claimed in any of Claims 6 to 10, in which at the major surface beside the base zone a further surface zone of the second conductivity type adjoining the collector region of the first conductivity type is present and extends from the major surface to substantially the same depth in the semi-conductor body as the base zone, said further surface zone of the second conductivity type serving as a collector of the complementary auxiliary transistor and being connected to the substrate region.

11. An integrated logic circuit as claimed in Claim 10, in which the distance at the major surface between the base zone and the further surface zone of the second conductivity type is at most 5 microns.

12. An integrated logic circuit as claimed in Claim 10 or Claim 11, in which the isolation zones are surface zones of the second conductivity type which extend from the major surface down to a larger depth in the semiconductor body than the said further surface zone of the second conductivity type, and the said further surface zone of the second conductivity type overlaps at the major surface the isolation zone adjoining the collector region of the first conductivity type so as to be connected directly to said isolation zone.

13. An integrated logic circuit as claimed in any of Claims 10, 11 or 12, in which the base zone of the second conductivity type is surrounded at the major surface only partly by the said further surface zone of the second conductivity type, and the periphery of the said base zone at the major surface is situated partly opposite to one or more third apertures and for the whole remaining part is situated opposite to the said further surface zone of the second conductivity type.

14. An integrated logic circuit as claimed in Claim 13, in which the base zone of the second conductivity type is substantially rectangular, the said further surface zone of the second conductivity type is substantially U-shaped and surrounds the base zone on three sides, and the third apertures in the insulating layer are arranged beside the fourth side of said base zone.

15. An integrated circuit as claimed in any of the preceding Claims, in which the said further surface zone of the first conductivity type at the major surface occupies an area which is at least one third of the area occupied by the emitter zone.

16. An integrated circuit as claimed in any of the preceding Claims, in which the electrical connection of the further surface zone of the first conductivity type is formed by the conductor track which extends into the second aperture overlying the base zone of the bipolar transistor.

17. An integrated logic circuit having a signal input formed by a base of a bipolar transistor and having a plurality of signal outputs each coupled via a diode to a collector of the bipolar transistor, which transistor has an emitter zone of a first conductivity type and a base zone of a second conductivity type opposite to the first, the signal input comprising current supply means, the integrated circuit comprising in a semiconductor body a semiconductor region of the first conductivity type which belongs to a collector region of the bipolar transistor and is situated on a substrate region of the second conductivity type, said collector region having a high-ohmic part and a low-ohmic part, the low-ohmic part extending at and along the interface between the collector region and the substrate region, the base zone being formed in the collector region and being situated above a portion of the collector region, characterized in that means are present to restrict storage of charge-carriers in the high-ohmic part of the collector region, and in addition there is incorporated in the semiconductor structure of the bipolar transistor a further surface zone of the first conductivity type which is provided with an electrical connection and is separated by the base zone from the said collector region, which collector region, base zone and said further surface zone of the first conductivity type serve as emitter, base and collector, respectively, of an auxiliary transistor so that, if the bipolar transistor is overdriven, a considerable part of the current flowing through the base connection of the bipolar transistor can be dissipated in the auxiliary transistor and the storage of mobile charge carriers in the overdriven transistor can be considerably restricted.

18. An integrated logic circuit substantially as described with reference to Figures 2 and 3 of the

accompanying drawings.

19. An integrated logic circuit substantially as described with reference to Figures 4 and 5 of the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1982. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

(12)

ERRATUM

SPECIFICATION No. 2 008 318 B

Front Page Heading (73) Proprietors *for* N.V. Phillips' *read* N.V. Philips'

THE PATENT OFFICE
28th June, 1982