A Tensile Strained NMOS Transistor Using Group III-N Source/Drain Regions

FIELD OF THE INVENTION

[0001] The invention relates to the field of transistors with strain and compression on channel regions.

PRIOR ART AND RELATED ART

[0002] It is recognized that improved performance in PMOS transistors is obtained when a uniaxial compressive strain is imparted directly to the channel of the transistors from, for instance, embedded silicon germanium (SiGe) source/drain regions. Similarly, it is known that increased performance is obtained in an NMOS transistor when uniaxial tensile strain is placed on its channel. In some cases this tensile strain is obtained from a silicon nitride capping layer, as will be discussed in conjunction with Figure 1. Additionally, see "Sacrificial Capping Layer for Transistor Performance Enhancement," US Serial No. 11/174,230, filed June 30, 2005.

BRIEF DESCRIPTION OF THE DRAWINGS

[0003] Figure 1 is a cross-sectional, elevation view of a substrate showing a p channel and n channel field-effect transistor (FET) as fabricated in the prior art.

[0004] Figure 2 is a cross-sectional, elevation view of a substrate showing one embodiment of placing strain on a channel region of an n channel.

[0005] Figure 3 is a cross-sectional, elevation view of a substrate showing another embodiment for placing tensile strain on the channel region of an n channel.

[0006] Figure 4 is a cross-sectional, elevation view of a substrate illustrating one embodiment for placing tensile strain on an n channel transistor in conjunction with the fabrication of a p channel transistor.

[0007] Figure 5 is a cross-sectional, elevation view of a substrate showing another embodiment for placing tensile strain on an n channel transistor when fabricated in conjunction with a p channel transistor.

DETAILED DESCRIPTION

[0008] An n channel transistor and method of fabricating the transistor where tensile strain is placed on the silicon channel is described. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art, that the present invention may be practiced without these specific details. In other instances, well-known structures and fabrication processes are not described in detail in order not to unnecessarily obscure the present invention.

[0009] Referring first to the prior art of Figure 1, a p channel transistor 10 and n channel transistor 11 are shown fabricated on a substrate 12. The transistors are separated by a shallow trench isolation region 14. The transistor 10 has a channel region 15 insulated from the gate 17 by, for instance, a high k oxide 16. Similarly, the channel region 20 of the transistor 11 is separated from the gate 23 by the high k oxide 22. In one embodiment, the gate oxides 16 and 22 are hafnium dioxide (HfO_2) or zirconium dioxide (ZrO_2). The gates 17 and 23 may be metal

gates with work functions targeted such that a higher work function is used for the enhancement mode transistor 11, and a lower work function for the depletion mode transistor 10. In another embodiment, a silicon dioxide gate insulator is used with the gates fabricated from polysilicon.

[0010] As mentioned earlier, it is known that having the channel 15 of the transistor 10 in compression provides a better performing transistor. To this end, the substrate is etched at regions 24 and 25, and SiGe is epitaxially grown. The lattice mismatch between SiGe and Si causes the resultant source and drain regions to be in compression and thereby provides compression to the channel region 15. As shown in Figure 1, the source and drain regions are doped with a p type dopant, such as boron.

[0011] To provide the tensile strain for the n channel transistor 11, a high tensile silicon nitride capping layer 30 is used to impart uniaxial tensile strain to the channel 20 through the source and drain regions of transistor 11. This high tensile strain capping layer, as shown in Figure 1, also covers the p channel transistor and degrades its hole mobility somewhat, but not compared to the overall increase in performance obtained by placing the enhancement mode transistors in tensile stress.

[0012] As transistor densities continue to increase and gate pitch continues to decrease, there of course, is a reduction in contact area. This results in a relatively larger increase in the parasitic series resistance of the transistors, particularly the n channel transistors. The p channel transistors do not suffer as much from this scaling since the embedded SiGe source/drain regions and the lower barrier height associated with the silicide formed on these regions, provide lower series resistance.

[0013] As described below, a compound comprising a Group III element and nitride such as gallium nitride (GaN) and indium nitride (InN) is used in the source and drain regions to provide tensile strain on the channel for the n channel transistors. The Group III-N regions may be raised source/drain regions such as shown in Figure 2, or embedded source/drain regions as shown in Figure 3. The larger lattice mismatch between the Group III-N compound and silicon results in a highly tensile strain in the Group III-N film which results in a high tensile strain in the silicon channel, thereby enhancing electron mobility.

[0014] A benefit of using the Group III-N compound is the high electron mobility and high carrier concentration arising from polarization induced doping. For instance, in InN films with $\mu > 3{,}000\ cm^2V^{-1}s^{-1}$, $R_{sheet} = 27$ ohm/sq has been experimentally demonstrated. Low resistance ohmic contacts have also been demonstrated due to the very high surface electron accumulation resulting from Fermi level pinning. This is particularly beneficial for gate length and gate pitch scaling, as transistor density increases.

[0015] In the embodiments described below, InN is described as the Group III-N compound. As mentioned, other compounds such as GaN may be used. Moreover, the InN may be epitaxially grown on a step graded buffer layer of InGaN or GaN epitaxially grown on Si.

[0016] Figure 2 illustrates one embodiment with an n channel transistor disposed on a monocrystalline substrate 60. The InN regions 61 are grown in an ordinary epitaxial process and doped with an n type dopant such as arsenic or phosphorous. The doping may occur during the growth of the regions or subsequently through, for example, ion implantation. In Figure 2 the regions 61 are

disposed on the substrate, that is, they are not recessed but rather are raised source and drain regions. Note that the regions 61 in Figure 2 and like regions in the other figures are spaced apart from the oxide 62 and gate 63. This illustrates the use of sidewall spacers typically used after the formation of the extension, or tip, source and drain regions, and before the formation of the main source and drain regions.

[0017] Figure 3 shows another embodiment, where prior to the formation of the source and drain regions, selective etching of the substrate 70 occurs to allow subsequent growth of embedded regions 71. This embedding is what is shown in Figure 1 for the SiGe regions. The embedded source and drain region 71 disposed in the substrate 70 of Figure 3 are again spaced apart from the oxide 72 and gate 73.

[0018] In both Figures 2 and 3, because of the lattice mismatch between the silicon and the InN, the InN regions are in tension which produces corresponding tension in the channel regions of the n channel transistors.

[0019] In all the figures, it will be appreciated that with a replacement gate process, a dummy gate and an insulator other than a high k insulator may be present when the source/drain regions are grown. The dummy gate is replaced with a metal gate after the source/drain regions are grown for this process.

[0020] In Figure 4, one embodiment is shown for integrating the Group III-N source/drain regions into an integrated circuit having depletion mode transistors with compressive strained channels. A substrate 80, separated into two regions by a shallow trench isolation region 81, is illustrated. One region includes a p channel transistor 82, and the other, an n channel transistor 83. In a typical process after the gates and spacers are formed for the transistors, selective etching occurs to etch the silicon substrate to provide recesses for all the source and drain regions as indicated

by 84. As mentioned earlier, the gates at this point in the processing may be dummy gates. Then, one of the p channel and n channel transistor regions are covered while the appropriate source/drain regions are grown at the other regions.

[0021] For instance, referring to Figure 4 after the formation of the recesses 84, the n channel transistor regions are covered with a photoresist. Then, the SiGe 85 is grown and doped with a p type dopant. Following this, the p channel transistors are covered allowing the InN regions 86 to be epitaxially grown and doped to provide the recess source and drain regions for the enhancement mode transistors, as shown in Figure 4.

[0022] Note in Figure 4 the gates are shown as p+ or n+. This is used to indicate that where polysilicon gates are used, the gates are doped, for example, when the source and drain regions are doped. Where metal gates are used, the p+ and n+ is used to indicate the targeted work function for the metal appropriate for either an enhancement mode or depletion mode transistor.

[0023] Figure 5 illustrates another embodiment where the InN source and drain regions are integrated into all the CMOS transistors. Fewer masking steps are required for the embodiment of Figure 5 when compared to the embodiment of Figure 4.

[0024] First, the regions for the n channel transistors may be covered after the gates (or dummy gates) are formed. Then, the substrate 90 is etched at the proposed locations of the source and drain regions for the p channel transistors as indicated by regions 91. This allows a subsequent growth of the SiGe at these regions for recessed p+ SiGe source and drain regions. As indicated in Figure 5, this places compressive strain on the silicon channels of the depletion mode transistors.

[0025] Following this, InN is selectively grown on all the source and drain regions. That is, it is grown both on the SiGe and on the Si, adjacent the gates of the n channel transistors, as shown for transistors 92 and 93 of Figure 5. This results in tensile strain on the silicon channel of the n channel transistor. The InN on the SiGe does degrade hole mobility to some extent in transistor 92, but not significantly enough to overcome the benefit of the SiGe regions.

[0026] Other combinations of recessed and raised source and drain regions are possible. For example, InN regions may be recessed while the SiGe regions are not recessed. In another embodiment, the InN regions can be recessed and the SiGe grown for raised source and drain regions for the p channel transistors, and simultaneously grown on the embedded InN source and drain regions of the n channel transistors.

[0027] Thus, n channel transistors have been described where tensile strained channels are formed using a Group III-N compound. The resultant source and drain regions may be raised or recessed, and formed in conjunction with compressive source and drain regions for p channel transistors.

CLAIMS

What is claimed is:

1. A method for fabricating an n channel transistor comprising:
forming Group III-N regions adjacent a channel region; and
doping the Group III-N regions with an n type dopant.

2. The method of claim 1, wherein the Group III-N regions are InN regions.

3. The method of claim 1, wherein the Group III-N regions are recessed into a silicon substrate.

4. The method of claim 1, wherein the Group III-N regions are raised from a silicon substrate.

5. The method of claim 1, forming a p channel transistor with the fabrication of the n channel transistor.

6. The method of claim 5, including forming SiGe regions adjacent a channel region of the p channel transistor.

7. The method of claim 6, including recessing the SiGe regions into a silicon substrate.

8. The method of claim 6, wherein the SiGe are raised from a silicon substrate.

9. The method of claim 2, including growing the InN regions on a step graded buffer region of GaN formed on a silicon substrate.

10. A method for fabricating an n-channel transistor comprising:
forming tensilly stressed regions of a Group III-N material adjacent a channel region;

doping the material with an n type dopant.

11. The method of claim 10, wherein the material comprises InN.

12. The method of claim 11, including fabricating a p-channel transistor while fabricating the n channel transistor.

13. The method of claim 12, including forming SiGe regions adjacent a channel region of the p channel transistor.

14. The method of claim 11, including recessing the InN material into a silicon substrate.

15. The method of claim 11, wherein the InN material is raised from a silicon substrate.

16. The method of claim 11, wherein the InN is grown on a GaN region.

17. The method of claim 16, including growing the InN region on a step graded region comprising GaN and InGaN formed on a silicon substrate.

18. An n channel transistor having a source and drain region comprising a Group III-N compound.

19. The transistor of claim 18, wherein the compound comprises InN.

20. The transistor of claim 19, wherein the InN is doped with arsenic or phosphorous.

21. The transistor of claim 20, wherein the InN is disposed over a GaN region formed on silicon.